TGS96AD56-125

Four-Channel Analog-to-Digital Converter

Data sheet

Features

- Signal-to-Noise Ratio (SNR): 79 dBFS (9.7 MHz, VREF = 1.4 V)
- Signal-to-Noise Ratio (SNR): 77 dBFS (9.7 MHz, VREF = 1.0 V)
- Spurious-Free Dynamic Range (SFDR): 85 dBc (to Nyquist frequency, VREF = 1.4 V)
- Spurious-Free Dynamic Range (SFDR): 91 dBc (to Nyquist frequency, VREF = 1.0 V)
- JESD204B Subclass 1 encoding, serial digital output
- Analog input range (adjustable): 2.0 Vp-p / 2.8 Vp-p
- 1.8 V power supply operation
- Low power consumption: ≤ 195 mW per channel at 125 MHz mode
- Differential Nonlinearity (DNL): ±0.6 LSB
- Integral Nonlinearity (INL): ±5.0 LSB
- 650 MHz full power analog input bandwidth
- Serial port control:

  Full-chip and individual channel power-down modes

  Built-in and user-defined test modes

  Multi-chip synchronization and clock divider functions

  Standby mode

Application Range

- Medical Imaging
- High-Speed Imaging
- Radio Receivers
- Portable Measurement Equipment

Product Overview

This product is a 4-channel, 16-bit, 125 MSPS sampling rate analog-to-digital converter (ADC), specifically designed and developed for low power consumption, small size, and flexibility of use. The conversion rate of this product can reach up to 125 MSPS, offering excellent dynamic performance and ultra-low power consumption, making it suitable for a wide range of applications.

The ADC operates from a single 1.8 V power supply and features an LVPECL/CMOS/LVDS compatible sampling clock input. It requires no external voltage reference or driver to meet its requirements.

It supports independent power-down of each internal channel; when all channels are disabled, typical power consumption is less than 14 mW. The ADC integrates a variety of functions, including programmable clock output, data alignment, and digital test pattern generation. Available digital test patterns include built-in fixed test patterns and pseudo-random test patterns, as well as user-defined test patterns via the Serial Port Interface (SPI).

Functional Block Diagram

This product is offered in a 56-pin package. The ADC is rated for operation from -40°C to +85°C.

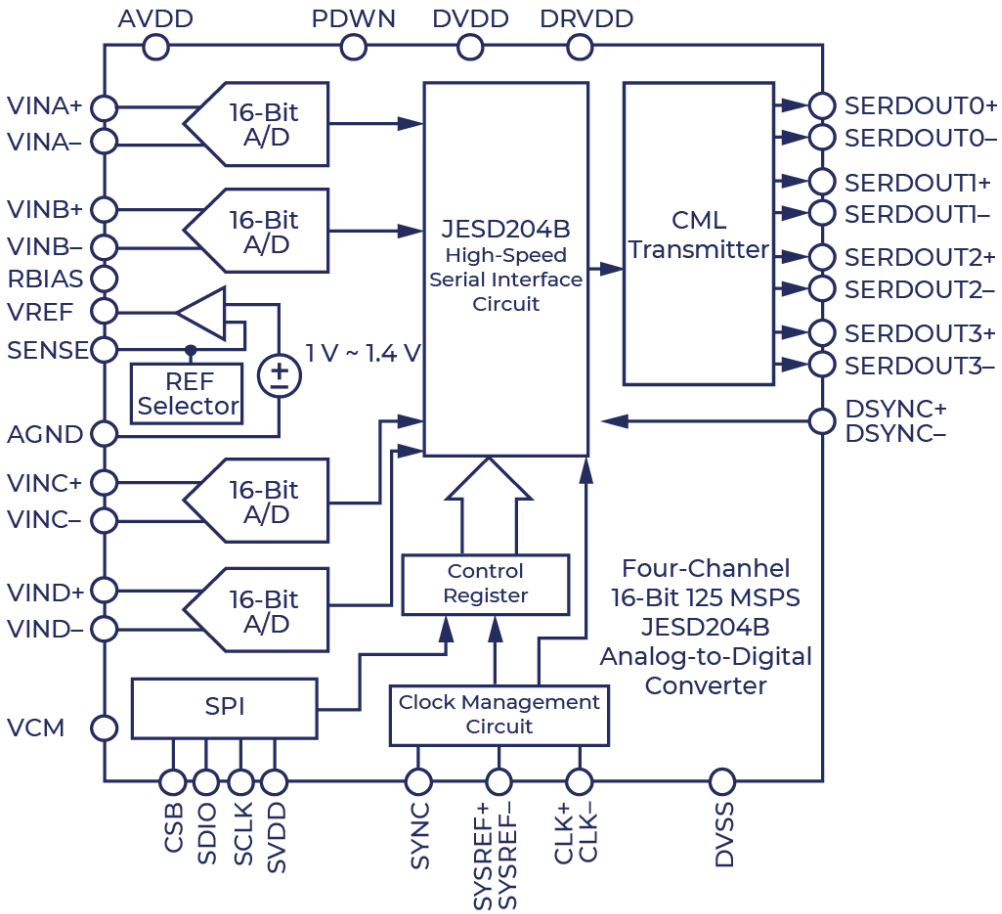

Figure 1. Functional Block Diagram

Product Features

1. Highly integrated: Four high-speed 16-bit analog-to-digital converters are integrated into a single small-footprint chip.
2. Integrated on-chip phase-locked loop (PLL): The PLL multiplies the ADC sampling clock to provide the corresponding JESD204B data clock to the user.
3. Configurable JESD204B output mode: Supports data rates up to 6.4 Gbps per channel.
4. JESD204B output module: Supports 1/ 2/ 4 lane configurations.

5. Low power consumption: Less than 200 mW per channel at 125 MSPS.

6. SPI control: Provides flexible configuration features to meet various system requirements.

Technical specifications

- DC Specifications (V_{REF} = 1.4 V)

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 Vp-p full-scale differential input, 1.4 V reference voltage, unless otherwise specified A_{IN} = -1.0 dBFS.

Table 1.

Parameters	Temp.	Min.	Typ.	Max.	Unit
Resolution	25°C		16		Bits
Accuracy					
No Missing Codes	25°C		Design Guarantee		
Offset Error	25°C		0.2		%FSR
Offset Matching	25°C		0.05		%FSR
Gain Error	25°C		1.2		%FSR
Gain Matching	25°C		0.95		%FSR
Differential Nonlinearity (DNL)	25°C		±0.5		LSB
Integral Nonlinearity (INL)	25°C		±5.0		LSB
Temperature Drift					
Gain Error	Full Temp		5.2		ppm/°C
Offset Error	Full Temp		-2.5		ppm/°C
Internal Reference Voltage Source					
Internal Reference Voltage Source	25°C		1.4		V
Load Regulation (1.0 mA)	25°C		4		mV
Input Resistance	25°C		7.5		kΩ
Input Referred Noise					
V_{REF} = 1.4 V	25°C		2.1		LSB rms
Analog Input					
Differential Input Voltage	25°C		2.8		Vp-p
Common-Mode Voltage	25°C		0.9		V
Common-Mode Range	25°C	0.7		1.1	V
Differential Input Resistance	25°C		2.6		kΩ
Differential Input Capacitance	25°C		7		pF
Power Supply					
AVDD	25°C		1.8		V

DVDD, DRVDD	25°C		1.8		V
I_{AVDD} (125 MSPS, 2 Lanes)	25°C		288		mA
I_{DVDD} (125 MSPS, 2 Lanes)	25°C		67		mA
I_{DRVDD} (125 MSPS, 2 Lanes)	25°C		83		mA
Total Power Dissipation					
DC Input (125 MSPS, 2 Lanes)	25°C		706		mW
Sine Input (125 MSPS, 2 Lanes)	25°C		788		mW
Power-Down Mode	25°C		14		mW
Standby Mode	25°C		547		mW

- **DC Specifications (V_{REF} = 1.0 V)**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 Vp-p full-scale differential input, 1.0 V reference voltage, unless otherwise specified, A_{IN} = -1.0 dBFS.

Table 2.

Parameter	Temp.	Min.	Typ.	Max.	Unit
Resolution	25°C		16		Bits
Accuracy					
No Missing Codes	25°C		Design Guarantee		
Offset Error	25°C		0.2		%FSR
Offset Matching	25°C		0.13		%FSR
Gain Error	25°C		1.0		%FSR
Gain Matching	25°C		0.4		%FSR
Differential Nonlinearity (DNL)	25°C		±0.5		LSB
Integral Nonlinearity (INL)	25°C		±4.0		LSB
Temperature Drift					
Gain Error	Full Temp		3.1		ppm/°C
Offset Error	Full Temp		-3		ppm/°C
Internal Reference Voltage Source					
Internal Reference Voltage Source	25°C		1.0		V
Load Regulation (1.0 mA)	25°C		2		mV
Input Resistance	25°C		7.5		kΩ
Input Referred Noise					
V_{REF} = 1.4 V	25°C		2.7		LSB rms
Analog Input					

Differential Input Voltage	25°C		2.0		Vp-p
Common-Mode Voltage	25°C		0.9		V
Common-Mode Range	25°C	0.5		1.3	V
Differential Input Resistance	25°C		2.6		kΩ
Differential Input Capacitance	25°C		7		pF
Power Supply					
AVDD	25°C		1.8		V
DVDD, DRVDD	25°C		1.8		V
I_{AVDD} (125 MSPS, 2 Lanes)	25°C		276		mA
I_{DVDD} (125 MSPS, 2 Lanes)	25°C		69		mA
I_{DRVDD} (125 MSPS, 2 Lanes)	25°C		83		mA
Total Power Dissipation					
DC Input (125 MSPS, 2 Lanes)	25°C		688		mW
Sine Input (125 MSPS, 2 Lanes)	25°C		771		mW
Power-Down Mode	25°C		14		mW
Standby Mode	25°C		520		mW

- **AC Specifications (V_{REF} = 1.4 V)**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 Vp-p full-scale differential input, 1.4 V reference voltage, unless otherwise specified, A_{IN} = -1.0 dBFS.

Table 3.

Parameter	Temp.	Min.	Typ.	Max.	Unit
Signal-to-Noise Ratio (SNR)					
f_{IN} = 9.7 MHz	25°C		79.0		dBFS
f_{IN} = 16 MHz	25°C		78.2		dBFS
f_{IN} = 64 MHz	25°C		76.3		dBFS
f_{IN} = 128 MHz	25°C		71.5		dBFS
f_{IN} = 201 MHz	25°C		69.7		dBFS
f_{IN} = 301 MHz	25°C		66.2		dBFS
Signal-to-Noise and Distortion Ratio (SINAD)					
f_{IN} = 9.7 MHz	25°C		78.3		dBFS
f_{IN} = 16 MHz	25°C		77.7		dBFS
f_{IN} = 64 MHz	25°C		75.2		dBFS
f_{IN} = 128 MHz	25°C		70.9		dBFS

f_{IN} = 201 MHz	25°C		68.7		dBFS
f_{IN} = 301 MHz	25°C		65.9		dBFS
Effective Number of Bits (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.7		Bits
f_{IN} = 16 MHz	25°C		12.6		Bits
f_{IN} = 64 MHz	25°C		12.2		Bits
f_{IN} = 128 MHz	25°C		11.5		Bits
f_{IN} = 201 MHz	25°C		11.1		Bits
f_{IN} = 301 MHz	25°C		10.7		Bits
Spurious-Free Dynamic Range (SFDR)					
f_{IN} = 9.7 MHz	25°C		93.2		dBc
f_{IN} = 16 MHz	25°C		90.1		dBc
f_{IN} = 64 MHz	25°C		82.8		dBc
f_{IN} = 128 MHz	25°C		82.3		dBc
f_{IN} = 201 MHz	25°C		76.1		dBc
f_{IN} = 301 MHz	25°C		82.3		dBc
Worst Harmonic (2nd or 3rd)					
f_{IN} = 9.7 MHz	25°C		93.2		dBc
f_{IN} = 16 MHz	25°C		90.1		dBc
f_{IN} = 64 MHz	25°C		82.8		dBc
f_{IN} = 128 MHz	25°C		82.3		dBc
f_{IN} = 201 MHz	25°C		76.1		dBc
f_{IN} = 301 MHz	25°C		82.3		dBc
Worst Other Harmonic (excluding 2-nd or 3-rd)					
f_{IN} = 9.7 MHz	25°C		-96		dBc
f_{IN} = 16 MHz	25°C		-92		dBc
f_{IN} = 64 MHz	25°C		-90		dBc
f_{IN} = 128 MHz	25°C		-89		dBc
f_{IN} = 201 MHz	25°C		-93		dBc
f_{IN} = 301 MHz	25°C		-90		dBc
Two-Tone Intermodulation Distortion (IMD): Input Amplitude = -7.0 dBFS					
f_{IN1} = 70.5 MHz, f_{IN1} = 72.5 MHz	25°C		-84		dBc
Crosstalk					

In-Range Crosstalk [2]	25°C		-93		dB
Over-Range Crosstalk [3]	25°C		-89		dB
Analog Input Bandwidth (Full Power)	25°C		650		MHz

1. Tested at $f_{IN} \geq 401$ MHz, A_{IN} = -5.0 dBFS.
2. One channel input with f_{IN} = 70 MHz, -1.0 dBFS analog input, and no input signal on the adjacent channel.
3. Over-range is defined as 3 dB above the full-scale range.

- **AC Specifications (V_{REF} = 1.0 V)**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.0 Vp-p full-scale differential input, 1.0 V reference voltage, unless otherwise specified, A_{IN} = -1.0 dBFS.

Table 4.

Parameter	Temp.	Min.	Typ.	Max.	Unit
Signal-to-Noise Ratio (SNR)					
f_{IN} = 9.7 MHz	25°C		77.4		dBFS
f_{IN} = 16 MHz	25°C		77.1		dBFS
f_{IN} = 64 MHz	25°C		75.3		dBFS
f_{IN} = 128 MHz	25°C		71.9		dBFS
f_{IN} = 201 MHz	25°C		69.2		dBFS
f_{IN} = 301 MHz	25°C		65.8		dBFS
Signal-to-Noise and Distortion Ratio (SINAD)					
f_{IN} = 9.7 MHz	25°C		77.3		dBFS
f_{IN} = 16 MHz	25°C		76.9		dBFS
f_{IN} = 64 MHz	25°C		75.1		dBFS
f_{IN} = 128 MHz	25°C		71.6		dBFS
f_{IN} = 201 MHz	25°C		68.5		dBFS
f_{IN} = 301 MHz	25°C		65.6		dBFS
Effective Number of Bits (ENOB)					
f_{IN} = 9.7 MHz	25°C		12.5		Bits
f_{IN} = 16 MHz	25°C		12.4		Bits
f_{IN} = 64 MHz	25°C		12.2		Bits
f_{IN} = 128 MHz	25°C		11.6		Bits
f_{IN} = 201 MHz	25°C		11.1		Bits
f_{IN} = 301 MHz	25°C		10.6		Bits
Spurious-Free Dynamic Range (SFDR)					

f_{IN} = 9.7 MHz	25°C		97.6		dBc
f_{IN} = 16 MHz	25°C		94.9		dBc
f_{IN} = 64 MHz	25°C		92.5		dBc
f_{IN} = 128 MHz	25°C		86.0		dBc
f_{IN} = 201 MHz	25°C		77.5		dBc
f_{IN} = 301 MHz	25°C		80.3		dBc
Worst Harmonic (2-nd or 3-rd)					
f_{IN} = 9.7 MHz	25°C		-97.6		dBc
f_{IN} = 16 MHz	25°C		-94.9		dBc
f_{IN} = 64 MHz	25°C		-92.5		dBc
f_{IN} = 128 MHz	25°C		-86.0		dBc
f_{IN} = 201 MHz	25°C		-77.5		dBc
f_{IN} = 301 MHz	25°C		-80.3		dBc
Worst Other Harmonic (excluding 2-nd or 3-rd)					
f_{IN} = 9.7 MHz	25°C		-95		dBc
f_{IN} = 16 MHz	25°C		-95		dBc
f_{IN} = 64 MHz	25°C		-94		dBc
f_{IN} = 128 MHz	25°C		-89		dBc
f_{IN} = 201 MHz	25°C		-91		dBc
f_{IN} = 301 MHz	25°C		-89		dBc
Two-Tone Intermodulation Distortion (IMD): Input Amplitude = -7.0 dBFS					
f_{IN1} = 70.5 MHz, f_{IN1} = 72.5 MHz	25°C		-89		dBc
Crosstalk					
In-Range Crosstalk [2]	25°C		-94		dB
Over-Range Crosstalk [3]	25°C		-89		dB
Analog Input Bandwidth (Full Power)	25°C		650		MHz

1. Tested at $f_{IN} \geq 401$ MHz, with A_{IN} = -5.0 dBFS.
2. One channel input with f_{IN} = 70 MHz, -1.0 dBFS analog input, and no input signal on the adjacent channel.
3. Over-range is defined as 3 dB above the full-scale range.

- **Digital Specifications**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 Vp-p full-scale differential input, 1.4 V reference voltage, unless otherwise specified, A_{IN} = -1.0 dBFS.

Table 5.

Parameter	Temp.	Min.	Typ.	Max.	Unit
Clock Input (CLK+, CLK-)					
Logic Compatibility			CMOS/LVDS/ LVPECL		
Differential Input Voltage Range	Full Temp	0.2		3.6	Vp-p
Input Voltage Range	Full Temp	AGND−0.2		AVDD+0.2	V
Input Common-Mode Voltage	Full Temp		0.9		V
Input Resistance (Differential)	25℃		15		kΩ
Input Capacitance	25℃		4		pF
DSYNC Input (DSYNC+/DSYNC-)					
Logic Compatibility	Full Temp		LVDS		
Internal Common-Mode Bias	Full Temp		0.9		V
Differential Input Voltage Range	Full Temp	0.3		3.6	Vp-p
Input Voltage Range	Full Temp	DGND		DVDD	V
Input Common-Mode Voltage Range	Full Temp	0.9		1.4	V
High-Level Input Current	Full Temp	−5		+5	μA
Low-Level Input Current	Full Temp	−5		+5	μA
Input Capacitance	Full Temp		1		pF
Input Resistance	Full Temp	12	16	20	kΩ
DSYSREF Input (DSYSREF+ / DSYSREF-)					
Logic Compatibility			LVDS		
Internal Common-Mode Bias	Full Temp		0.9		V
Differential Input Voltage Range	Full Temp	0.3		3.6	Vp-p
Input Voltage Range	Full Temp	DGND		DVDD	V
Input Common-Mode Voltage Range	Full Temp	0.9		1.4	V
High-Level Input Current	Full Temp	−5		+5	μA
Low-Level Input Current	Full Temp	−5		+5	μA
Input Capacitance	Full Temp		4		pF
Input Resistance	Full Temp	8	10	12	kΩ
Logic Inputs (PDWN, SYNC, SCLK)					
Logic 1 Voltage Range	Full Temp	1.2		AVDD+0.2	V
Logic 0 Voltage Range	Full Temp	0		0.8	V
Input Resistance	25℃		30		kΩ

Input Capacitance	25°C		2		pF
Logic Input (CSB)					
Logic 1 Voltage Range	25°C	1.2		AVDD+0.2	V
Logic 0 Voltage Range	25°C	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF
Logic Input (SDIO)					
Logic 1 Voltage Range	25°C	1.2		AVDD+0.2	V
Logic 0 Voltage Range	25°C	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
Digital Output (SERDOUTx+, SERDOUTx-)					
Logic Compatibility	Full Temp		CML400		
Differential Output Voltage (V_{OD})	Full Temp	400	600	750	mV
Output Offset Voltage (V_{OS})	Full Temp	0.75	DRVDD/2	1.05	V

- **Switching Specifications**

AVDD = 1.8 V, DRVDD = 1.8 V, 2.8 Vp-p full-scale differential input, 1.4 V reference voltage, unless otherwise specified, AIN = -1.0 dBFS.

Parameter	Temp.	Min.	Typ.	Max.	Unit
Clock Parameters					
Input Clock Rate	Full Temp	40		1000	MHz
Conversion Rate		40		125	MSPS
Clock High Pulse Width (t_{EH})			4		ns
Clock Low Pulse Width (t_{EL})			4	1.4	ns
SYNC Setup Time to Clock				-0.4	ns
SYNC Hold Time to Clock			370	600	ns
DSYSREF Setup Time to Clock (t_{REFS})			-92	0	ps
DSYSREF Hold Time to Clock (t_{REFH})					ps
Data Output Parameters					
Data Output Period or Unit Interval (UI)	Full Temp		$L/(20 \times M \times f_S)$		sec
Data Output Duty Cycle	25°C		50		%
Data Valid Time	25°C		0.81		UI

PLL Lock Time (t_{LOCK})	25°C		25		µs
Wake-Up Time					
Standby	25°C		250		ns
ADC (Power-Down Mode)	25°C		375		µs
Output (Power-Down Mode)	25°C		50		µs
DSYNC Falling Edge to First K.28 Character	Full Temp	4			Multiframe
K.28 Character Duration in CGS Phase	Full Temp	1			Multiframe
Pipeline Delay					
JESD204B M4, L1 Mode (Latency)	Full Temp		23		Period 7
JESD204B M4, L2 Mode (Latency)	Full Temp		29		Period 7
JESD204B M4, L4 Mode (Latency)	Full Temp		44		Period 7
Data Rate per Channel	Full Temp			6.4	Gbps
Deterministic Jitter (DJ)					
At 6.4 Gbps	Full Temp		8		Ps
Random Jitter (RJ)					
At 6.4 Gbps	Full Temp		1.25		ps rms
Output Rise Time / Fall Time	Full Temp		50		ps
Differential Termination Resistor	25°C		100		Ω
Aperture Parameters					
Aperture Delay (t_A)	25°C		1		
Aperture Uncertainty (Jitter, t_J)	25°C		135		
Over-Range Recovery Time	25°C		1		

- **Timing Specifications**

Table 7.

Parameter	Description	Limits	Unit
SPI Timing Requirements			
t_{DS}	Data Setup Time to SCLK Rising Edge	2	ns (min.)
t_{DH}	Data Hold Time to SCLK Rising Edge	2	ns (min.)
t_{CLK}	SCLK Period	40	ns (min.)
t_S	CSB Setup Time to SCLK	2	ns (min.)
t_H	CSB Hold Time to SCLK	2	ns (min.)
t_{HIGH}	SCLK High Pulse Width	10	ns (min.)
t_{LOW}	SCLK Low Pulse Width	10	ns (min.)

t_{EN_SDIO}	Time required for SDIO pin to switch from input state to output state relative to SCLK falling edge	10	ns (min.)
t_{DIS_SDIO}	Time required for SDIO pin to switch from output state to input state relative to SCLK falling edge	10	ns (min.)

Timing Diagrams for SPI register settings, refer to the "Memory Map Register Table" section.

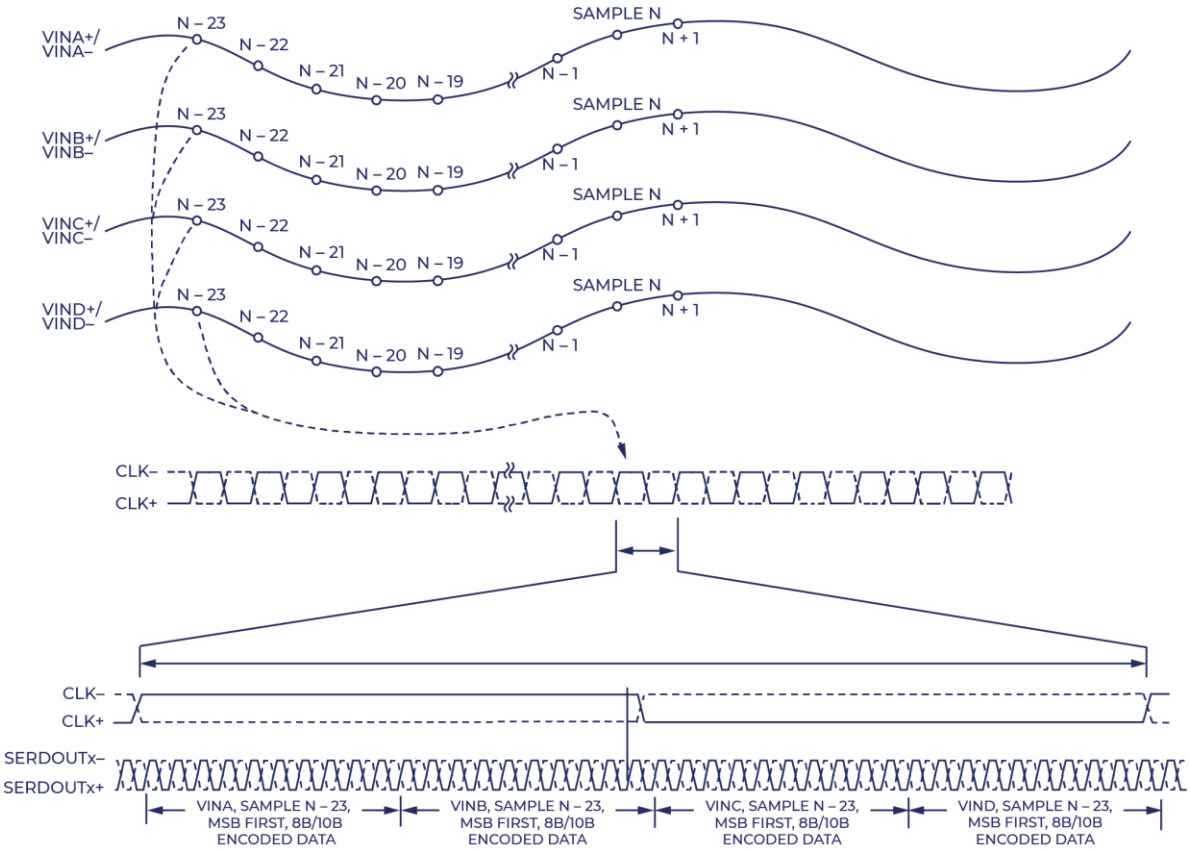

Figure 2. Data Output Timing

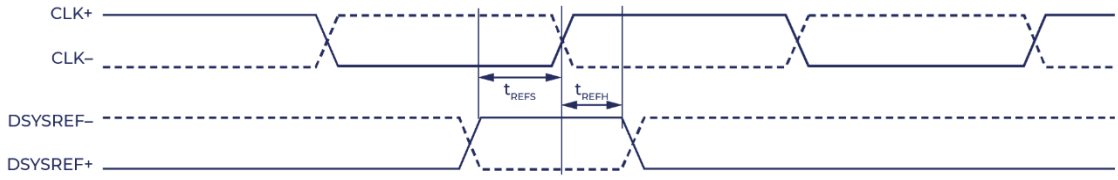

Figure 3. DSYSREF+/DSYSREF- Setup and Hold Time (Clock Divider = 1)

Absolute Maximum Ratings

Parameter	Rating
Electrical	−0.3 V to +2.0 V
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
DVDD to DVSS	−0.3 V to +2.0 V
SVDD to AGND	−0.3 V to +2.0 V
Digital Output to AGND	−0.3 V to +2.0 V
CLK+, CLK− to AGND	−0.3 V to +2.0 V
VINx+, VINx− to AGND	−0.3 V to +2.0 V
DSYSREF+, DSYSREF− to AGND DSYNC−, DSYNC+ to AGND	−0.3 V to +2.0 V
SCLK, SDIO, CSB, PDWN to AGND SYNC to AGND	−0.3 V to +3.9 V
RBIAS to AGND	−0.3 V to +2.0 V
V_{CM}, V_{REF}, SENSE to AGND	
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature	150°C
Pin Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Resistance (θ_{JA}): Test conditions for θ_{JA} are based on a four-layer printed circuit board (PCB, simulation) with a solid ground plane. The exposed pad is soldered to the PCB ground.

Package Type	Airflow Velocity (m/s)	θ_{JA} (°C/W)	θ_{JB} (°C/W)[1]	θ_{JC} (Top) (°C/W) [1]	θ_{JC} (Bottom) (°C/W) [1]
56-Lead LFCSP, 8 mm × 8 mm	0	22.4	7.7	7.42	2.29
	1	19.0	N/A	N/A	N/A
	2.5	17.6	N/A	N/A	N/A

ESD Warning
Electrostatic Sensitive Device
All pins have been proven to withstand 2 kV electrostatic discharge (ESD) under the Human Body Model (HBM).
Although this device features proprietary ESD protection circuitry, it may still be damaged by high-energy electrostatic shocks. Appropriate ESD precautions should be taken during handling and assembly.

Pin Configuration and Function Description

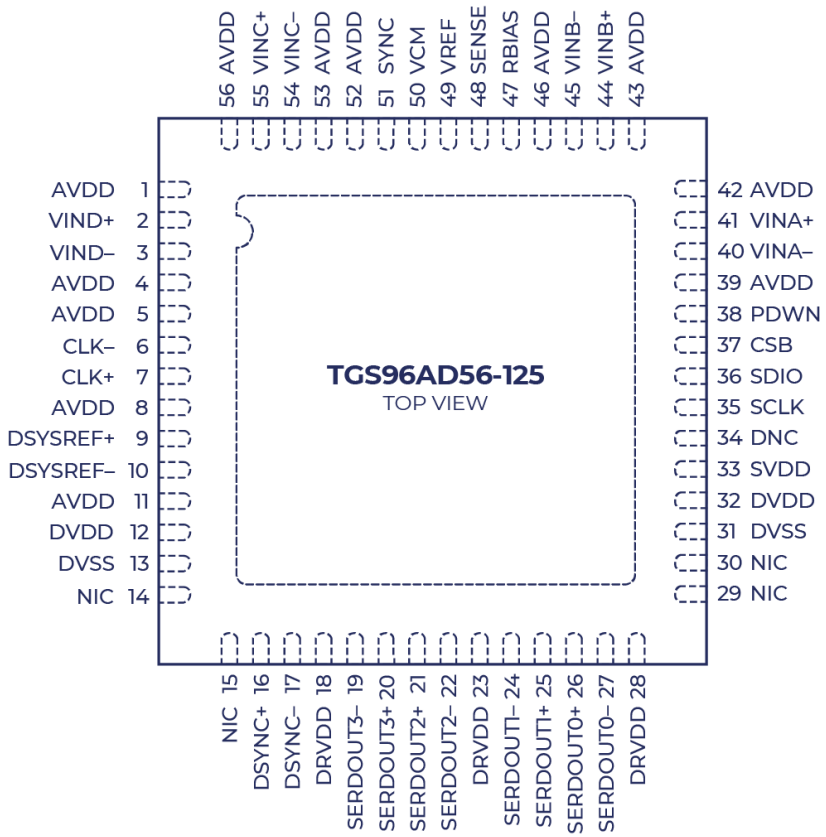

Figure 4. Pin Configuration (Top View)

The INL and DNL test curves are shown in Figure 3.
FFT plots with analog input frequency of 100 MHz at a sampling rate of 250 MSPS are shown in Figure 4.
FFT plots with analog input frequency of 170 MHz at a sampling rate of 250 MSPS are shown in Figure 5.
FFT plots with analog input frequency of 230 MHz at a sampling rate of 250 MSPS are shown in Figure 6.
FFT plots with analog input frequency of 300 MHz at a sampling rate of 250 MSPS are shown in Figure 7.
The bandwidth test is shown in Figure 8.

Table 10. Pin Function Description

Pin Number	Pin Name	Description
0	AGND, Exposed Pad	Analog ground. The exposed thermal pad on the bottom of the package provides analog ground for the device.
1, 4, 5, 8, 11, 39, 42, 43, 46, 52, 53, 56	AVDD	1.8 V analog power supply pin.
2	VIND+	ADC Channel D analog input (+).
3	VIND-	ADC Channel D analog input (-).
6, 7	CLK-, CLK+	Differential clock, PECL, LVDS, or 1.8 V CMOS input.
9	DSYSREF+	JESD204B LVDS SYSREF active low input (+).

10	DSYSREF-	JESD204B LVDS SYSREF active low input (-).
12, 32	DVDD	Digital power supply pin.
13, 31	DVSS	Digital ground pin.
14, 15, 29, 30	NIC	Internal no connect. Can be grounded if needed.
16	DSYNC+	JESD204B LVDS SYNC active low input (+).
17	DSYNC-	JESD204B LVDS SYNC active low input (-).
18, 23, 28	DRVDD	Digital output driver power supply pin.
19	SEROUT3-	Lane 3 digital output (-).
20	SEROUT3+	Lane 3 digital output (+).
21	SEROUT2+	Lane 2 digital output (+).
22	SEROUT2-	Lane 2 digital output (-).
24	SEROUT1-	Lane 1 digital output (-).
25	SEROUT1+	Lane 1 digital output (+).
26	SEROUT0+	Lane 0 digital output (+).
27	SEROUT0-	Lane 0 digital output (-).
33	SVDD	SPI power supply pin.
34	DNC	No connect. Do not connect to this pin.
35	SCLK	SPI clock input.
36	SDIO	SPI data input and output.
37	CSB	SPI chip select, active low enable, internal 30 kΩ pull-up resistor.
38	PDWN	Digital input: high = power-down; low = normal operation.
40	VINA-	ADC Channel A analog input (-).
41	VINA+	ADC Channel A analog input (+).
44	VINB+	ADC Channel B analog input (+).
45	VINB-	ADC Channel B analog input (-).
47	RBIAS	Sets analog circuit bias. Connect this pin to ground with a 10 kΩ resistor.
48	SENSE	Reference voltage mode select.
49	VREF	Reference voltage input and output pin.
50	VCM	Analog input common-mode voltage.
51	SYNC	Digital input, synchronization input for the clock divider.
54	VINC-	ADC Channel C analog input (-).
55	VINC+	ADC Channel C analog input (+).

Typical performance parameters

V_{REF} = 1.4 V

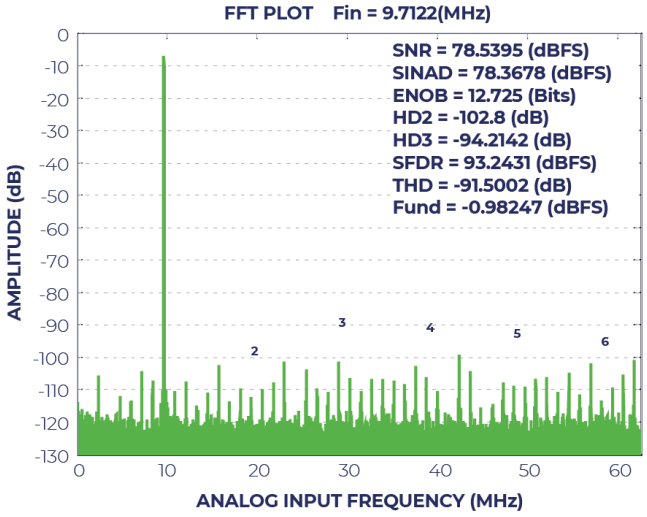

Figure 5. Single Tone 32K (f_{IN} = 9.7 MHz, f_S = 125 MSPS)

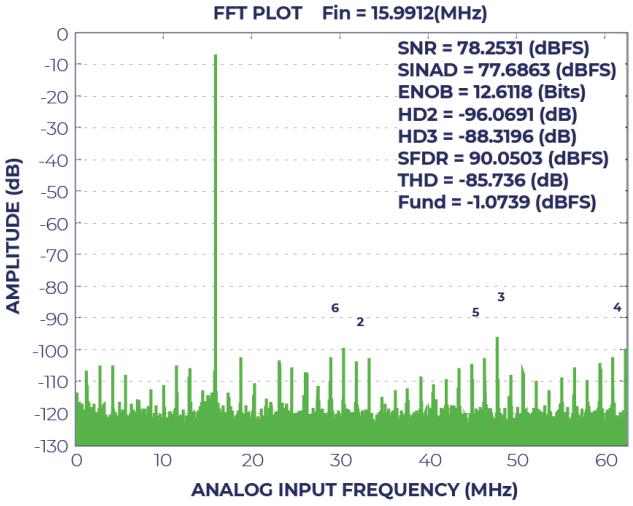

Figure 6. Single Tone 32K (fIN = 16 MHz, fS = 125 MSPS)

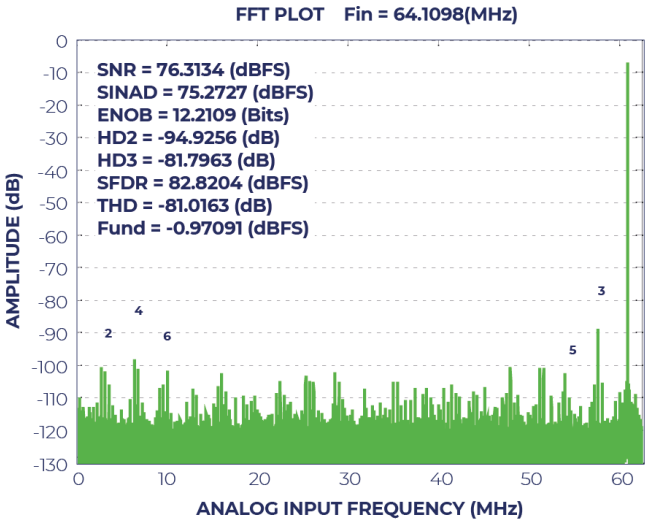

Figure 7. Single Tone 32K (fIN = 64 MHz, fS = 125 MSPS)

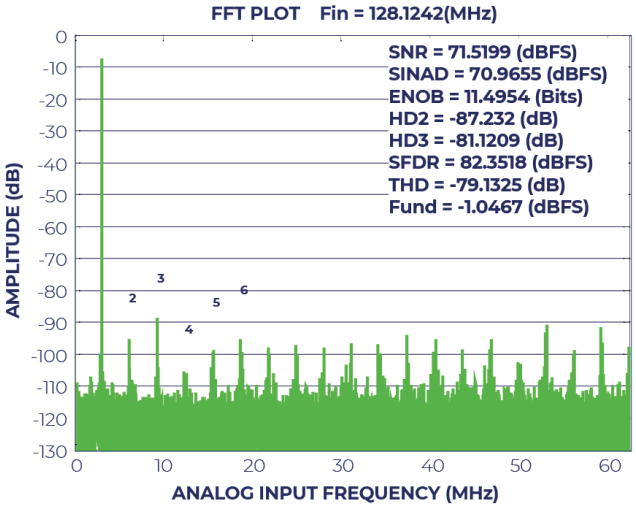

Figure 8. Single Tone 32K (fIN = 128 MHz, fS = 125 MSPS)

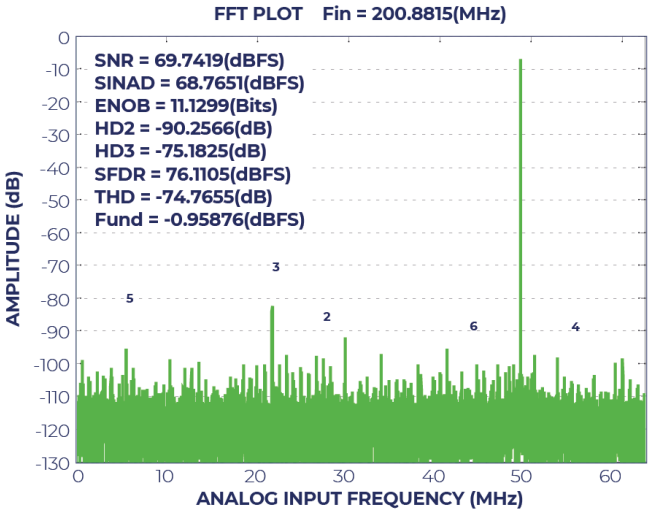

Figure 9. Single Tone 32K (fIN = 201 MHz, fS = 125 MSPS)

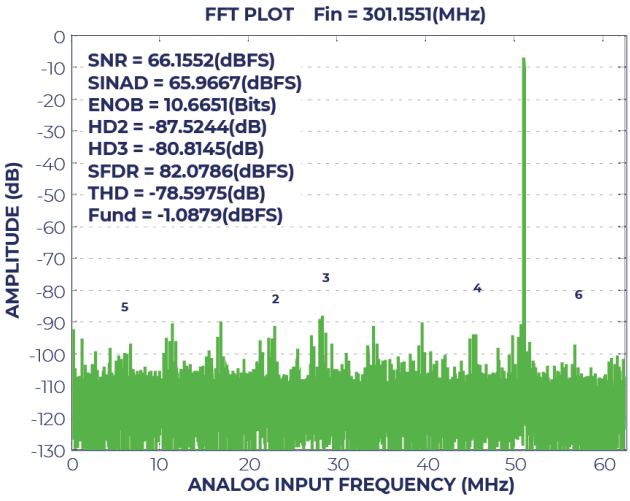

Figure 10. Single Tone 32K (fIN = 301 MHz, fS = 125 MSPS)

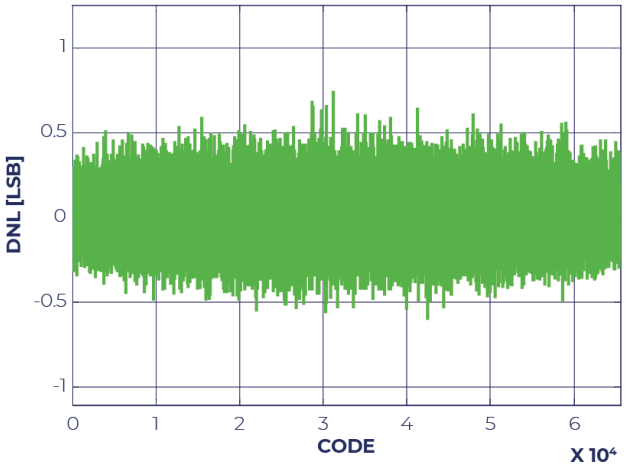

Figure 11. Differential Nonlinearity
(fIN = 9.7 MHz, fS = 125 MSPS)

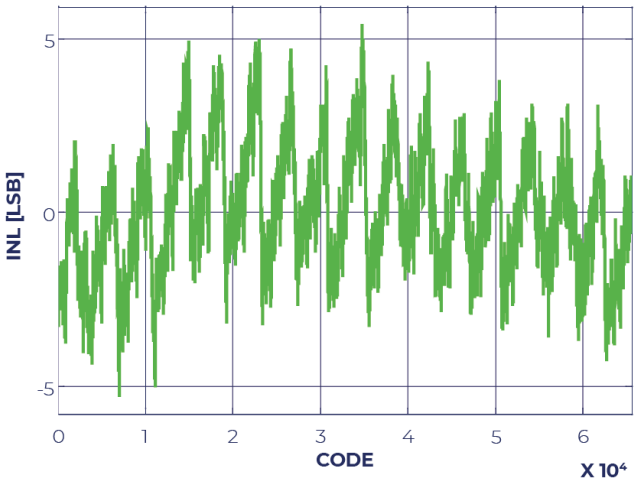

Figure 12. Integral Nonlinearity
(fIN = 9.7 MHz, fS = 125 MSPS)

V_{REF} = 1.0 V

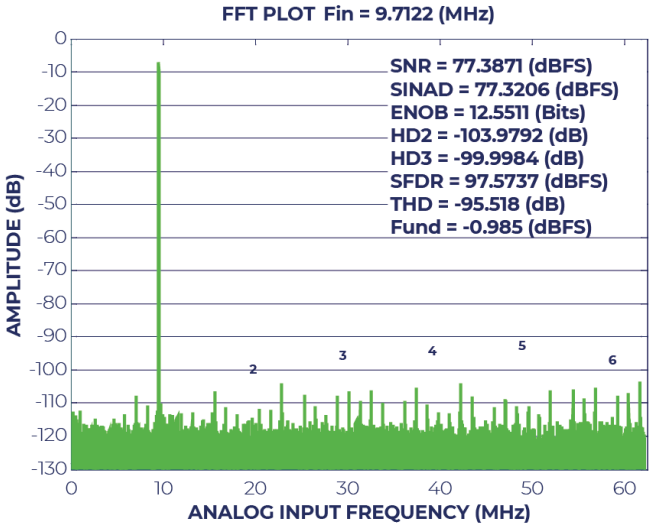

Figure 13. Single Tone 32K (fIN = 9.7 MHz, fS = 125 MSPS)

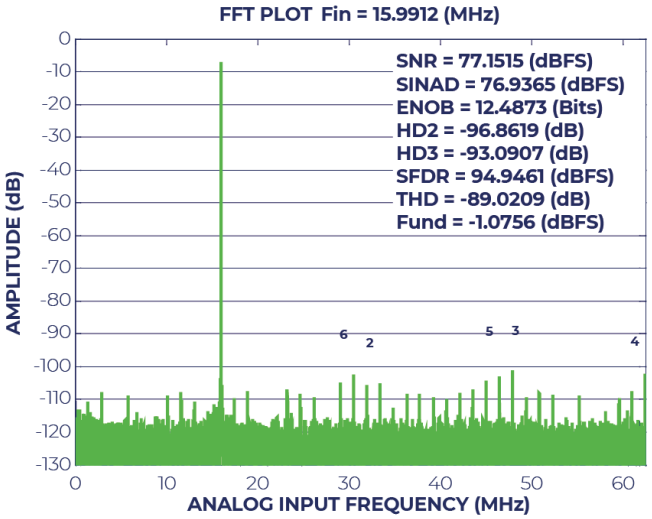

Figure 14. Single Tone 32K (fIN = 16 MHz, fS = 125 MSPS)

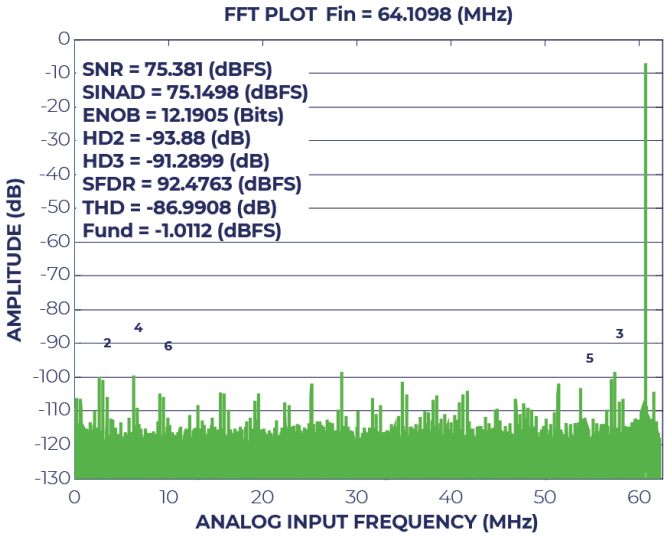

Figure 15. Single Tone 32K (f_{IN} = 64 MHz, f_S = 125 MSPS)

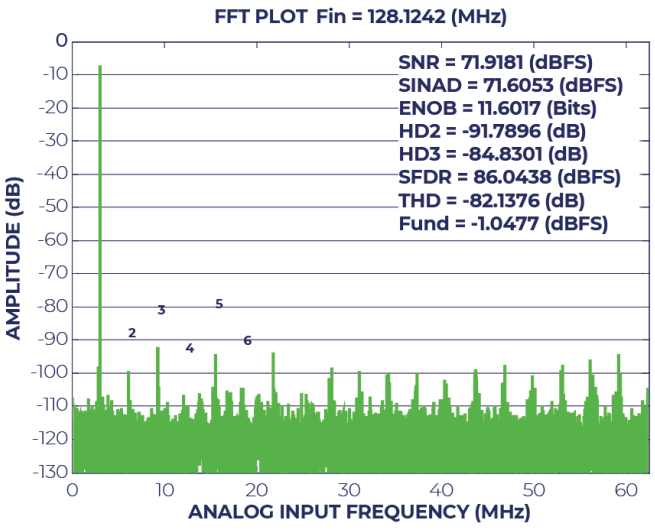

Figure 16. Single Tone 32K (f_{IN} = 128 MHz, f_S = 125 MSPS)

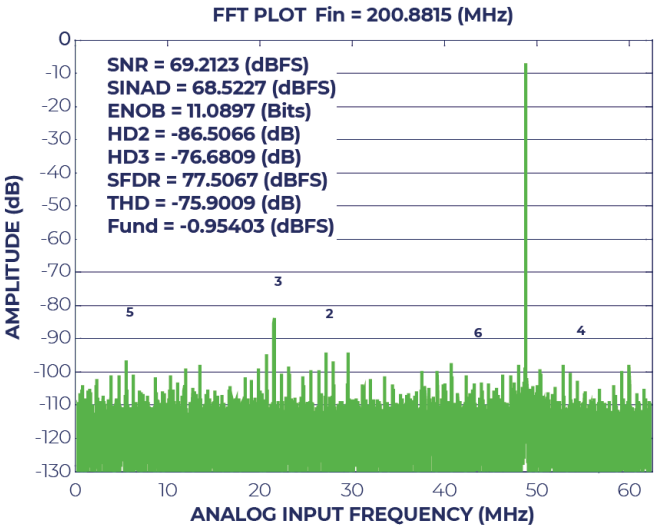

Figure 17. Single Tone 32K (fIN = 201 MHz, fS = 125 MSPS)

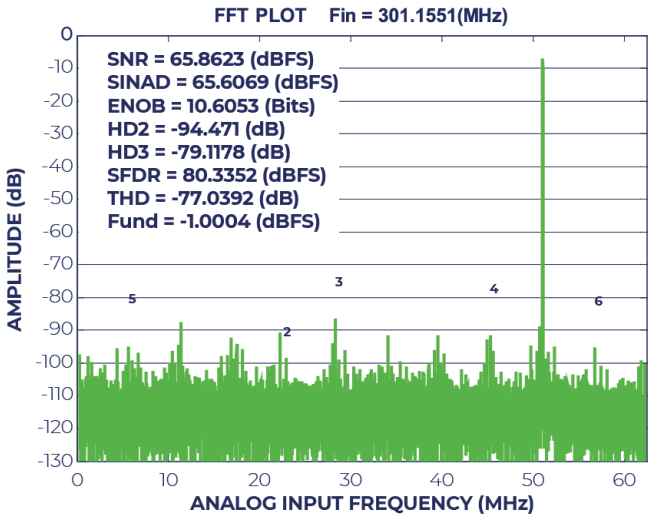

Figure 18. Single Tone 32K (fIN = 301 MHz, fS = 125 MSPS)

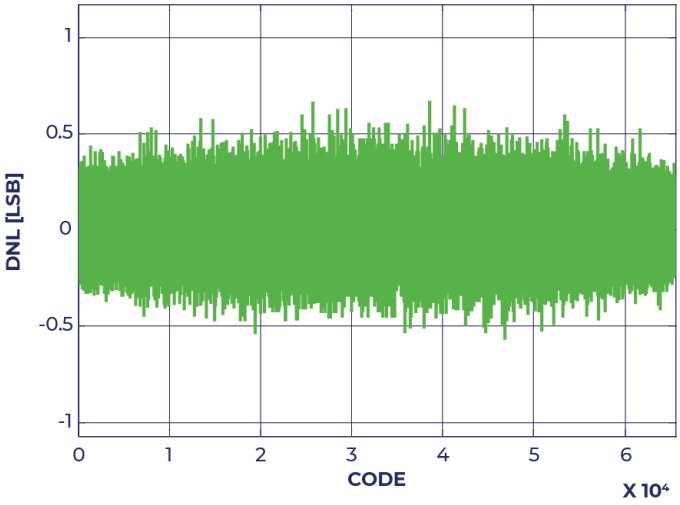

Figure 19. Differential Nonlinearity (f_{IN} = 10 MHz, f_S = 125 MSPS)

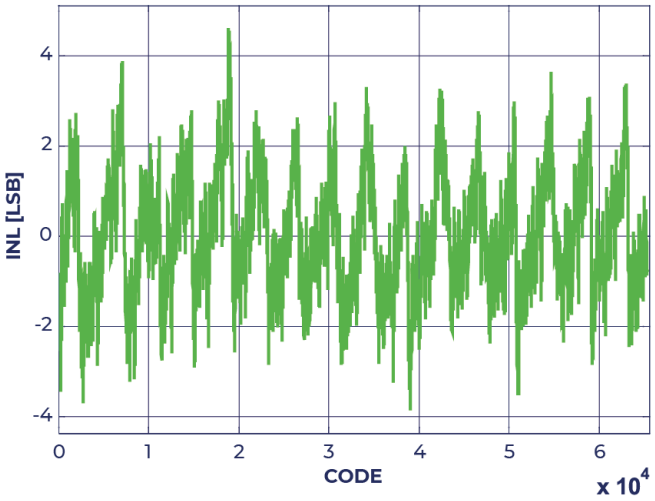

Figure 20. Integral Nonlinearity (f_{IN} = 10 MHz, f_S = 125 MSPS)

Equivalent Circuit

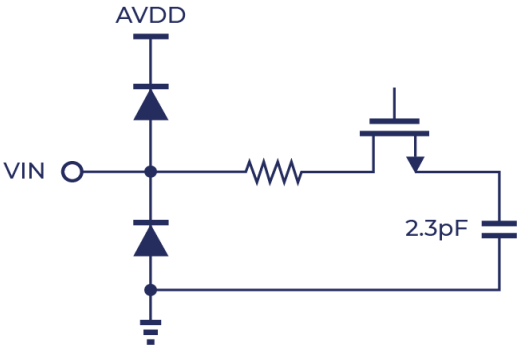

Figure 21. Equivalent Analog Input Circuit Diagram

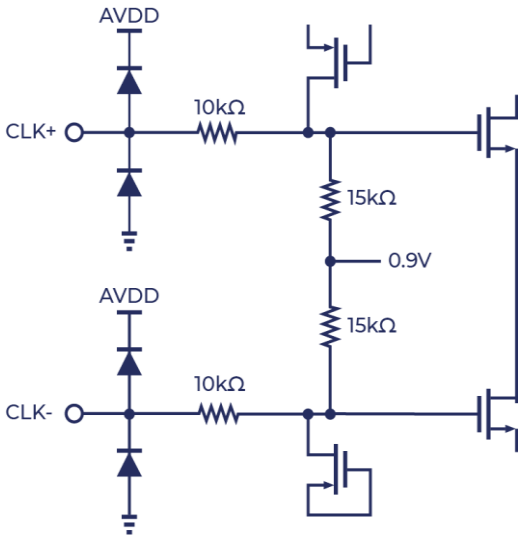

Figure 22. Equivalent Clock Input Circuit

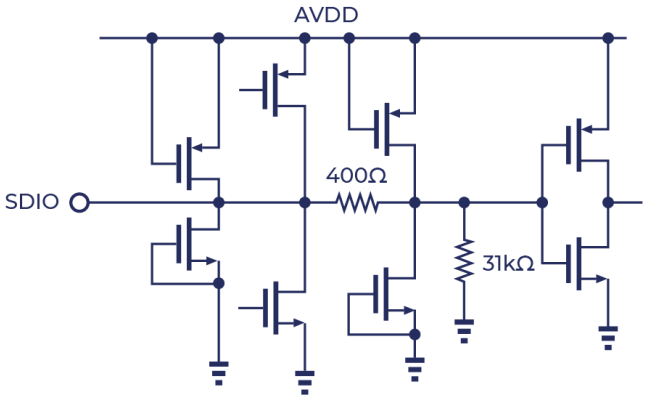

Figure 23. Equivalent SDIO Input Circuit Diagram

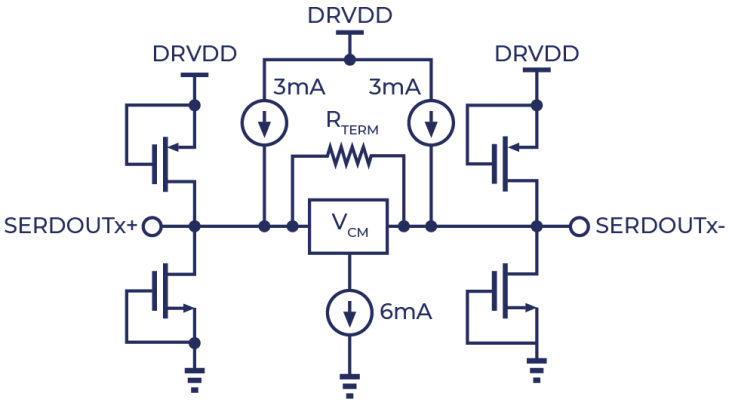

Figure 24. Equivalent SERDOUT± Circuit

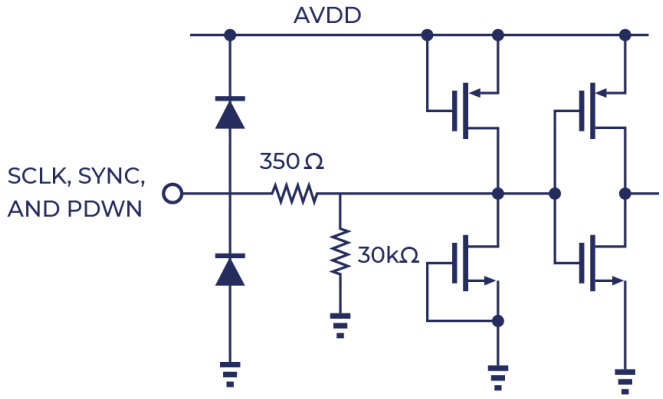

Figure 25. Equivalent SCLK, SYNC, PDWN Circuit

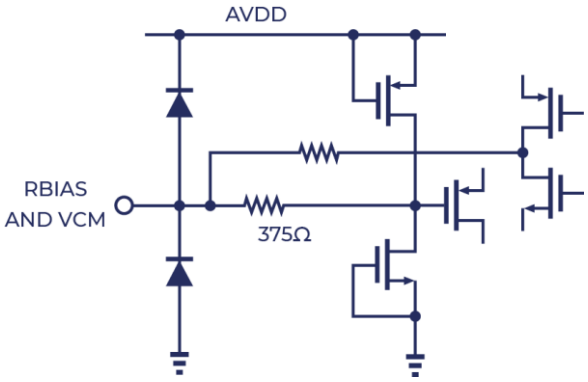

Figure 26. Equivalent RBIAS, VCM Circuit

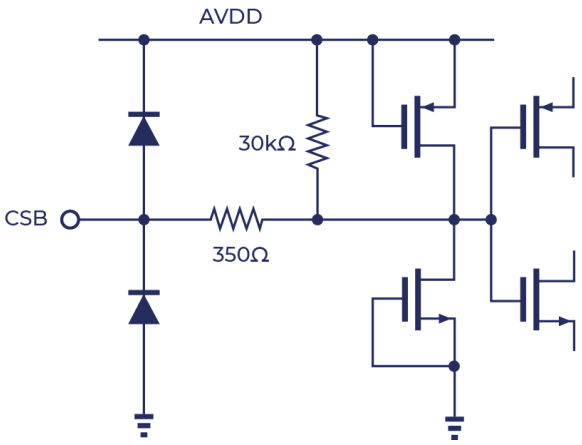

Figure 27. Equivalent CSB Input Circuit

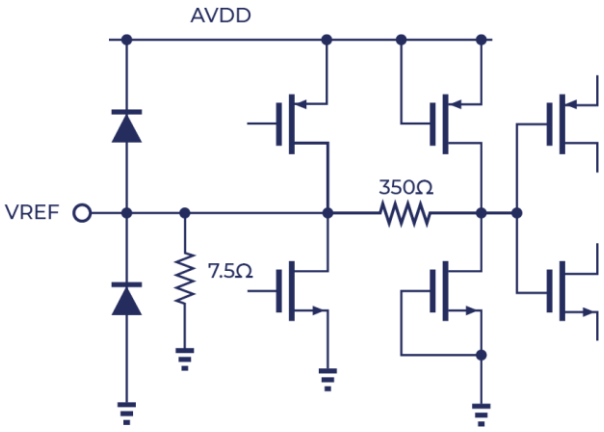

Figure 28. Equivalent VREF Circuit

Operating Principle

The product core uses a multi-stage, pipelined ADC architecture, with each stage providing one bit of redundancy to eliminate offset errors from the coarse quantizer comparators. The quantization results from each pipeline stage are reconstructed in the digital domain using a shift adder to form a 16-bit conversion result. A serializer sends this conversion result in a 16-bit output format.
Except for the final stage, each stage of the pipeline consists of a low-resolution Flash ADC, a switched-capacitor DAC connected to it, and an interstage residue amplifier (e.g., a multiplying digital-to-analog converter [MDAC]). The residue amplifier amplifies the difference between the reconstructed DAC output and the Flash input to provide it to the next stage of the pipeline. To assist in digital correction of Flash errors, each stage is provided with one bit of redundancy. The final stage consists only of a Flash ADC.

Analog Input

The analog input of this product is a differential switched-capacitor circuit designed to handle differential input signals. This circuit supports a wide common-mode range while maintaining excellent performance. Signal-dependent errors are minimized, and optimal performance is achieved, when the input common-mode voltage is at mid-supply.

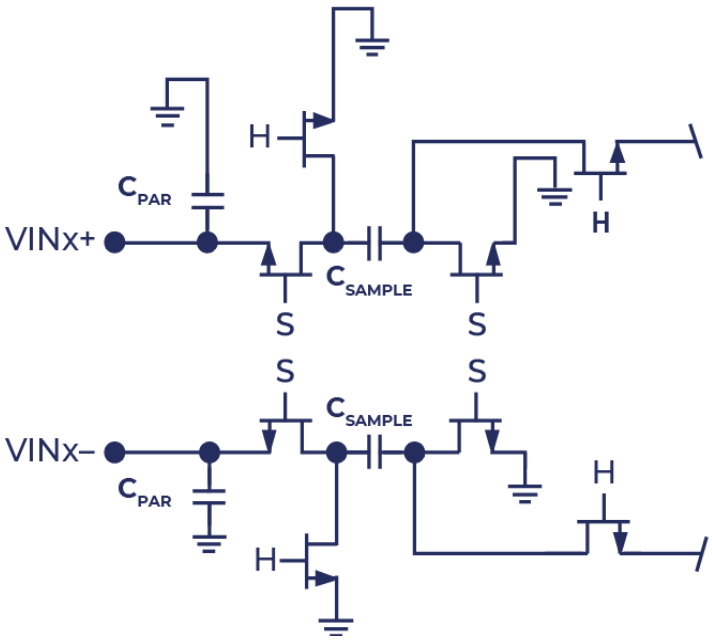

Figure 29. Switched-Capacitor Input Circuit

The input circuit switches between sampling mode and hold mode according to the clock signal (see Figure 29). When the input circuit switches to sampling mode, the signal source must be able to charge the sampling capacitor and settle within half a clock cycle. A small resistor is placed in series with each input to help reduce the peak transient current injected from the output stage of the driving source. In addition, a low-Q inductor or ferrite bead can be used on each side of the input to reduce the high differential capacitance at the analog input, thereby achieving maximum ADC bandwidth. When driving the converter front end at high intermediate frequencies (IF), low-Q inductors or ferrite beads must be used. A differential capacitor or two single-ended capacitors can be used at the input to provide a matched passive network. This ultimately forms a low-pass filter at the input to limit unwanted wideband noise.

Input Common-Mode Level

The analog input of this product has no internal DC bias. In AC-coupled applications, the user must provide external biasing. For optimal dynamic performance, the user must configure the device so that the input common-mode level is VCM = AVDD/2. This device can also achieve reasonable performance over a wider input common-mode range, as shown in Figure 30 and Figure 31.

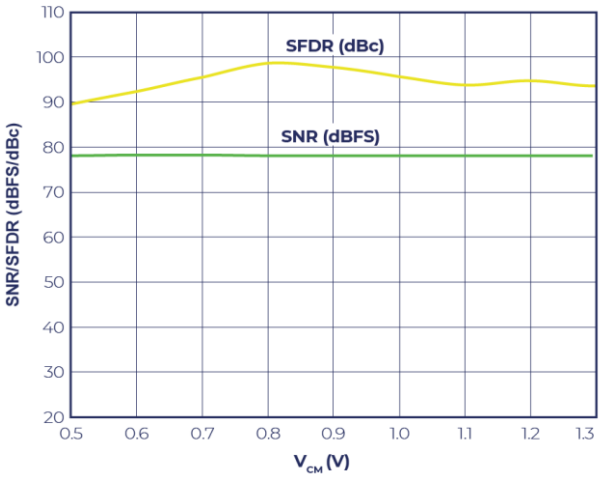

Figure 30. SNR/SFDR vs. Input Common-Mode Level (VCM) (f_{IN} = 9.7 MHz, f_{SAMPLE} =125 MSPS, V_{REF} = 1.0 V)

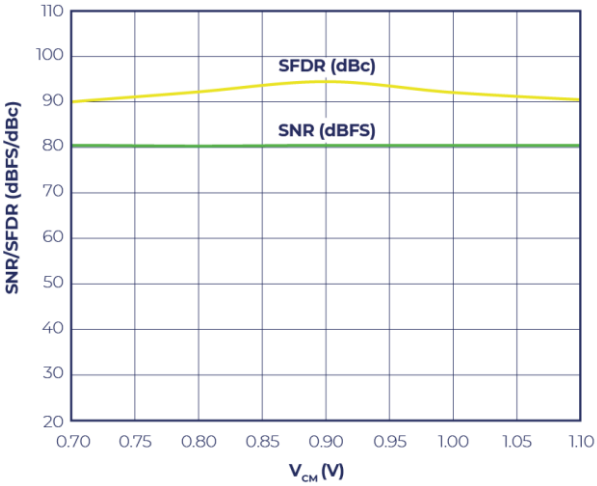

Figure 31. SNR/SFDR vs. Input Common-Mode Level (VCM) (f_{IN} = 9.7 MHz, f_{SAMPLE} =125 MSPS, V_{REF} = 1.4 V)

This product provides an on-chip reference voltage through the VCM pin. A 0.1 µF capacitor must be used to bypass the VCM pin to ground.
In a differential configuration, setting the device input to the maximum range achieves the highest signal-to-noise ratio (SNR) performance. For this product, the input range depends on the reference voltage, and performance degrades sharply if the input range is exceeded.

Differential Input Configuration

There are various active and passive methods to effectively drive this product. Driving it differentially suppresses even-order harmonics, thereby achieving optimal performance.

In baseband applications, using a differential balun configuration to drive this product provides excellent performance and a flexible interface for the ADC (see Figure 32). In applications where SNR is a critical parameter, because the noise performance of most amplifiers is insufficient to meet the true performance of this product, the input configuration requires differential transformer coupling (see Figure 33).

In the two applications above, the value of capacitor C needs to be matched to the input frequency spectrum. It is recommended to reduce or remove this capacitor when converting high-frequency analog input signals.

Driving this product in a single-ended input configuration is not recommended.

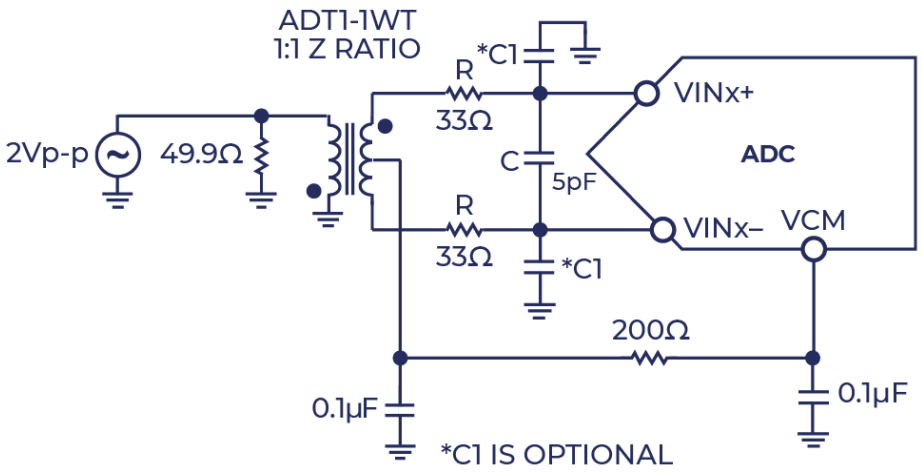

Figure 32. Differential Dual-Balun Configuration

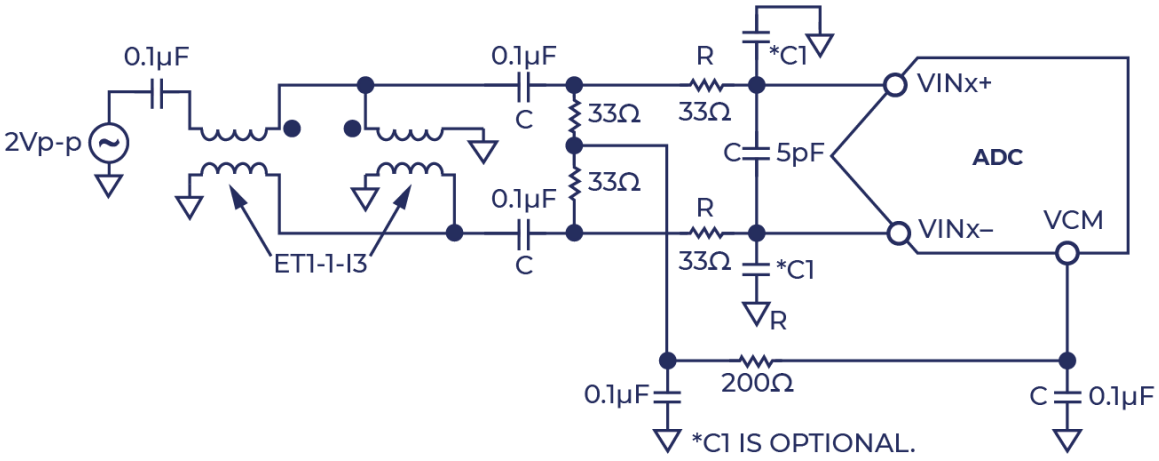

Figure 33. Differential Transformer Coupling

Reference Voltage

This product features a stable and accurate internal reference voltage source. VREF can be configured using the internal 1.0 V reference voltage, an externally applied 1.0 V to 1.4 V reference voltage, or an external resistor divider acting on the internal reference voltage, allowing the user to select the reference voltage. For a description of the reference voltage source modes, refer to the "Internal Reference Voltage Connection" section and the "External Reference Voltage" section. The VREF pin should be bypassed to ground externally with a parallel combination of a low equivalent series resistance (ESR) 1.0µF capacitor and a low ESR 0.1 µF ceramic capacitor.

The built-in comparator of this product detects the voltage at the SENSE pin, allowing the reference voltage to be configured into one of three possible modes. If the SENSE pin is grounded, the reference voltage amplifier switch is connected to the internal resistor divider (see Figure 34), setting the VREF pin voltage to 1.0 V. If the SENSE pin is connected to an external resistor divider (see Figure 35), VREF is defined as:

$$Vref = 0.5 \times (1 + R2/R1)$$

where, $7\ k\Omega \leq (R1 + R2) \leq 10\ k\Omega$

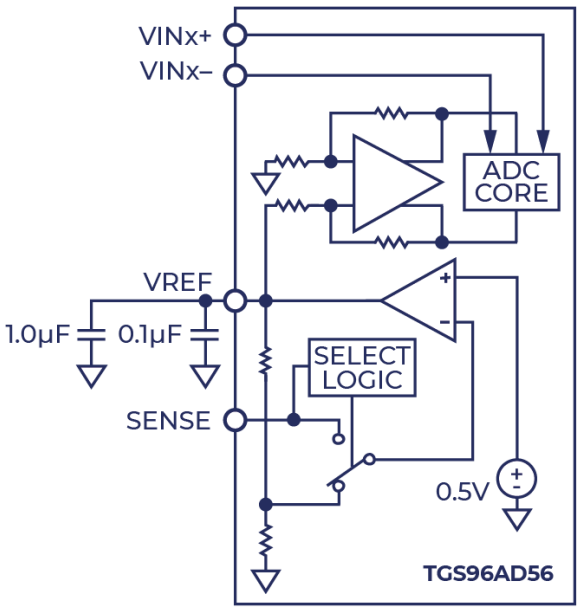

Figure 34. Reference Voltage Configuration 1

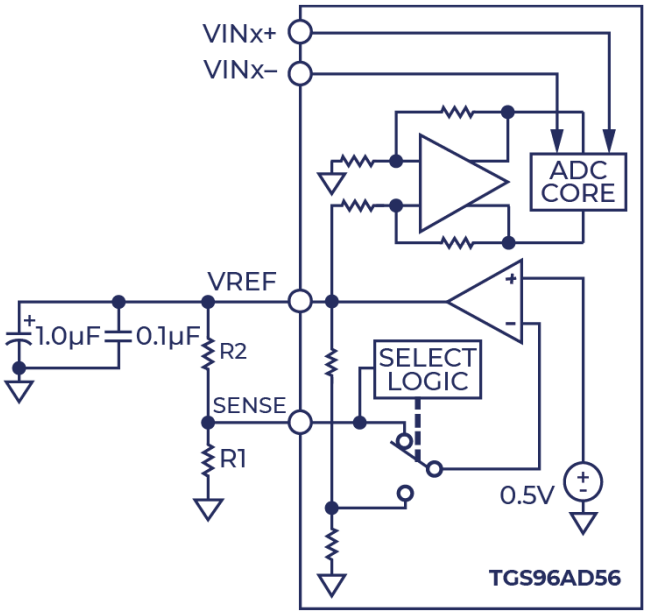

Figure 35. Reference Voltage Configuration 2

If the internal reference voltage of this product is used to drive multiple converters to improve gain matching, the load placed on the reference voltage by the other converters must be taken into account. Figure 36 and Figure 37 show how the load affects the internal reference voltage.

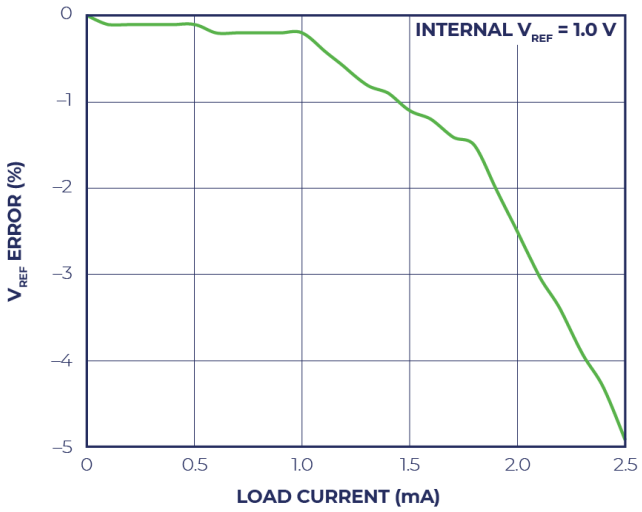

Figure 36. VREF Error (Internal VREF = 1.0 V) vs. Load Current

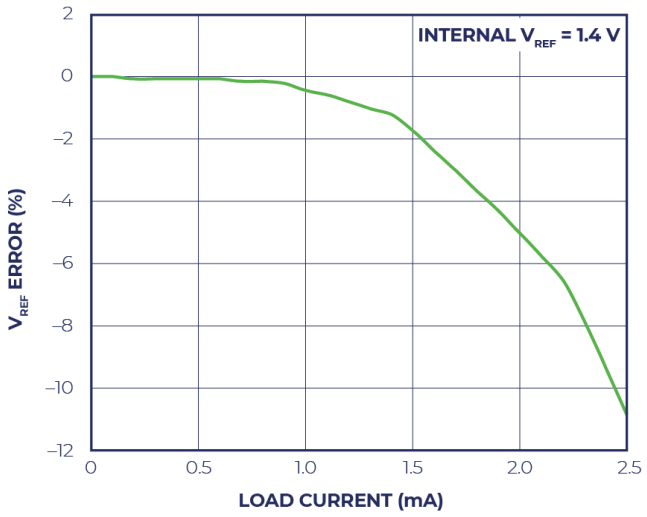

Figure 37. VREF Error (Internal VREF = 1.4 V) vs. Load Current

External Reference Voltage

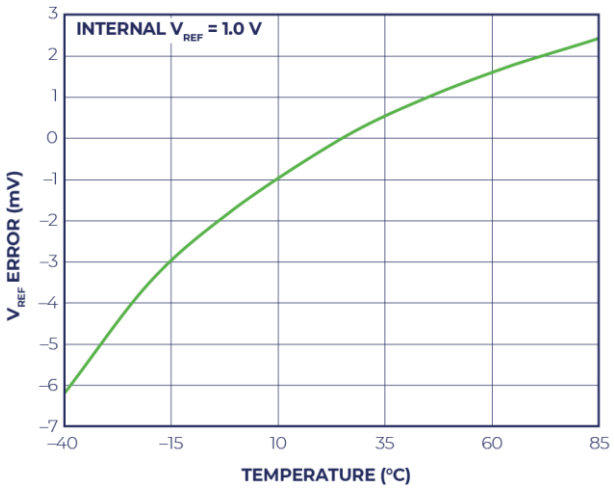

Figure 38. VREF Error vs. Temperature
(VREF = 1.0 V Typical Drift)

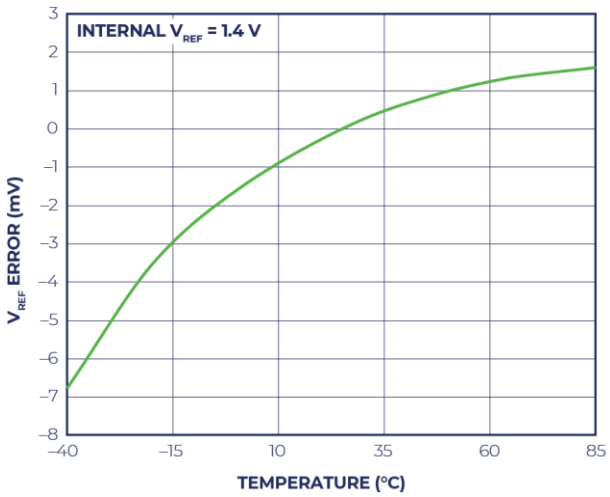

Figure 39. VREF Error vs. Temperature
(VREF = 1.0 V Typical Drift)

External reference voltage must be used to further improve ADC gain accuracy and thermal drift characteristics. Figure 38 and Figure 39 show the typical drift characteristics of the internal reference voltage source in 1.0 V mode and 1.4 V mode, respectively. Connecting the SENSE pin to AVDD disables the internal reference voltage source, allowing the use of an external reference voltage source. The internal reference voltage buffer presents a load equivalent to 7.5 kΩ to the external reference voltage source. The internal buffer generates the positive and negative full-scale reference voltages for the ADC core. Leaving the SENSE pin floating is not recommended.

Clock Input Considerations

To achieve the full performance of the chip, a differential signal should be used as the clock signal for the product's sampling clock inputs (CLK+ and CLK−). This signal is typically AC-coupled into the CLK+ and CLK− pins using a transformer or capacitors. These two pins are internally biased and require no external biasing.

Clock Input Options

This product features a flexible clock input structure. CMOS, LVDS, LVPECL, or sine wave signals can all be used as its clock input signal. Regardless of which signal is used, the clock source jitter must be taken into consideration (see the Jitter Considerations section). Figure 10 and Figure 11 show two preferred methods for providing the clock signal to this product (the clock rate before internal clock division can reach up to 1 GHz).
A low-jitter clock source's single-ended signal can be converted to a differential signal using an RF transformer or RF balun. For clock frequencies from 125 MHz to 1GHz, an RF balun configuration is recommended; for clock frequencies from 40 MHz to 200 MHz, an RF transformer configuration is recommended. Schottky diodes connected across the secondary winding of the transformer/balun can limit the clock signal input to this product to approximately 0.8 Vp-p differential (see Figure 40 and Figure 41).
This not only prevents large voltage swings on the clock from feeding through to other parts of the product but also preserves the fast rise and fall times of the signal, which is very important for achieving low jitter performance.
However, at frequencies above 500 MHz, the diode capacitance can have an effect. Care must be taken to select appropriate signal limiting diodes.

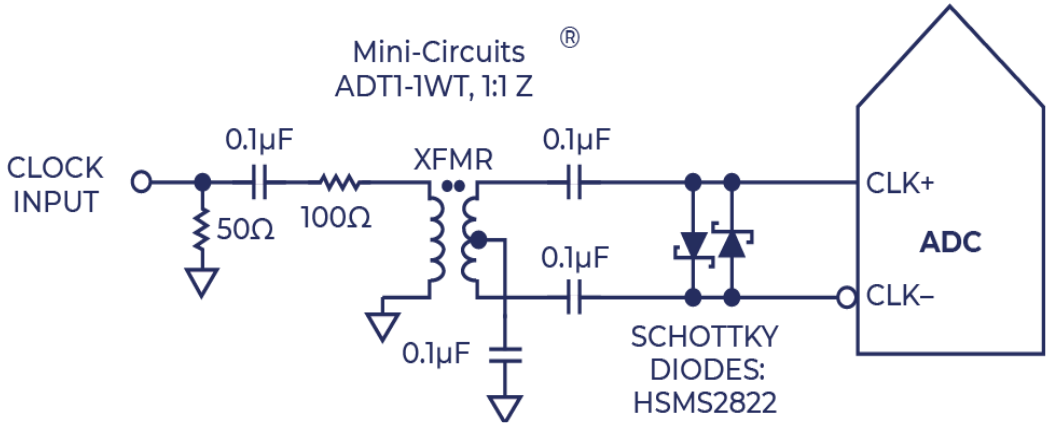

Figure 40. Transformer-Coupled Differential Clock (Frequency up to 200 MHz)

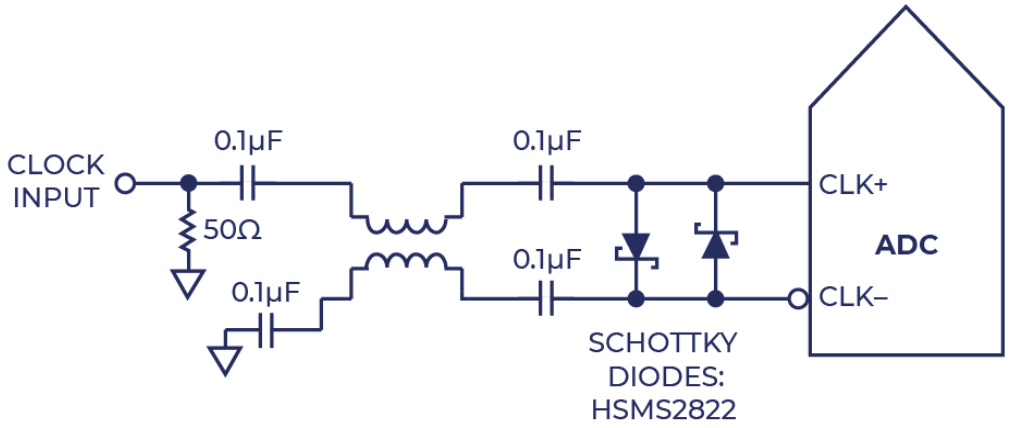

Figure 41. Balun-Coupled Differential Clock (Frequency up to 1 GHz)

If a low-jitter clock source is not available, an alternative method is to AC-couple a differential PECL signal and transmit it to the sampling clock input pins (as shown in Figure 42).
The AD9510/ AD9511/ AD9512/ AD9513/ AD9514/ AD9515/ AD9516/ AD9517 clock drivers offer excellent jitter performance.

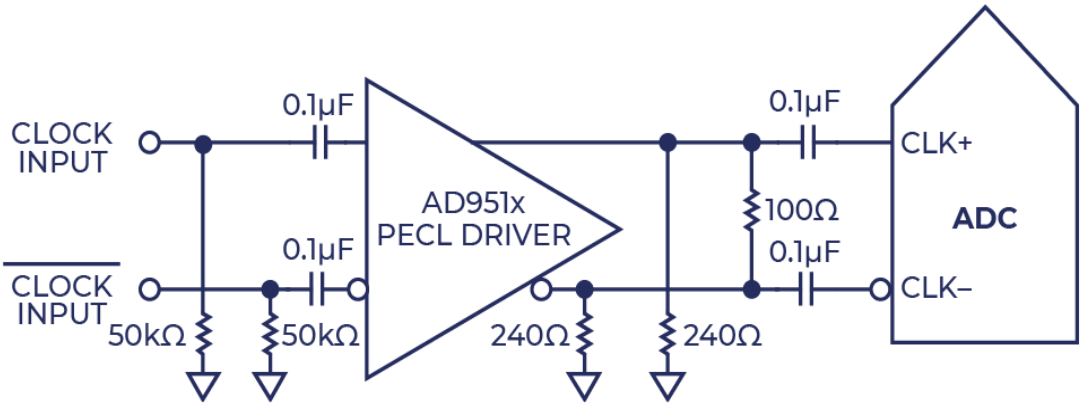

Figure 42. Differential PECL Sampling Clock (Frequency up to 1 GHz)

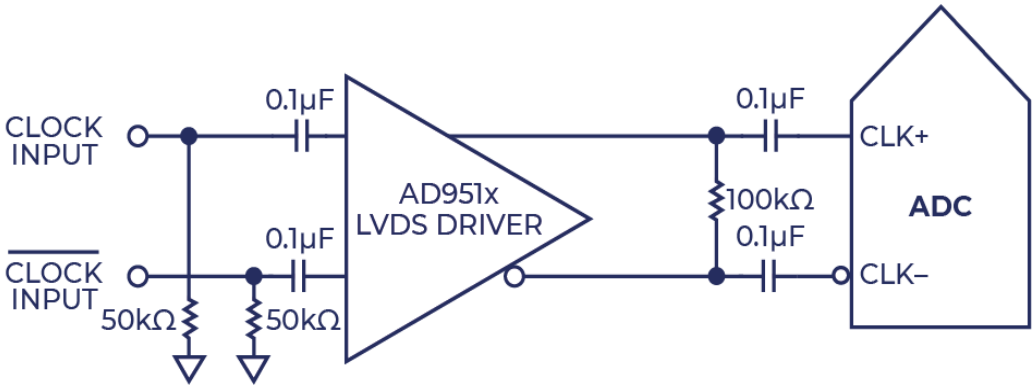

Figure 43. Single-Ended 1.8 V CMOS Input Clock (Frequency up to 200 MHz)

Input Clock Divider

This product features an internal input clock divider that can divide the input clock by integer factors from 1 to 8. The product's clock divider can be synchronized using an external SYNC input signal. By writing to bits 0 and 1 of Register 0x109, the clock divider can be configured to resynchronize either each time a SYNC signal is received or only the first time a SYNC signal is received. An active SYNC resets the divider to its initial state. This synchronization feature allows the clock dividers of multiple devices to be aligned, thereby ensuring simultaneous input sampling.

Clock Duty Cycle

Typical high-speed ADCs generate different internal timing signals using both clock edges and are therefore very sensitive to clock duty cycle. Generally, to maintain ADC dynamic performance, the clock duty cycle tolerance should be ±5%.
This product features an internal duty cycle stabilizer (DCS) that retimes the non-sampling edge (falling edge) and provides an internal clock signal with a nominal 50% duty cycle. This feature minimizes performance degradation when the clock input duty cycle deviates from the nominal 50% duty cycle by more than ±5%. Enabling the DCS function significantly improves noise and distortion performance for clock input duty cycles between 30% to 45% and 55% to 70%.
Jitter on the input rising edge remains a concern and cannot be easily reduced by the internal stabilization circuit. In applications where the clock rate changes dynamically, the time constant associated with this loop must be considered. A period of 1.5 µs to 5 µs is required for the DCS loop to relock to the input signal.

Jitter Considerations

High-speed, high-resolution ADCs are very sensitive to the quality of the clock input signal. IF under sampling applications are particularly sensitive to jitter (see Figure 44). When aperture jitter can affect the dynamic range of this product, the clock input signal should be treated as an analog signal. Separate the clock driver power supply from the ADC output driver power supply to prevent digital noise from contaminating the clock signal. A low-jitter, crystal-controlled oscillator provides the best clock source. If the clock signal is derived from other types of clock sources (through gating, division, or other methods), it should be retimed using the original clock in the final step.

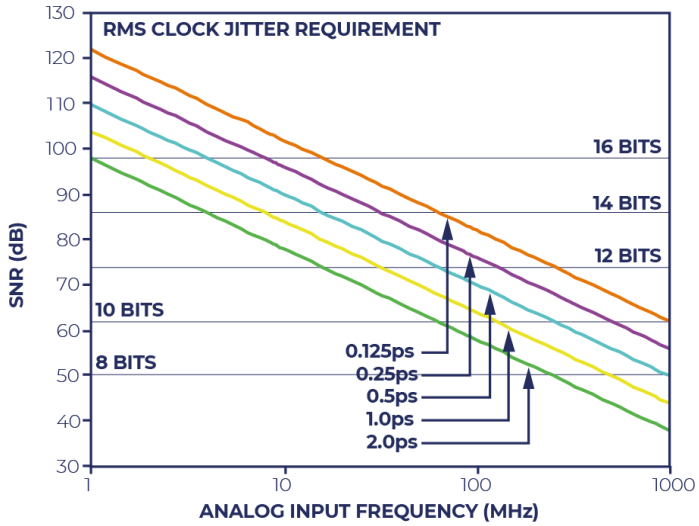

Figure 44. Ideal SNR vs. Analog Input Frequency and Jitter

Power Dissipation and Power-Down Modes

As shown in Figure 45 and Figure 46, the power dissipation of this product is proportional to its sampling rate. The product can be put into power-down mode through the SPI port or by asserting the PDWN pin high. In power-down mode, the typical power dissipation of the ADC is 14 mW. In power-down mode, the output drivers are in a high-impedance state. When the PDWN pin is asserted low, the product returns to normal operation mode. Note that PDWN is referenced to the data output driver power supply voltage (DRVDD) and must not exceed this supply voltage.

In power-down mode, low power dissipation is achieved by turning off the reference voltage source, reference voltage buffer, bias network, and clock. When entering power-down mode, internal capacitors are discharged; when returning to normal operation mode, these internal capacitors must be recharged. Therefore, the wake-up time is related to the time spent in power-down mode; the shorter the time in power-down mode, the shorter the corresponding wake-up time. When using the SPI port interface, the user can place the ADC in either power-down mode or standby mode. For a shorter wake-up time, standby mode can be used, in which the internal reference voltage circuit remains powered on. For more information on using these features, see the "Memory Map" section.

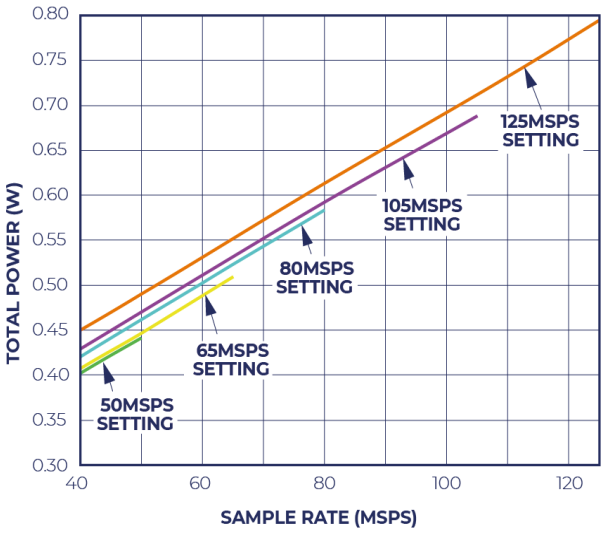

Figure 45. Total Power Dissipation vs. f_{SAMPLE} (f_{IN} = 9.7 MHz, 4 Channels, V_{REF} = 1.4 V)

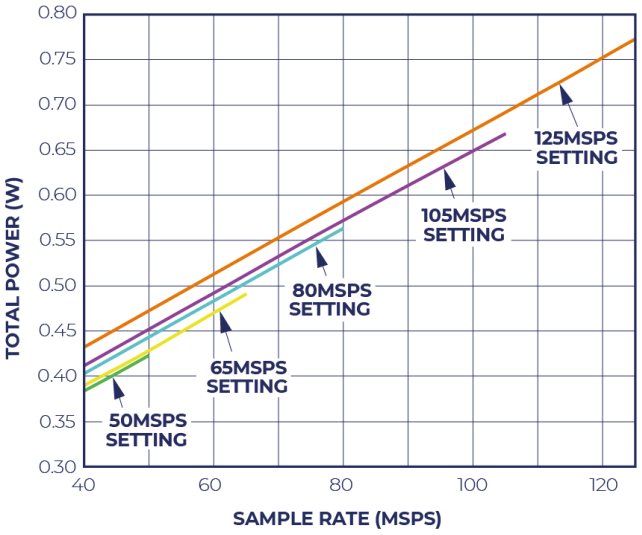

Figure 46. Total Power Dissipation vs. f_{SAMPLE} (f_{IN} = 9.7 MHz, 4 Channels, V_{REF} = 1.0 V)

Digital Output

JESD204B Transmitter Top-Level Description

The digital output of this product uses the JEDEC standard (Standard No. JESD204B, Serial Interface for Data Converters). JESD204B is the protocol for this product to connect to digital processing devices through a serial interface (up to 6.4 Gbps link speed). The advantages of the JESD204B interface include less board space required for data interface routing and smaller packages for converters and logic devices. This product supports 1-lane, 2-lane, and 4-lane interfaces.

JESD204B Overview

The JESD204B data transmission module (JTX) combines parallel data from the ADCs into data frames and outputs serial data using 8b/10b encoding and optional data scrambling. During the initial link establishment, special characters are used to support lane synchronization; additional synchronization is achieved in the subsequent data stream. An external receiver must be matched to lock onto the serial data stream and recover the data and clock. For more information on the JESD204B interface, refer to the JESD204B standard.
The JESD204B transmitter module of this product maps the outputs of the four ADCs onto the link. The link can be configured to use single, dual, or quad serial differential outputs, referred to as lanes. The JESD204B specification uses multiple parameters to define the link, and these parameters must match between the JESD204B transmitter (the output of this product) and the receiver.

JESD204B Link Parameters:

- S = Number of samples per converter per frame cycle (value for this product is 1)
- M = Number of converters per device (value for this product is 4)
- L = Number of lanes per device (value for this product is 1, 2, or 4)
- N = Converter resolution (value for this product is 16)
- N' = Total number of bits per sample (value for this product is 16)
- CF = Number of control words per frame clock cycle per converter (value for this product is 0)
- CS = Number of control bits per conversion sample (value for this product is 0)
- K = Number of frames per multiframe (configurable on this product)
- HD = High density mode (value for this product is 0)
- F = Number of 8-bit words per frame (value for this product is 2, 4, or 8, depending on the corresponding L value of 4, 2, or 1 respectively)
- C = Control bits (over-range, overflow, underflow; not provided in default mode of this product)
- T = Tail bits (not provided in default mode of this product)
- SCR = Scrambler enable/disable (configurable on this product)
- FCHK = Checksum of JESD204B parameters (automatically calculated and stored in the register map)

Figure 57 shows a simplified block diagram of the JESD204B link of this product. The default configuration of this product uses four converters and one lane. This product supports other configurations, such as combining the outputs of two or four converters into a single lane, allowing data from four converters to be output through two lanes. The mapping of the 0, 1, 2, and 3 digital output paths can be changed. These modes can be configured through the fast configuration registers in the SPI register map, and additional customization options are provided.
By default, the 16-bit word of each converter in this product is split into two 8-bit words (data bits are 8 bits). The first 8-bit word includes bits 0 (MSB) through 7, and the second 8-bit word includes bits 8 through 15 (LSB)

The generated two 8-bit words can be scrambled. Scrambling is optional; this option avoids spectral spikes when transmitting similar digital data patterns. The scrambler uses a self-synchronous, polynomial-based algorithm defined by the equation 1+x14+x15. The descrambler in the receiver must also use a self-synchronous version of the scrambler polynomial.
The two 8-bit words are then encoded through an 8b/10b encoder. The 8b/10b encoder encodes 8 data bits (one 8-bit word) into a 10-bit symbol. Figure 58 shows how the 16-bit data is output from the ADC, how the two 8-bit words are scrambled, and how the 8-bit words are encoded into two 10-bit symbols. Figure 58 shows the default data format.
At the data link layer, in addition to 8b/10b encoding, character substitution is used to allow the receiver to monitor frame alignment. Character substitution occurs at frame and multiframe boundaries, and its implementation depends on which boundary the process occurs on and whether scrambling is enabled.
If scrambling is disabled, the following measures are taken. If the last scrambled 8-bit word of the last frame in a multiframe equals the last 8-bit word of the previous frame, the transmitter replaces that last 8-bit word with the control character /A/ = /K28.3/. For other frames in the multiframe, if the last 8-bit word within the frame equals the last 8-bit word of the previous frame, the transmitter replaces that last 8-bit word with the control character /F/ = /K28.7/.
If scrambling is enabled, the following measures are taken. If the last 8-bit word of the last frame in a multiframe equals 0x7C, the transmitter replaces that last 8-bit word with the control character /A/ = /K28.3/. For other frames in the multiframe, if the last 8-bit word equals 0xFC, the transmitter replaces that last 8-bit word with the control character /F/ = /K28.7/.
For more information on the JESD204B interface, refer to the JEDEC standard (Standard No. JESD204B, July 2011). Section 5.1 includes details on the transport layer and data format; Section 5.2 includes details on scrambling and descrambling.

JESD204B Synchronization Details

This product is a JESD204B Subclass 1 device and achieves link synchronization using two control signals (SYSREF and DSYNC). At the system level, multiple converter devices are aligned using a common DSYSREF and device clock (CLK).
The synchronization process is completed in three stages: Code Group Synchronization (CGS), Initial Lane Alignment Sequence (ILAS), and Data Transmission. If scrambling is enabled, data bits are not actually scrambled until after the data transmission phase; scrambling is not performed during the CGS and ILAS phases.

CGS Phase

During the CGS phase, the JESD204B transmitter module transmits /K28.5/ characters. The receiver (external logic device) must use Clock and Data Recovery (CDR) techniques to find the K28.5 character in the incoming data stream.
Once a certain number of consecutive K28.5 characters are detected on the link lane, the receiver generates a DSYSREF edge signal to allow the transmitted data of this product to establish an internal Local Multiframe Clock (LMFC) signal.
The DSYSREF edge can also reset any sampling edge of the ADC to synchronize the sampling instance with the LMFC. This is very important for maintaining synchronization between multiple devices. The receiver or logic device de-asserts the SYNC~ signal applied to DSYNC, and the transmitter module begins the ILAS phase.

ILAS Phase

During the ILAS phase, the transmitter sends known patterns, and the receiver aligns all lane links and verifies the link parameters.
After SYNC~ is de-asserted (becomes high), the ILAS phase begins. The transmitter module begins sending 4 multiframes. Dummy samples are inserted into the required characters to transmit complete multiframes. The 4 multiframes include:

- Multiframe 1: Starts with the /R/ character [K28.0] and ends with the /A/ character

- Multiframe 2: Starts with the /R/ character, followed by the /Q/ [K28.4] character, then 14 link configuration parameters consisting of 8-bit configuration words (see Table 12), and ends with the /A/ character.
- Multiframe 3: Same as Multiframe 1.
- Multiframe 4: Same as Multiframe 1.

Table 11. The 14 Configuration 8-Bit Words in the ILAS Phase

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0(LSB)
0	DID [7:0]							
1					BID [3:0]			
2				LID [4:0]				
3	SCR			L [4:0]				
4	F [7:0]							
5				K [4:0]				
6	M [7:0]							
7	CS [1:0]			N [4:0]				
8	SUBCLASS [2:0]			N’ [4:0]				
9	JESDV [2:0]			S [4:0]				
10				CF [4:0]				
11	Reserved, Don't Care (RES1)							
12	Reserved, Don't Care (RES2)							
13	FCHK [7:0]							

Data Transmission Phase

During the data transmission phase, frame alignment is monitored through control characters. Character substitution is performed at the end of a frame. Character substitution is performed on the transmitter when the following conditions occur:

- If scrambling is disabled, and the last 8-bit word of a frame or multiframe equals the 8-bit word of the previous frame.
- If scrambling is enabled, and the last 8-bit word of a multiframe equals 0x7C, or the last 8-bit word of a frame equals 0xFC.

Link Setup Parameters

The following shows how to configure the JESD204B interface of this product. The steps to configure the output include:

1. Disable the lane(s) before changing the configuration.
2. Select a fast configuration option.
3. Configure detailed options.
4. Check the checksum (FCHK) of the JESD204B interface parameters.
5. Set other digital output configuration options.

6. Re-enable the lane(s).

Disable the lane(s) before changing the configuration. Before changing the JESD204B link parameters, disable the link and keep it in the reset register. This can be done by writing a logic 1 to Register 0x5F (Bit 0).

Select a Fast Configuration Option

Write to Register 0x5E (JESD204B Fast Configuration Register) to select a configuration option. The configuration options and their corresponding JESD204B parameter values are shown in Table 12.

- 0x41 = 4 converters, 1 lane
- 0x42 = 4 converters, 2 lanes
- 0x44 = 4 converters, 4 lanes
- 0x21 = 2 converters, 1 lane
- 0x22 = 2 converters, 2 lanes
- 0x11 = 1 converter, 1 lane

Table 12. Fast Configuration

JESD204B Fast Configuration (Register 0x5E)	M (Number of Converters, Register 0x71, [7:0])	L (Number of Lanes, Register 0x6E, [4:0])	F (8-bit Words/ Frame, Register 0x6F, [7:0])	S (Samples/ADC / Frame, Register 0x74, [4:0])	HD (High Density Mode, Register 0x75, [7:0])
0x41	4	1	8	1	0
0x42	4	2	4	1	0
0x44	4	4	2	1	0
0x22	2	2	2	1	0
0x21	2	1	4	1	0
0x11	1	1	2	1	0

Configure Detailed Options

Configure tail bits and control bits.

- Since N' = 16 and N = 14 (non-default configuration), each sample has 2 data bits available for transmitting additional information over the JESD204B link. Either tail bits or control bits can be selected. The default uses tail bits with a value of 0b00.
- Tail bits are pseudo-data bits sent over the link to complete two 8-bit words; they do not convey any information about the input signal. Tail bits can be fixed zero (default) or a pseudo-random number (Register 0x5F, Bit 6).
- One or two control bits can be selected via bits [7:6] of Register 0x72 to replace the tail bits. The meaning of the control bits can be set via bits [7:5] of Register 0x14.
- Set lane identification values.
- JESD204B supports identifying devices and lanes with parameters. These parameters are transmitted

during the ILAS phase and can be accessed via internal registers.

- The three identification values are Device ID (DID), Bank ID (BID), and Lane ID (LID). DID and BID are device-specific identifiers and can therefore be used to identify the circuit.
- Set the number of frames per multiframe, K.
- According to the JESD204B specification, a multiframe is defined as a set of K consecutive frames, where K ranges from 1 to 32, and the number of 8-bit words is required to be between 17 and 1024. Register 0x70 (bits [4:0]) sets the K value to 32 by default. Note that the K value is the register value plus 1.
- The K value can be changed, but certain conditions must be met. Based on the setting in the JESD204B fast configuration, this product uses a fixed 8-bit word value for each frame [F]. K must also be a multiple of 4 and satisfy the following equation:
- $32 \geq K \geq \text{Ceil}(17/F)$
- The JESD204B specification also specifies that the number of 8-bit words per multiframe, i.e., (K × F), ranges from 17 to 1024. The F value is set to a fixed value through fast configuration to ensure this relationship holds true.

Table 13. JESD204B Configurable Identification Values

DID Value	Register, Bits	Value Range
LID (Lane 0)	0x66, [4:0]	0…31
LID (Lane1)	0x67, [4:0]	0…31
DID	0x64, [7:0]	0…255
BID	0x65, [3:0]	0…15

Scrambling, SCR

- Scrambling can be enabled or disabled via Bit 7 of Register 0x6E. Scrambling is enabled by default. According to the
- JESD204B protocol, scrambling is only effective after lane synchronization is completed.
- Select Lane Synchronization Options
- Most synchronization functions of the JESD204B interface are enabled by default to facilitate typical applications. In certain cases, these features can be disabled or changed in the following ways:
- Bits [3:2] of Register 0x5F enable the ILAS (Initial Lane Alignment Sequence), which is enabled by default. Additionally, to support certain specific interfaces (such as NMCDA-SL), the JESD204B interface can be programmed to disable the ILAS sequence or continuously repeat the ILAS sequence.
- Fixed JESD204B Interface Parameter Values
- This product has some fixed JESD204B interface parameter values, as follows:
- [N'] = 16: Number of bits per sample is 16 (Register 0x73, bits [4:0])
- [CF] = 0: Number of control words per frame clock cycle per converter is 0 (Register 0x75, bits [4:0])

- Verify Read-Only Values: Number of lanes per link (L), number of 8-bit words per frame (F), number of converters (M), and number of samples per converter per frame (S). This product calculates certain JESD204B parameter values based on other settings (particularly the options in the Fast Configuration Register). The following read-only values in the register map are used for verification.
- [L] = Number of lanes per link can be 1, 2, or 4; read this value from Register 0x6E (bits [4:0])
- [F] = Number of 8-bit words per frame can be 2, 4, or 8; read this value from Register 0x6F (bits [7:0])
- [HD] = High density mode is 0; read this value from Register 0x75 (bit 7)
- [M] = Number of converters per link is 4 by default, but can be 1, 2, or 4; read this value from Register 0x71 (bits [7:0])
- [S] = Number of samples per converter per frame is 1; read this value from address 0x74 (bits [4:0])

Check the Checksum (FCHK) of the JESD204B Interface Parameters

The JESD204B parameters can be verified through the checksum (FCHK) of the JESD204B interface parameters. Each link has its own corresponding FCHK value. The FCHK value is transmitted during the second multiframe of the ILAS and can be read via internal registers.
The checksum is the modulo 256 sum of the parameters listed in the "Number" column of Table 14. The checksum is calculated by summing the parameter fields before they are encapsulated into 8-bit words as shown in Table 14.
The FCHK for the lane configuration that outputs data from Lane 0 can be read from Register 0x78. Similarly, the FCHK for the lane configuration that outputs data from Lane 1 can be read from Register 0x79, the FCHK for Lane 2 from Register 0x7A, and the FCHK for Lane 3 from Register 0x7B.

Table 14. JESD204B Configuration Table for ILAS and Checksum Calculation

No.	Bit 7(MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0(LSB)
0	DID [7:0]							
1					BID [3:0]			
2				LID [4:0]				
3	SCR			L [4:0]				
4	F [7:0]							
5				K [4:0]				
6	M [7:0]							
7	CS [1:0]			N [4:0]				
8	SUBCLASS [2:0]			N’ [4:0]				
9	JESDV [2:0]			S [4:0]				
10				CF [4:0]				

Set Other Digital Output Configuration Options

Other data format controls include:

- Serial output data polarity inversion: Register 0x60, Bit 1
- ADC data format (offset binary or twos complement): Register 0x14, Bits [1:0]
- Options for interpreting signals on DSYSREF and DSYNC: Register 0x3A, Bits [4:3]
- Options for remapping converter (logical lane) and SERDOUTx± (physical lane) assignments: Register 0x82 and Register 0x83. Figure 57 shows a simplified functional block diagram.

Re-enable Lanes After Configuration

After changing the JESD204B link parameters, the link lanes should be enabled to begin synchronization. This can be done by writing a logic 0 to Register 0x5F (Bit 0).

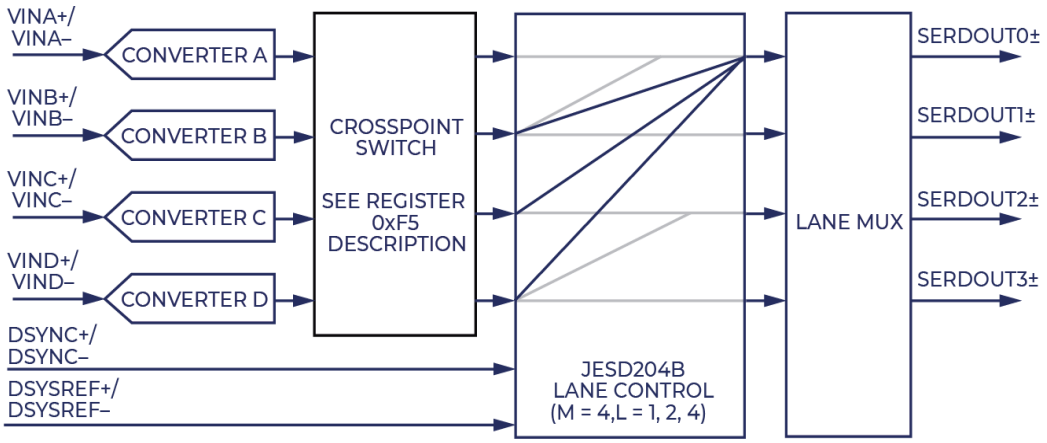

Figure 57. Simplified Functional Block Diagram of the Product's Transmission Link

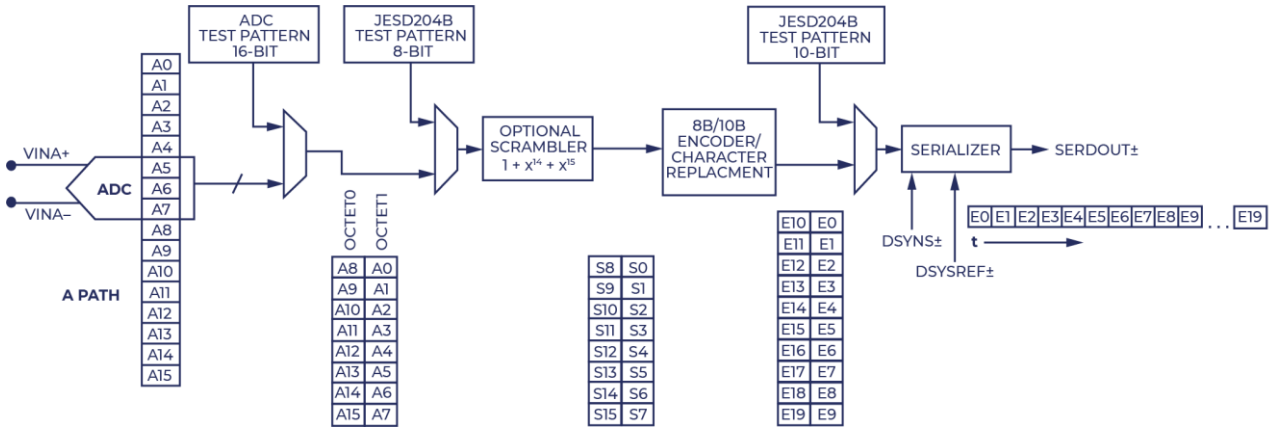

Figure 58. Digital Processing of the Product's JESD204B Lane

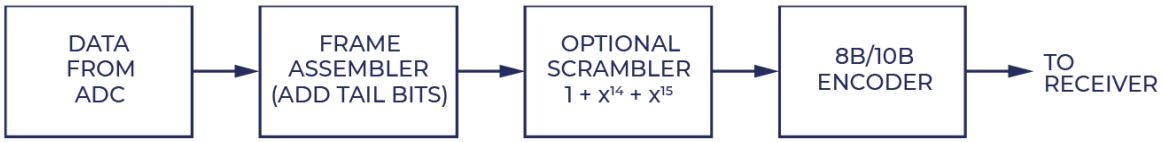

Figure 59. ADC Output Data Path of the Product

Frame and Lane Alignment Monitoring and Correction

Frame alignment monitoring and correction are both part of the JESD204B specification. A 16-bit word requires two 8-bit words to complete the transmission of all data. Two 8-bit words (MSB and LSB, F = 2) form a frame. Under normal operating conditions, frame alignment is monitored through alignment characters; characters can be inserted at the end of a frame when certain conditions are met. Table 16 summarizes the conditions under which character insertion can occur and the expected characters in various operating modes. If lane synchronization is enabled, the replacement character value depends on whether the 8-bit word is at the end of a single frame or at the end of a multiframe.
By correctly receiving the replacement characters, the receiver can ensure that it remains synchronized to the frame boundary under different operating modes.

Table 15. Frame and Lane Alignment Monitoring and Correction Replacement Character Table

Scrambling	Lane Synchronization	Character Requiring Replacement	Is it the last 8-bit character in a multiframe?	Replacement Character
Off	On	Last 8-bit word repeats the content of the previous frame	No	K28.7
Off	On	Last 8-bit word repeats the content of the previous frame	Yes	K28.3
Off	Off	Last 8-bit word repeats the content of the previous frame	(N/A)	K28.7
On	On	Last 8-bit word equals D28.7	No	K28.7
On	On	Last 8-bit word equals D28.3	Yes	K28.3
On	Off	Last 8-bit word equals D28.7	(N/A)	K28.7

Digital Output and Timing

When powering up this product, differential digital outputs are available by default. The driver current is sourced from the chip, and the output current of each output is set to a nominal value of 4 mA. Each output features a dynamic internal termination resistance of 100 Ω to reduce reflections.
Placing a 100 Ω differential termination resistor at the input of each receiver achieves a nominal receiver differential swing of 600 mVp-p (see Figure 60). Single-ended 50 Ω termination resistors can also be used. When using single-ended termination, the termination voltage must be DRVDD/2; alternatively, AC coupling capacitors can be used for termination to any single-ended voltage.

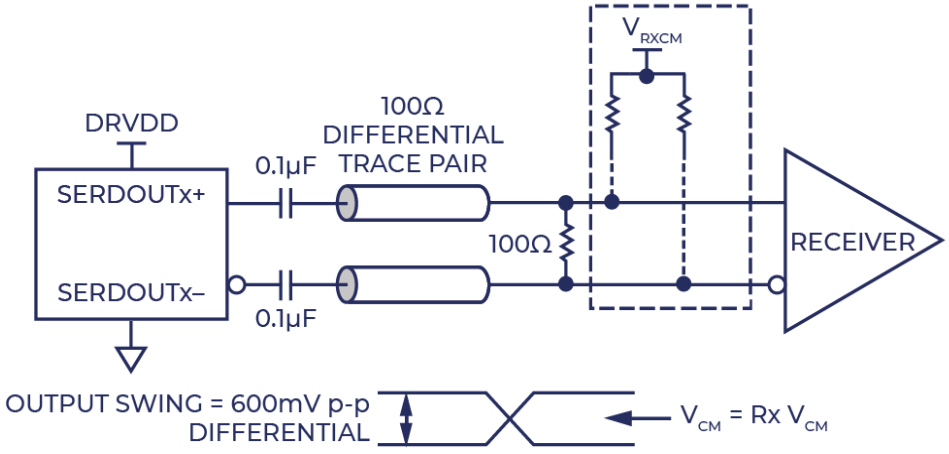

Figure 60. AC-Coupled Digital Output Termination Example

The digital output of this product can interface with custom ASIC and FPGA receivers, achieving excellent switching performance in high-noise environments. A single point-to-point network topology is recommended, with a single 100 Ω differential termination resistor placed as close as possible to the receiver. If a DC-coupled connection is used (as shown in Figure 61), the common-mode digital output automatically biases itself to the midpoint of the receiver's power supply (i.e., when the receiver supply is 1.8 V, the common-mode voltage is 0.9 V). For receivers whose logic levels are outside the DRVDD supply range, AC coupling is used. Place a 0.1 µF capacitor on each output pin and use a 100 Ω differential termination resistor near the receiver.

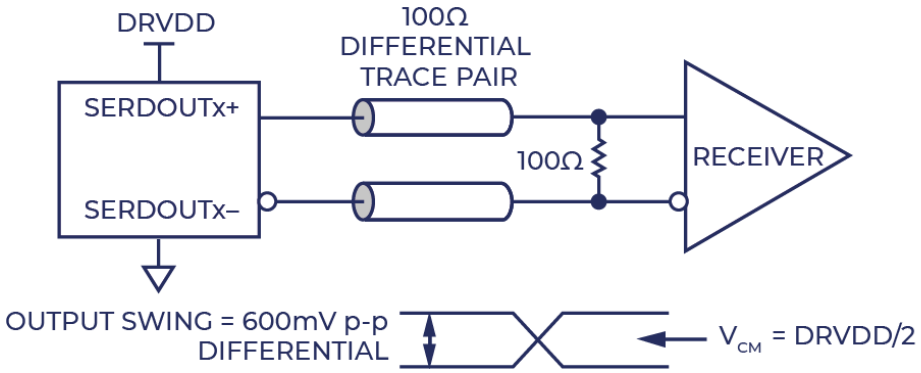

Figure 61. DC-Coupled Digital Output Termination Example

If there is no remote receiver termination resistor, or if the differential traces are not routed properly, timing errors may occur. To avoid timing errors, it is recommended that trace lengths not exceed 6 inches, and that the differential output traces be kept as close together and equal in length as possible.
Figure 62 shows an example of the digital output data eye diagram, Time Interval Error (TIE) jitter histogram, and bathtub curve when a lane of this product is operating at 6.4 Gbps. Additional SPI options allow the user to further increase the output driver voltage swing of all four outputs to drive longer traces. Using this option will increase power consumption from the DRVDD supply. For more information, see the Memory Map section.
The output data format defaults to twos complement. To change the output data format to offset binary, refer to the Memory Map section and Register 0x14 in Table 16.

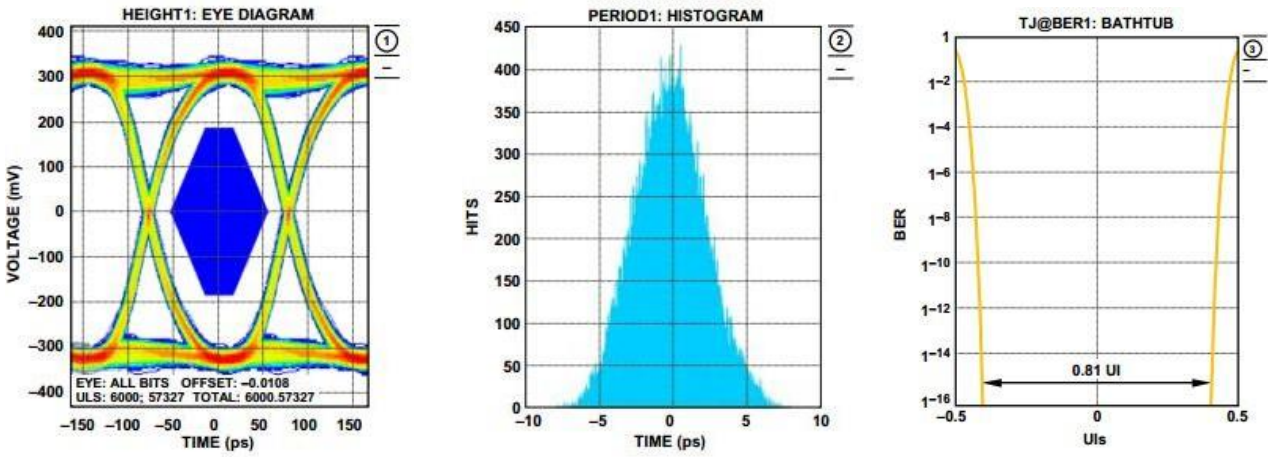

Figure 62. Product Digital Output Data Eye Diagram, Histogram, and Bathtub Curve
(External Termination Resistor = 100 Ω at 6.4 Gbps)

Frame and Lane Alignment Monitoring and Correction

Frame alignment monitoring and correction are both part of the JESD204B specification. A 16-bit word requires two 8-bit words to complete the transmission of all data. Two 8-bit words (MSB and LSB, F = 2) form a frame. Under normal operating conditions, frame alignment is monitored through alignment characters; characters can be inserted at the end of a frame when certain conditions are met. Table 16 summarizes the conditions under which character insertion can occur and the expected characters in various operating modes. If lane synchronization is enabled, the replacement character value depends on whether the 8-bit word is at the end of a single frame or at the end of a multiframe. By correctly receiving the replacement characters, the receiver can ensure that it remains synchronized to the frame boundary under different operating modes.

Memory Map

Reading the Memory Map Register Table

Each row in the Memory Map Register Table has 8 bits. The memory map is roughly divided into three sections: Chip Configuration Registers (Addresses 0x00 to 0x02), Channel Index and Transfer Registers (Addresses 0x05 and 0xFF), and ADC Function Registers, including setup, control, and test (Addresses 0x08 to 0x10A).
The Memory Map Register Table (see Table 16) lists each hexadecimal address and its hexadecimal default value. The Bit 7 (MSB) column indicates the starting bit of the given hexadecimal default value. For example, the Output Mode Register (Address 0x14) has a hexadecimal default value of 0x01. This indicates that Bit 0 = 1, while all other bits are 0. This setting is the default output format value (twos complement).

Disabled and Reserved Locations

This device does not support any addresses and bits not included in Table 16. Zeros should be written to unused bits in valid address locations. When only some bits at a given address (e.g., Address 0x18) are disabled, those locations can be written to. If an entire address (e.g., Address 0x13) is disabled, that address should not be written to.

Default Values

After the product is reset, the key registers are loaded with default values. The Memory Map Register Table (see Table 19) lists the default values for each register.

Logic Levels

The following terminology is used for logic levels:

- "Set" means "set a bit to logic 1" or "write a logic 1 to a bit."
- "Clear bit" means "set a bit to logic 0" or "write a logic 0 to a bit."

Channel-Specific Registers

Different values can be set for certain functions for each channel through programming. In these cases, the channel address locations are internally duplicated for each channel.

These registers and their corresponding bits are referred to as local registers in Table 16. Access to these local registers and their corresponding bits is achieved by setting the Channel 0, Channel 1, Channel 2, or Channel 3 bits of Register 0x05. If all four bits are set, subsequent write operations will affect the registers of all four channels. During a read cycle, only one channel should be set to perform a read operation on one of the four registers. If all bits are set during an SPI read cycle, the device returns the value from Channel 0. The global registers and their corresponding bits given in Table 16 affect the characteristics of the entire device and all channels, and do not allow each channel to be set individually. The settings in Register 0x05 do not affect the values of the global registers and their corresponding bits.

- **Memory Map Register Table**

This product uses a 3-wire interface and 16-bit addressing. Bits 0 and 7 of Register 0x00 are set to 0, and bits 3 and 4 are set to 1. When bit 5 of Register 0x00 is set to 1, the SPI enters soft reset, all user registers are restored to their default values, and bit 2 is automatically cleared to 0.

Table 16. Memory Map Registers (SPI registers/bits not marked as "Local" are "Global" registers/bits)

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments/ Remarks
Chip Configuration Register											
0x00	SPI Port Configuration	0	LSB First	Soft Reset	1	1	Soft Reset	LSB First	0	0x18	
0x01	Chip ID	8-bit Chip ID [7:0]; This product = 0xC0 (4-channel, 16-bit, 125 MSPS, JESD204B)								0xC0	Read Only
0x02	Chip Grade	Disable	Speed Grade ID [6:4]; 110 = 125 MSPS			Disable	Disable	Disable	Disable	0x60	Read Only
Channel Index and Transfer Register											
0x05	Device Index	Disable	Disable	Disable	Disable	Data Channel 3	Data Channel 2	Data Channel 1	Data Channel 0	0x0F	
0xFF	Transfer	Disable	Disable	Disable	Disable	Disable	Disable	Disable	Start Register 0x100 Override (Self-Clearing)	0x00	
ADC Function											
0x08	Power Mode	Disable	Disable	PDWN Pin Function: 0 = Full Power-Down 1 = Standby	JTX Standby Mode: 0 = Ignore Standby 1 = Do Not Ignore Standby	Reserved		Power Mode: 00 = Normal Operation 01 = Full Power-Down 10 = Standby 11 = Digital Reset		0x00	
0x09	Clock	Disable	0	Disable	Disable	Disable	Disable	Disable	Duty Cycle Stabilizer (DCS):	0x00	

									0 = Off 1 = On		
0x0A	PLL_STATUS	PLL Lock Status Bit: 0 = PLL Unlocked 1 = PLL Locked	Disable	Disable	Disable	Disable	Disable	Disable	JTX Link Status: 0 = Not Ready 1 = Ready		Read only
0x0B	Clock Divider	Disable	Disable	Disable	Disable	Disable	Clock Divide Ratio [2:0]: 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8			0x00	
0x0C	Enhanced Control	Disable	Disable	Disable	Disable	Disable	Chopper Mode: 0 = Off 1 = On	Disable	Disable	0x00	
0x0D	Test Mode (Local, except Pseudo-Random (PN) sequence reset)	User Input Test Mode: 00 = Single 01 = Toggle 10 = Single Once 11 = Toggle Once (Only affects User Input Test Mode Bits [3:0] = 1000)		Reset PN Long Sequence Generator	Reset PN Long Sequence Generator	Output Test Mode [3:0] (Local): 0000 = Off (default) 0001 = Midscale Short 0010 = Positive Full Scale (FS) 0011 = Negative FS 0100 = Toggle Checkerboard Pattern 0101 = PN23 Sequence 0110 = PN9 Sequence 0111 = 1/0 Word Inverted 1000 = User Input 1001 = 1/0 Bit Inverted 1010 = 1× Synchronous 1011 = 1-Bit High 1100 = Mixed Bit Frequency			0x00	When set to 1, test data will replace normal data and be placed on the output pins.

0x10	Offset Adjustment (Local)	8-bit Device Offset Adjustment [7:0] (Local); Offset adjustment is in LSBs, ranging from +127 to -128 (twos complement format)								0x00	Device Offset Adjustment
0x14	Output Mode	JTXCS Mode: 000 = {Over-range OR Under-range, Valid Flag} 001 = {Over-range, Under-range} 010 = {Over-range OR Under-range, Empty} 011 = {Empty, Valid Flag} 100 = {Empty, Empty} Others = {Over-range OR Under-range, Valid Flag}			ADC Output Valid Flag: 0 = Output Valid 1 = Output Invalid (Local)	Disable	Disable	Output Format: 0 = Offset Binary 1 = Twos Complement		0x01	
0x15	Output Adjustment	Disable	Disable	Disable	Disable	Disable	Typical CML Differential Output Drive Level: 000 = 473 mVp-p, 001 = 524 mVp-p, 010 = 574 mVp-p, 011 = 621 mVp-p (Default), 100 = 667 mVp-p, 101 = 716 mVp-p, 110 = 763 mVp-p, 111 = 811 mVp-p			0x03	
0x16	Clock Phase Control	Disable	Input Clock Phase Adjustment [2:0] (Value is the number of input clock cycles of phase delay)			Disable	Disable	Disable	Disable	0x00	
0x18	Input Range Select	Internal VREF Adjustment [1:0]: 00 = 1.0 V, 01 = 1.2 V, 10 = 1.3 V, 11 = 1.4 V		Disable	Disable	Disable	Differential Range Adjustment: 000 = 50% of Normal Value 001 = 57% of Normal Value 010 = 67% of Normal Value 011 = 80% of Normal Value 100 = Normal Value			0x04	

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments/ Remarks
0x19	User Test Code 1LSB	User Test Code 1 [7:0]								0x00	
0x1A	User Test Code 1MSB	User Test Code 1 [15:8]								0x00	
0x1B	User Test Code 2LSB	User Test Code 2 [7:0]								0x00	
0x1C	User Test Code 2MSB	User Test Code 2 [15:8]								0x00	
0x21	FLEX_SERIAL_ CONTROL	Disable	Disable	Disable	Disable	PLL Low Rate Mode: 0 = Lane Rate ≥ 2 Gbps 1 = Lane Rate < 2 Gbps	Disable	Disable	Disable	0x00	
0x22	FLEX_SERIAL_ CH_STAT	Disable	Disable	Disable	Disable	Disable	Disable	Disable	Channel Power-Down (Local)	0x00	
0x3A	SYSREF_CTRL	Disable	Disable	Disable	0 = Normal Mode 1 = Realign lane each time DSYNC± is activated	0 = Realign lane only when DSYSREF± causes counter resynchronization 1 = Realign lane on every DSYNC±	Disable	Disable	Disable	0x00	
0x3B	REALIGN_PATT ERN_CTRL	When aligning a lane, write this pattern code to the FIFO: 00 = Lane outputs all 0s 55 = Lane outputs alternating pattern code								0x55	
0x5E	JESD204B Fast Configuration	0x41 = 4 converters, 1 lane; 0x42 = 4 converters, 2 lanes; 0x44 = 4 converters, 4 lanes 0x22 = 2 converters, 2 lanes; 0x21 = 2 converters, 1 lane; 0x11 = 1 converter, 1 lane								0x00	Self-clearing, always reads back 0x00.
0x5F	JESD204B Link Control 1	Disable	End Bit Mode: 0 = Fill with 0	JTX Transport Layer Test: 0 = Not enabled	Multiframe Alignment Character Insertion: 0 = Disabled	ILAS Mode: 00 = ILAS disabled 01 = ILAS enabled (normal mode)		Frame Alignment Character Insertion: 0 = Enabled	JTX Link Control: 0 = JTX link enabled 1 = JTX link disabled	0x14	

			1 = Fill with 9-bit PN sequence	Enable, 1 = Long transport layer test enabled	1 = Enabled	11 = ILAS always on (test mode)		1 = Disabled			
0x60	JESD204BLink Control 2	Reserved		DSYNC± Pin Invert: 0 = No Invert 1 = Invert	DSYNC± Pin Input Bias: 0 = Disabled 1 = Enabled	Disable	Disable	JTX Output Invert: 0 = Normal 1 = Invert	Reserved	0x10	
0x61	JESD204BLink Control 3	Reserved	Reserved	Test Data Injection Point: 01 = Inject 10-bit data at 8b/10b encoder output 10 = Inject 8-bit data at scrambler input		JTX Test Mode Code: 0000 = Normal operation (test mode disabled) 0001 = Toggle checkerboard pattern 0010 = 1/0 word toggle 0011 = PN sequence = PN23 0100 = PN sequence = PN9 0101 = Continuous/repeat user test mode 0110 = Single user test mode 0111 = Reserved 1000 = Modified RPAT test sequence (8-bit data only) 1100 = PN sequence = PN7 1101 = PN sequence = PN15 Other settings are unused				0x00	
0x62	JESD204B Link Control 4	Reserved								0x00	
0x64	JESD204BDID Configuration	Device ID (DID) = C0								0xC0	Read only
0x65	JESD204BBID Configuration	Disable	Disable	Disable	Disable	JTX Bank ID (BID) Number				0x00	

0x66	JESD204BLID Configuration 0	Disable	Disable	Disable	JTX Lane ID (LID) Number for Lane 0	0x00	
0x67	JESD204BLID Configuration1	Disable	Disable	Disable	JTX Lane ID (LID) Number for Lane 1	0x01	
0x68	JESD204BLID Configuration2	Disable	Disable	Disable	JTX Lane ID (LID) Number for Lane 2	0x02	
0x69	JESD204BLID Configuration3	Disable	Disable	Disable	JTX Lane ID (LID) Number for Lane 3	0x03	
0x6E	JESD204B Parameter SCR/L	JESD204B Scrambling (SCR): 0 = Disabled 1 = Enabled	Disable	Disable	JESD204B Serial Lane Control: 0 = 1 lane per link (L=1) 1 = 2 lanes per link (L=2) 2 = Unused 3 = 4 lanes per link (L=4) 4 to 31 = Unused	0x80	
0x6F	JESD204B Parameter F	JESD204B Number of 8-bit Words per Frame (F); Calculated value, F = (2 × M) / L				0x00	Read only
0x70	JESD204B Parameter K	Disable	Disable	Disable	JESD204B Number of Frames per Multiframe (K); K = register value + 1, and K must be a multiple of 4 8-bit words	0x1F	
0x71	JESD204B Parameter M	JESD204B Number of Converters (M): 0 = 1 converter (M = 1), 1 = 2 converters (M = 2), 3 = 4 converters (M = 4, default value)				0x03	
0x72	JESD204B Parameter CS/N	00 = Send 0 control bits per sample (CS = 0)		Disable	JTX Converter Resolution (N): 0x0F = 16 bits 0x0D = 14 bits 0x0B = 12 bits 0x09 = 10 bits	0x0F	
0x73	JESD204B Parameter subclass/Np	JESD204B Subclass: 0x0 = Subclass 0 0x1 = Subclass 1 (default)			JESD204B Number of Bits per Sample (N'); N' = register value + 1	0x2F	
0x74	JESD204B Parameter S	Reserved			JESD204B Number of Converter Samples per Frame (S); S = register value + 1	0x20	Read only

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments/ Remarks
0x75	JESD204B Parameter HD and CF	JESD204BHD Value = 0	Disable	Disable	JESD204B Control Words Per Frame Clock Cycle Per Link (CF = 0, Fixed Value)					0x00	Read only
0x76	JESD204BRESV1	JESD204B Serial Reserved Field 1 in Link Configuration, see Table 12 (RES1)								0x00	
0x77	JESD204BRESV2	JESD204B Serial Reserved Field 2 in Link Configuration, see Table 12 (RES2)								0x00	
0x78	JESD204BCHKSUM0	JESD204B Serial Checksum Value in Link Configuration for Lane 0, see Table 12 (FCHK)									Read only
0x79	JESD204BCHKSUM1	JESD204B Serial Checksum Value in Link Configuration for Lane 1, see Table 12 (FCHK)									Read only
0x7A	JESD204BCHKSUM2	JESD204B Serial Checksum Value in Link Configuration for Lane 2, see Table 12 (FCHK)									Read only
0x7B	JESD204BCHKSUM3	JESD204B Serial Checksum Value in Link Configuration for Lane 3, see Table 12 (FCHK)									Read only
0x80	JTX Physical Lane Disable	Disable	Disable	Disable	Disable	Channel 3: 0 = Enabled 1 = Disabled	Channel 2: 0 = Enabled 1 = Disabled	Channel 1: 0 = Enabled 1 = Disabled	Channel 0: 0 = Enabled 1 = Disabled	x00	Channel serialized; output driver turned off.
0x82	JESD204B Lane Alignment 1	Disable	Physical Lane 1 Alignment: 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			Disable	Physical Lane 0 Alignment: 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			x10	
0x83	JESD204B Lane Alignment 2	Disable	Physical Lane 3 Alignment: 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			Disable	Physical Lane 2 Alignment: 000 = Logical Lane 0 001 = Logical Lane 1 010 = Logical Lane 2 011 = Logical Lane 3			x32	
0x86	JESD204B Lane Inversion	Disable	Disable	Disable	Disable	Channel 3: 0 = No Invert 1 = Invert	Channel 2: 0 = No Invert	Channel 1: 0 = No Invert 1 = Invert	Channel 0: 0 = No Invert 1 = Invert	x00	

							1 = Invert				
0x8B	JESD204BLMFC Offset	Disable	Disable	Disable	Local Multiframe Clock (LMFC) Phase Offset Value; Reset value of the LMFC phase counter when DSYSREF± is asserted; used for deterministic latency applications					0x00	
0xA0	JTX User Mode Code 8-bit Word 0, LSB	User Test Code Least Significant Byte, 8-bit Word 0								0x00	
0xA1	JTX User Mode Code 8-bit Word 0, MSB	User Test Code Least Significant Byte, 8-bit Word 0								0x00	
0xA2	JTX User Mode Code 8-bit Word 1, LSB	User Test Code Least Significant Byte, 8-bit Word 1								0x00	
0xA3	JTX User Mode Code 8-bit Word 1, MSB	User Test Code Least Significant Byte, 8-bit Word 1								0x00	
0xA4	JTX User Mode Code 8-bit Word 2, LSB	User Test Code Least Significant Byte, 8-bit Word 2								0x00	
0xA5	JTX User Mode Code 8-bit Word 2, MSB	User Test Code Least Significant Byte, 8-bit Word 2								0x00	
0xA6	JTX User Mode Code 8-bit Word 3, LSB	User Test Code Least Significant Byte, 8-bit Word 3								0x00	
0xF5	JTX Converter Mapping	JTX Converter 3: 0 = ADC A 1 = ADC B 2 = ADC C 3 = ADC D		JTX Converter 2: 0 = ADC A 1 = ADC B 2 = ADC C 3 = ADC D		JTX Converter 1: 0 = ADC A 1 = ADC B 2 = ADC C 3 = ADC D		JTX Converter 0: 0 = ADC A 1 = ADC B 2 = ADC C 3 = ADC D		xE4	
0x100	Resolution/ Sample Rate Override	Disable	Override Enable	Resolution: 0 =16 bit 1 =14 bit 2 =12 bit 3 =10 bit	Disable	Sample Rate: 001=40 MSPS, 010=50 MSPS, 011=65 MSPS, 100=80 MSPS, 101=105 MSPS, 110=125 MSPS				x00	Sample Rate Override (Transfer Register 0xFF required)

0x101	User I/O Control 2	Disable	Disable	Disable	Disable	Disable	Disable	Disable	SDIO Pull-Down	x00	Disable SDIO Pull-Down Resistor
0x102	User I/O Control 3	Disable	Disable	Disable	Disable	VCM Power-Down	Disable	Disable	Disable	x00	VCM Control
0x109	Clock Divider Synchronization Control	Clock Divider Synchronization Mode: 0 = Use SYNC pin 1 = Use DSYSREF± pin	Reserved					Received Reset Clock Divider Synchronization	Clock Divider Synchronization Enable: 0 = Disabled, 1 = Enabled	x00	
0x10A	Clock Divider Synchronization Received	Disable	Disable	Disable	Disable	Disable	Disable	Disable	Clock Divider Synchronization Received	0x00	Read only

Memory Map Register Description

For more general information about the functions controlled by Register 0x00 through Register 0xFF, refer to Application Note AN-877: "Interfacing to High-Speed ADCs via SPI."

Device Index (Register 0x05)

For certain characteristics designated as local in the map, each channel can be set independently, while other characteristics are global (depending on context), regardless of which channel is selected. Bits [3:0] of Register 0x05 can be used to select which data channels are affected.

Transfer (Register 0xFF)

All registers except Register 0x100 are updated immediately upon writing. When Bit 0 of the Transfer Register is set to 1, the settings of the Resolution/Sample Rate Override Register (Address 0x100) are initialized.

Power Mode (Register 0x08)

- Bit 5 — PDWN Pin Function

When set to 1, the PDWN pin initiates standby mode. When set to 0 (cleared), the PDWN pin initiates full power-down mode.

- Bit 4 — JTX Standby Mode

When set to 1, if the chip standby function is enabled, the JTX module enters standby mode. In standby mode, only the PLL remains running. When cleared to 0, if the chip standby function is enabled, the JTX module remains running.

- Bits [1:0] — Power Mode

In normal operation (Bits [1:0] = 00), all ADC channels and the JTX module are enabled.

In full power-down mode (Bits [1:0] = 01), all ADC channels and the JTX module are powered down, the digital data path clock is disabled, and the digital data path is reset. The outputs are disabled.

In standby mode (Bits [1:0] = 10), all ADC channels are partially powered down, and the digital data path clock is disabled. If JTX standby mode is set, the outputs are also disabled.

During digital reset (Bits [1:0] = 11), all other digital data path clocks and outputs (where applicable) of the chip are reset, except for the SPI port. Note that the SPI is always under user control and is never automatically disabled or reset (except at power-up). When digital reset is deasserted, the foreground calibration sequence is initiated.

Enhanced Control (Register 0x0C)

- Bit 2 — Chopper Mode

For applications that are sensitive to offset voltage and other low-frequency noise, such as homodyne or direct conversion receivers, Bit 2 can be set to enable the chopping feature of the first stage of this product. In the frequency domain, chopping converts offset and other low-frequency noise to $f_{CLK}/2$, which can be filtered out.

Output Mode (Register 0x14)

- Bits [7:5] — JTX CS Mode

Specifies the meaning of the JTX control bits.

- Bits [1:0] — Output Format

By default, this field is set to 1, and data is output in twos complement format. When this field is cleared to 0, the output mode changes to offset binary.

Clock Phase Control (Register 0x16)

- Bits [6:4] — Input Clock Phase Adjustment

When using the clock driver (Register 0x0B), the applied clock frequency is higher than the internal sampling clock. Bits [6:4] determine the phase of the external clock at which sampling is performed. This only applies when using the clock divider. Bits [6:4] cannot be set to a value greater than Bits [2:0] of Register 0x0B.

JTX User Mode Code (Register 0xA0 to Register 0xA7)

When Bits [3:0] of register 0x61 are set to 5 or 6, the mode codes in these registers are output on all active lanes. When Bits [5:4] of register 0x61 are set to 2, a 32-bit mode code formed by concatenating register 0xA0, register 0xA2, register 0xA4, and register 0xA6 is inserted before the scrambler. When Bits [5:4] of Register 0x61 are set to 1 (40-bit mode code), a mode code formed by concatenating the following is inserted before the 8b/10b encoder: Bits [1:0] of Register 0xA1 and Bits [7:0] of Register 0xA0; Bits [1:0] of Register 0xA3 and Bits [7:0] of Register 0xA2; Bits [1:0] of Register 0xA5 and Bits [7:0] of Register 0xA4; Bits [1:0] of Register 0xA7 and Bits [7:0] of Register 0xA6.

Resolution/Sample Rate Override (Register 0x100)

In applications that do not require the highest resolution and/or sample rate, the user can use this register to reduce the resolution and/or maximum sample rate (to reduce power consumption). The settings of this register are initialized after Bit 0 of the Transfer Register (Register 0xFF) is written high.

Bits [2:0] do not affect the sample rate but affect the maximum sample rate of the ADC. User I/O Control 2 (Register 0x101)

- Bit 0 — SDIO Pull-Down

Bit 0 can be set to disable the built-in 30 kΩ pull-down resistor on the SDIO pin. This setting can be used to limit the load when many devices are connected to the SPI bus.

User I/O Control 3 (Register 0x102)

- Bit 3 — VCM Power-Down

By setting Bit 3 high, the internal VCM generator can be turned off. This function is used when using an external reference voltage source.

Application information

Design Guidelines

Before performing system-level design and layout of this product, it is recommended that designers familiarize themselves with the following design guidelines, which discuss special circuit connections and layout requirements for certain pins.

Power Supply and Grounding Recommendations

When connecting power to this product, it is recommended to use two separate 1.8 V supplies: one supply for the analog output (AVDD) and another supply for the digital output (DRVDD and DVDD). Designers can use multiple different decoupling capacitors suitable for high and low frequencies. Decoupling capacitors should be placed close to the printed circuit board (PCB) entry points and close to the device pins, with the shortest possible trace lengths.

This product requires only a single PCB ground plane. Proper decoupling and careful separation of the analog, digital, and clock sections of the PCB can easily achieve optimal performance.

Clock Stability Considerations

At power-up, this product enters an initial phase, and the internal state machine sets biases and registers to allow the device to operate normally. During the initialization process, this product requires a stable clock. If the ADC clock source is absent or unstable during ADC power-up, it may interrupt the state machine, causing the ADC to power up into an unknown state. To correct this state, the initial sequence must be recalled after the ADC clock becomes stable. This operation can be performed by initiating a digital reset via Register 0x08. In the default configuration (internal VREF, AC-coupled input), VREF and VCM are provided by the ADC itself, so the clock is sufficiently stable at power-up. When VREF and/or VCM are supplied by an external source, they must also be stable at power-up; otherwise, a digital reset must be performed via Register 0x08. The pseudo-code sequence for the digital reset is as follows:

SPI_Write (0x08, 0x03); # Digital Reset SPI_Write (0x08, 0x00); # Normal Operation

Exposed Pad Heat Slug Recommendations

For optimal electrical and thermal performance, the exposed pad on the bottom of the ADC must be connected to analog ground (AGND). A continuous copper plane with exposed (solder mask-free) area on the PCB must match the exposed pad (Pin 0) of this product.

The copper plane must have multiple vias to provide the lowest possible thermal resistance path for heat dissipation through the bottom of the PCB. These vias should be filled or plugged with an insulating epoxy. To maximize coverage and connection between the ADC and the PCB, a solder mask layer should be applied to the PCB to divide the continuous plane into multiple equal sections. This prevents solder from accumulating during the reflow process and provides multiple connection points between the ADC and the PCB. A continuous, non-segmented plane only guarantees a single connection point between the ADC and the PCB. For PCB layout examples, refer to the evaluation board. For more detailed information on PCB layout for packages and chip-scale packages, refer to Application Note AN-772: "Pin Array Chip-Scale Package (LFCSP) Design and Manufacturing Guide."

VCM

Decouple the VCM pin to ground using a 0.1 µF capacitor.

Reference Voltage Decoupling

The VREF pin should be decoupled to ground externally using a parallel combination of a low ESR 0.1 µF ceramic capacitor and a low ESR 1.0 µF capacitor.

SPI Port

When the converter is required to achieve its full dynamic performance, the SPI port should be disabled. Typically, the SCLK, CSB, and SDIO signals are asynchronous to the ADC clock, and therefore noise on these signals can degrade converter performance. If other devices share the on-board SPI bus, a buffer may need to be connected between that bus and this product to prevent these signals from changing at the converter's input pins during critical sampling periods.

Overall dimensions

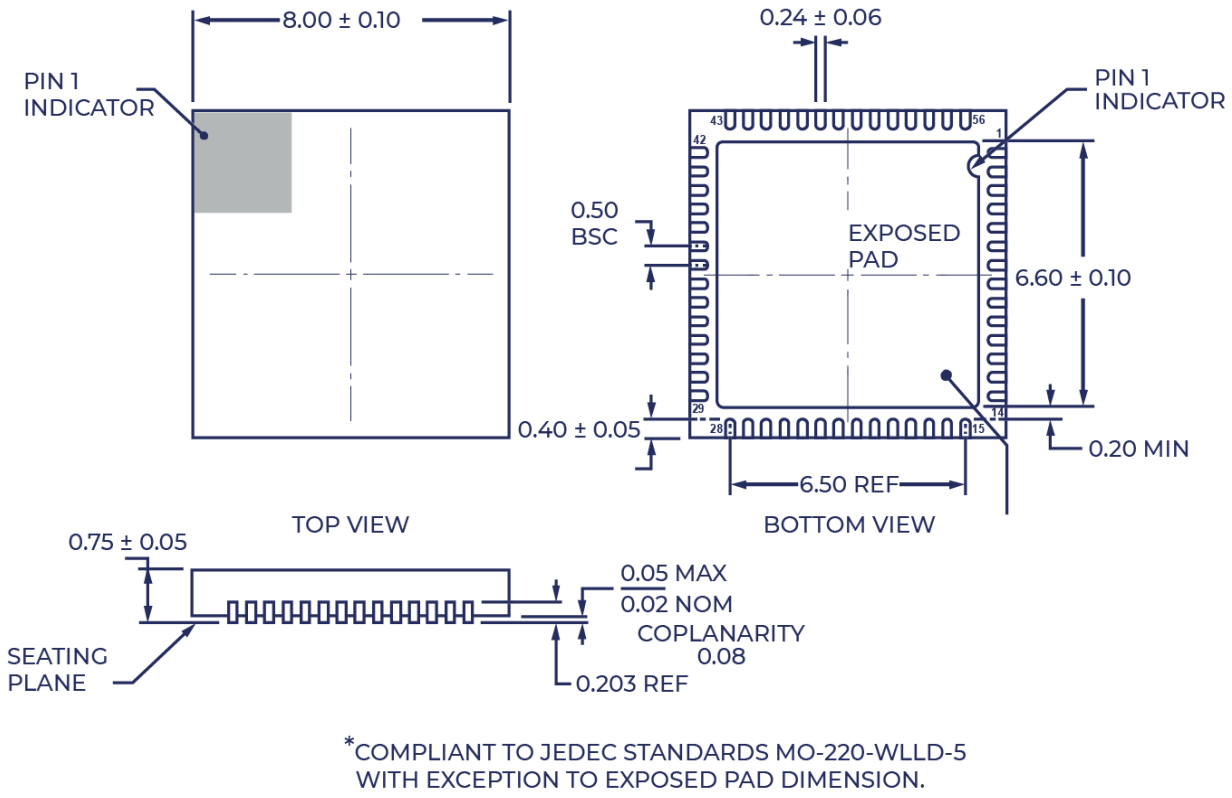

Figure 63. 56-Lead Pin Array Chip-Scale Package (Plastic Version) 8 mm × 8 mm, Dimensions in mm

Packaging / Ordering Information

Product Name	Temperature Range	Package Type	Shipping & Packaging Quantity
TGS96AD56-125	-40℃ ~ 85℃	QFN-56	Tray, 260