



## 1. Features

- Frequency band: 30 MHz ~ 6000 MHz
- Supports TDD and FDD
- Tunable channel bandwidth: 12 kHz to 100 MHz
- Single-channel receiver: 3 differential or 6 single-ended inputs
- Excellent receiver sensitivity with a noise figure of 4 dB
- RX Gain Control:
  - Real-time monitoring and control signal for manual gain
  - Independent automatic gain control
- Single-channel transmitter: 2 differential inputs
- TX power maximum adjustment range: 48 dB
- TX EVM:  $\leq -40$  dB
- TX noise:  $\leq -157$  dBm/Hz noise floor
- TX monitor: dynamic range  $\geq 40$  dB, accuracy = 1 dB
- Integrated fractional-N frequency synthesizer
- Multi-device synchronization
- CMOS/LVDS digital interface

## 2. Main applications

- General software radio system
- Femtocell/picocell/microcell base station
- Multifunctional intelligent terminal
- Point-to-point communication system

## 3. Overview

TGS9364 is a high-performance, highly integrated ultra-wideband SDR transceiver. It can be widely used in almost all modern digital wireless communication systems. It can support a frequency range of 30 MHz to 6000 MHz, and the configurable RF bandwidth can support a range of 12 KHz to 100 MHz.

The device integrates a 12-bit analog-to-digital converter ADC and a 12-bit digital-to-analog converter DAC. It has a built-in programmable analog filter, supporting an analog low-pass filter with a minimum bandwidth of 0.7 MHz and an analog low-pass filter with a maximum bandwidth of 50 MHz for TX and 50 MHz for RX. The mixer and phase-locked loop are also integrated inside the chip, and the transmitting part is integrated with a driver-level amplifier, which can output a single-tone signal of more than 7 dBm.

TGS9364 adopts direct frequency conversion architecture to achieve high modulation accuracy and ultra-low noise. The chip has functions such as image suppression calibration, local oscillator leakage calibration, transmit power monitoring, spurious suppression, and receive channel gain calibration. It also includes multi-chip synchronization function, which is suitable for scenarios where multiple chips are used together, such as MIMO. The chip register read and write control adopts standard four-wire SPI. TGS9364 adopts 10 mm × 10 mm, 144-pin chip-scale ball grid array package (CSP\_BGA).

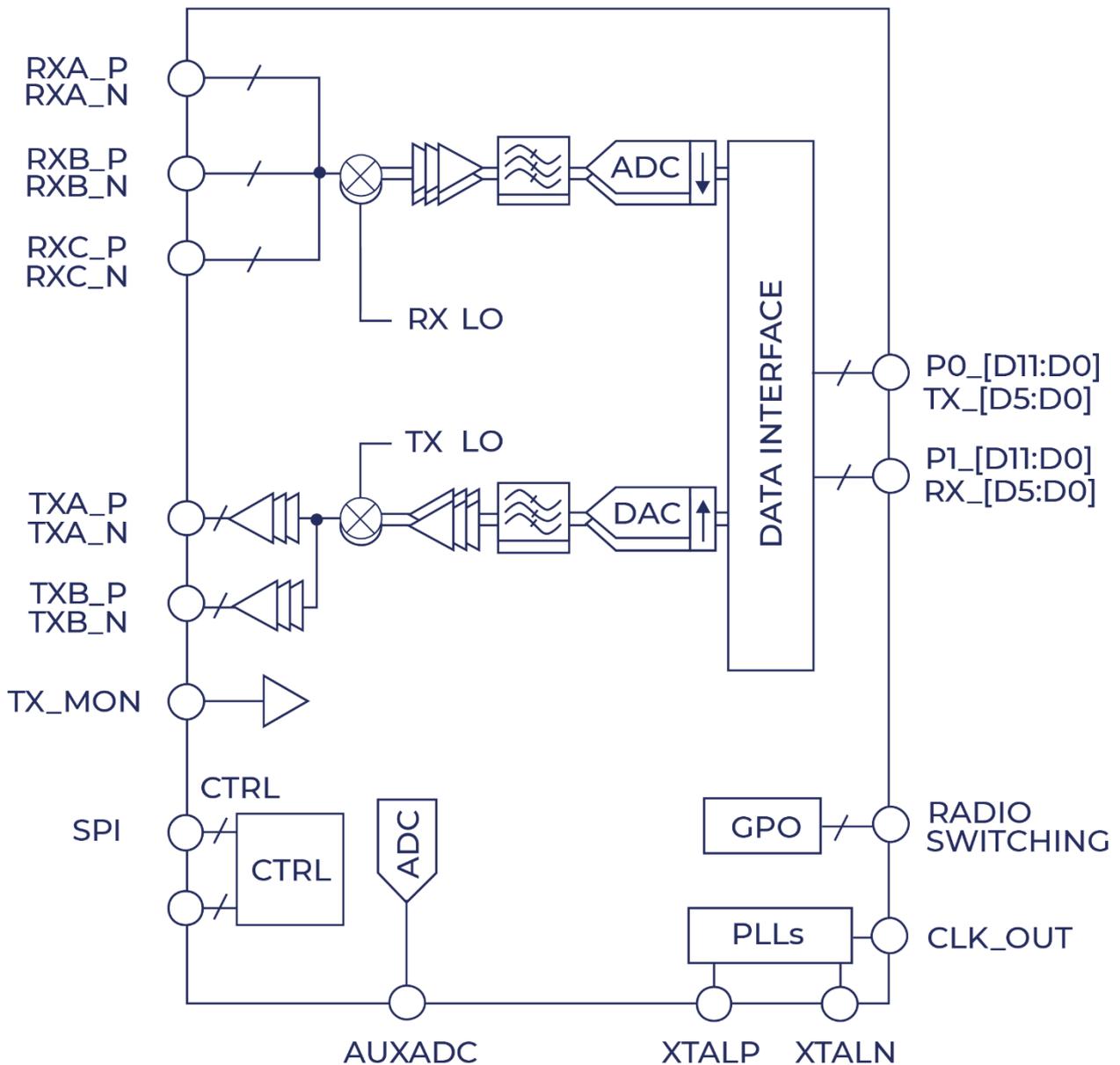


Figure 1. TGS9364 system block diagram

## 4. Product Specifications

### Absolute Maximum Ratings

Parameter	Absolute value range
VDDx to VSSx	-0.3 V ~ +1.5 V
VDD_INTERFACE to VSSx	-0.3 V ~ +2.7 V
VDD_GPO to VSSx	-0.3 V ~ +3.3 V
Logic Inputs and Inputs to VSSx	-0.3 V to VDD_INTERFACE + 0.3 V
Input current to any pin except the power pin	±10 mA
RF Input (Peak Power)	2.5 dBm
TX Monitor Input Power	9 dBm
Maximum Junction Temperature (TJMAX)	110°C
Operating temperature range	-40 ~ 85°C
Storage ambient temperature range	-65 ~ 150°C

Note: Exceeding the absolute maximum ratings listed above may cause permanent damage to the device. This is only a maximum rating, and normal operation of the device cannot be inferred under these conditions or any other conditions exceeding the specifications shown in the operation section of this technical specification. Long-term operation under absolute maximum rating conditions will affect the reliability of the device.

### Recommended operating conditions

Parameter	Recommended value
VDDx	+1.3 V (the actual acceptable range is between 1.3 V - 1.5 V)
VDD_GPO	+3.3 V
VDD_INTERFACE	+2.5 V
Working environment temperature	-40 ~ 85°C

### Thermal resistance parameters

Package Type	$\theta_{JA}$	$\theta_{JB}$	$\theta_{JC}$	Unit
144-Ball (CSP-BGA)	37.5	24.4	22.5	°C/W

### Reflow Temperature Curve

The TGS9364 reflow temperature profile is based on the JEDEC JESD20 device standard. The maximum reflow temperature is 260°C.

### ESD (Electrostatic Discharge) Sensitive Devices

Charged devices and circuit boards may discharge without being noticed. Although this product has patented or proprietary protection circuits, the device may be damaged when encountering high-energy ESD. Therefore, appropriate ESD precautions should be taken to avoid device performance degradation or loss of function.

## 5. Package and pin definition

Dimensions (unit: mm)

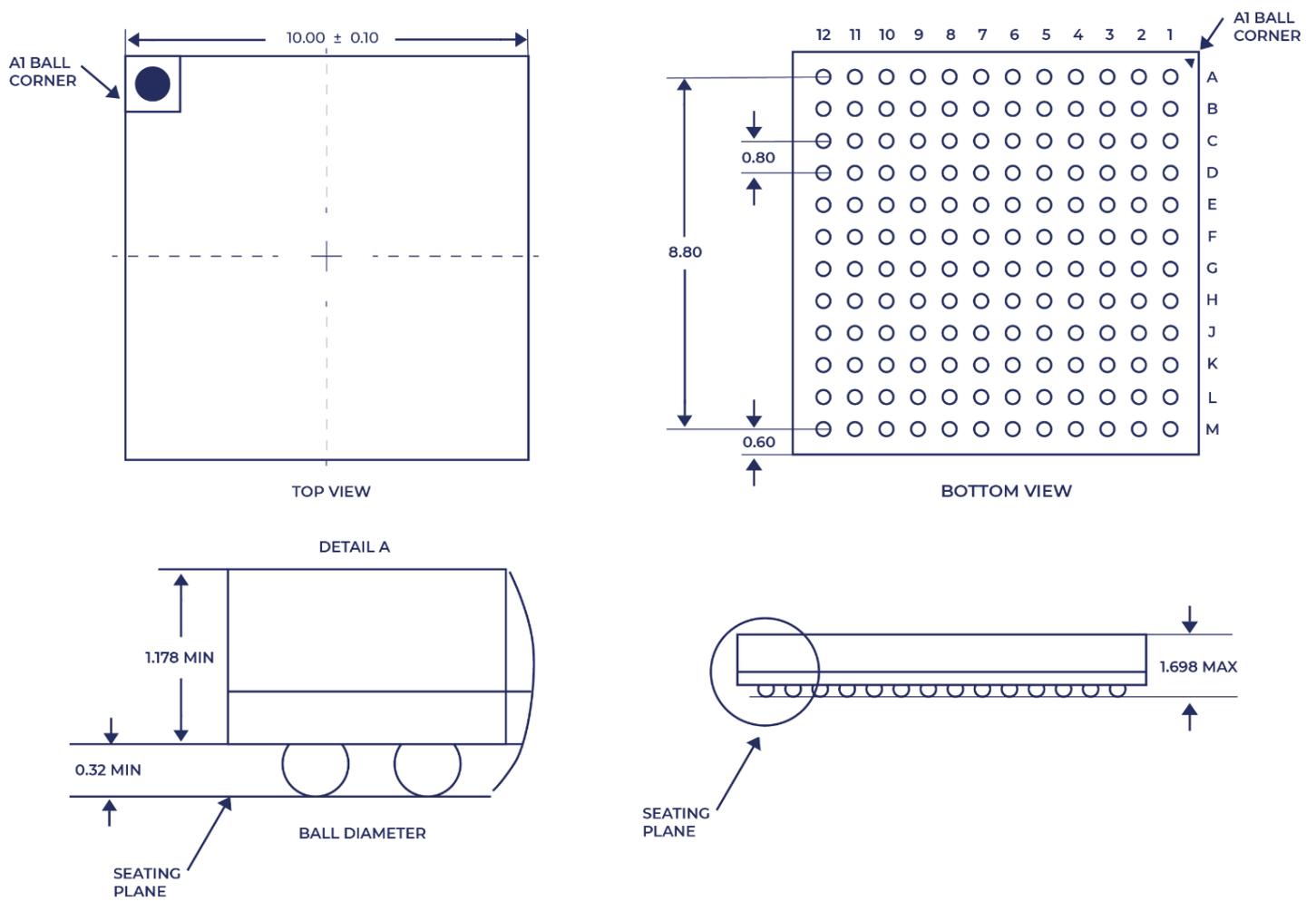


Figure 2.

## Pin Definition

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	TX_EXT_L O_IN
B	VSSA	VSSA	NC	GPO_3	GPO_2	GPO_1	GPO_0	VDD_GPO	VDD1P3_R F	NC	NC	VSSA
C	NC	VSSA	NC	TEST/ENA BLE	CTRL_IN0	CTRL_IN1	NC	VSSA	VSSA	VSSA	VSSA	VSSA
D	NC	VDD1P3_T X	AVDD13_ ADDA2	CTRL_OU T0	CTRL_IN3	CTRL_IN2	P0_D9/TX_ D4_P	P0_D7/TX_ D3_P	P0_D5/TX_ D2_P	P0_D3/TX_ D1_P	P0_D1/TX_ D0_P	VSSD
E	NC	VDD1P3_R X	NC	CTRL_OU T1	CTRL_OU T2	CTRL_OU T3	P0_D11/TX_ D5_P	P0_D8/TX_ D4_N	P0_D6/TX_ D3_N	P0_D4/TX_ D2_N	P0_D2/TX_ D1_N	P0_D0/TX_ D0_N
F	NC	VDD1P3_R X	VSSA	CTRL_OU T6	CTRL_OU T5	CTRL_OU T4	VSSD	P0_D10/TX_ D5_N	VSSD	FB_CLK_P	VSSD	VDDD1P3_ DIG
G	RX_EXT_ LO_IN	NC	NC	CTRL_OU T7	EN_AGC	ENABLE	RX_FRAM E_N	RX_FRAM E_P	TX_FRAM E_P	FB_CLK_ N	DATA_CL K_P	VSSD
H	RXC_N	PAD_RXIF IP	PAD_RXIF IN	TXNRX	SYNC_IN	VSSA	VSSD	P1_D11/R X_D5_P	TX_FRAM E_N	VSSD	DATA_CL K_N	VDD_INT ERFACE
J	RXC_P	VSSA	AVDD13_ ADDA1	SPI_DI	SPI_CLK	CLK_OUT	P1_D10/R X_D5_N	P1_D9/RX _D4_P	P1_D7/RX _D3_P	P1_D5/RX _D2_P	P1_D3/RX _D1_P	P1_D1/RX _D0_P
K	RXB_N	VSSA	VDD1P3_T X1	AVDD13_ LFCK	RESETB	SPI_ENB	P1_D8/RX _D4_N	P1_D6/RX _D3_N	P1_D4/RX _D2_N	P1_D2/RX _D1_N	P1_D0/RX _D0_N	VSSD
L	RXB_P	VSSA	PAD_RXIF QP	RBIAS	PADTIP (AUXADC 1)	SPI_DO	TX_EXT_ DAC_I_Iou tB	VSSA	TX_EXT_ DAC_I_Iou t	VSSA	VSSA	VSSA
M	RXA_N	RXA_P	PAD_RXIF QN	TX_EXT_ DAC_Q_Iou t	TX_MON	TX_EXT_ DAC_Q_Iou tB	TXA_P	TXA_N	TXB_P	TXB_N	XTALP	XTALN

Pin number	Type	Pin name	Illustrate
A1, A2, A3, A4, A5, A6, C7, A7, A8, A9, A10, A11, B3, C3, B10, B11, C1, D1, E1, F1, E3, G2, G3,	I	NC	Just leave it floating
A12	I	TX_EXT_LO_IN	External transmit LO input. If this pin is not used, connect to ground.
B1, B2, B12, C2, C8 to C12, F3, H6, J2, K2, L2, L8, L10, L11, L12	I	VSSA	Analogy
B4 to B7	O	GPO_3 to GPO_0	Support 3.3 V universal input
B8	I	VDD_GPO	GPO 3.3V power supply; if not in use, connect to 3.3 V or VDD_INTERFACE or 1.3 V
B9	I	VDD1P3_RF	RF 1.3 V power input
C4	I	TEST/ENABLE	Test input. For normal operation, connect this pin to ground.
C5, C6, D5, D6	I	CTRL_IN0 to CTRL_IN3	Control input. For manual RX gain and TX attenuation control
D2	I	VDD1P3_TX	TX 1.3V power input, connected to D3
D3	I	AVDD13_ADDA2	ADC/DAC 1.3 V power input
D4, E4 to E6, F4 to F6, G4	O	CTRL_OUT0, CTRL_OUT1 to CTRL_OUT3, CTRL_OUT6 to CTRL_OUT4, CTRL_OUT7	These pins are multi-function inputs with programmable functions.
D7	I/O	P0_D9/TX_D4_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D9, it functions as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D4_P) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination) in FDD mode or as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.
D8	I/O	P0_D7/TX_D3_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D7, it functions as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D3_P) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination) in FDD mode or as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.
D9	I/O	P0_D5/TX_D2_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D5, it functions as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D2_P) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination) in FDD mode or as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.
D10	I/O	P0_D3/TX_D1_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D3, it functions as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D1_P) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination) in FDD mode or as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.

Table 4. Pin Definition

Pin number	Type	Pin name	Illustrate
D11	I/O	P0_D1/TX_D0_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D1, it acts as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D0_P) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination) in FDD mode and as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.
D12, F7, F9, F11, G12, H7, H10, K12	I	VSSD	Digitally
E2	I	VDD1P3_RX	Receives 1.3 V power input
E7	I/O	P0_D11/TX_D5_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D11, it functions as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D5_P) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination) in FDD mode or as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.
E8	I/O	P0_D8/TX_D4_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D8, it functions as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D4_N) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination) in FDD mode or as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.
E9	I/O	P0_D6/TX_D3_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D6, it acts as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, in FDD mode this pin (TX_D3_N) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination); in TDD mode this pin (TX_D3_N) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
E10	I/O	P0_D4/TX_D2_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D4, it functions as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D2_N) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination) in FDD mode or as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.
E11	I/O	P0_D2/TX_D1_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D2, it functions as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D1_N) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination) in FDD mode or as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.
E12	I/O	P0_D0/TX_D0_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D0, it acts as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, in FDD mode this pin (TX_D0_N) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination); in TDD mode this pin (TX_D0_N) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
F2	I	VDDA1P3_RX	Receive VCO LDO 1.3 V power supply input
F8	I/O	P0_D10/TX_D5_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. For P0_D10, it acts as part of the 12-bit bidirectional parallel CMOS level data port 0. Alternatively, in FDD mode this pin (TX_D5_N) can also act as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination); in TDD mode this pin (TX_D5_N) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)

Table 5. Pin Definition (Continued)

Pin number	Type	Pin name	Illustrate
F10, G10	I	FB_CLK_P, FB_CLK_N	Feedback Clock. These pins receive the FB_CLK signal as the TX data clock. In CMOS mode, use FB_CLK_P as the input and FB_CLK_N as ground.
F12	I	VDD1P3_DIG	1.3 V digital power input
G1	I	RX_EXT_LO_IN	External receive LO input. If this pin is not used, connect it to ground.
G5	I	EN_AGC	Manual control input for automatic gain control (AGC)
G6	I	ENABLE	Control Input. This pin moves the device between various operating states
G7, G8	O	RX_FRAME_N, RX_FRAME_P	Receive digital data frame input signals. These pins transmit the RX_FRAME signal to indicate whether the RX input data is valid. In CMOS mode, use RX_FRAME_P as the input and keep RX_FRAME_N disconnected.
G9, H9	I	TX_FRAME_P, TX_FRAME_N	Transmit digital data frame input signal. These pins receive the TX_FRAME signal that indicates when the TX data is valid. In CMOS mode, TX_FRAME_P is the input and TX_FRAME_N is grounded.
G11, H11	O	DATA_CLK_P, DATA_CLK_N	Receive Data Clock Inputs. These pins transmit the DATA_CLK signals that the BBP uses to clock the RX data. In CMOS mode, use DATA_CLK_P as the input and leave DATA_CLK_N disconnected.
H1, J1	I	RXC_N, RXC_P	Receive channel differential input C, each pin can also be used as a single-ended input. If this pin is not used, please connect a DC blocking capacitor to ground.
H2, H3	O	PAD_RXIFIP PAD_RXIFIN	Receive channel intermediate frequency differential I input, please leave it unconnected when not in use
H4	I	TXNRX	Enable state machine control signal. This pin controls the data port bus direction. Logic low selects RX direction, logic high selects TX direction
H5	I	SYNC_IN	Input for synchronizing the digital clock between multiple TGS9364 devices. If this pin is not used, connect it to ground.
H8	I/O	P1_D11/RX_D5_P	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D11, it functions as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D5_P) can also function as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination) in FDD mode and as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.
H12	I	VDD_INTERFACE	Digital I/O pins, 1.8 V to 2.5 V supply
J3	I	AVDD13_ADDA1	ADC/DAC 1.3 V power input
J4	I	SPI_DI	SPI serial data input
J5	I	SPI_CLK	SPI clock input
J6	O	CLK_OUT	This pin can be configured to input the external input clock DCXO for the buffered version, or the internal ADC_CLK for the divided version.
J7	I/O	P1_D10/RX_D5_N	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D10, it functions as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D5_N) can also function as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination) in FDD mode and as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.
J8	I/O	P1_D9/RX_D4_P	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D9, it functions as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, this pin (RX_D4_P) can also function as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination) in FDD mode and as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination) in TDD mode.

Table 6. Pin Definition (Continued)

Pin number	Type	Pin name	Illustrate
J9	I/O	P1_D7/RX_D3_P	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D7, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D3_P) can also act as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination); in TDD mode this pin (RX_D3_P) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
J10	I/O	P1_D5/RX_D2_P	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D5, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D2_P) can also act as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination); in TDD mode this pin (RX_D2_P) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
J11	I/O	P1_D3/RX_D1_P	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D3, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D1_P) can also act as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination); in TDD mode this pin (RX_D1_P) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
J12	I/O	P1_D1/RX_D0_P	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D1, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D0_P) can also act as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination); in TDD mode this pin (RX_D0_P) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
K1, L1	I	RXB_N, RXB_P	Receive channel differential input B, each pin can also be used as a single-ended input. If this pin is not used, please connect a DC blocking capacitor to ground.
K3	I	VDD1P3_TX	TX 1.3 V power input.
K4	I	AVDD13_LFCK	SYSPLL/XO 1.3 V power supply input
K5	I	RESETB	Asynchronous reset. A logic low resets the device
K6	I	SPI_ENB	SPI Enable Input. Set this pin to logic low to enable the SPI bus.
J11	I/O	P1_D3/RX_D1_P	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D3, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D1_P) can also act as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination); in TDD mode this pin (RX_D1_P) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
J12	I/O	P1_D1/RX_D0_P	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D1, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D0_P) can also act as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination); in TDD mode this pin (RX_D0_P) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
K7	I/O	P1_D8/RX_D4_N	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D8, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D4_N) can also act as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination); in TDD mode this pin (RX_D4_N) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)

Table 7. Pin Definition (Continued)

Pin number	Type	Pin name	Illustrate
K8	I/O	P1_D6/RX_D3_N	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D6, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D3_N) can also act as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination); in TDD mode this pin (RX_D3_N) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
K9	I/O	P1_D4/RX_D2_N	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D4, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D2_N) can also act as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination); in TDD mode this pin (RX_D2_N) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
K10	I/O	P1_D2/RX_D1_N	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D2, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D1_N) can also act as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination); in TDD mode this pin (RX_D1_N) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
K11	I/O	P1_D0/RX_D0_N	Digital Data Port P1/Receive Differential Input Bus. This is a dual function pin. For P1_D0, it acts as part of the 12-bit bidirectional parallel CMOS level data port 1. Alternatively, in FDD mode this pin (RX_D0_N) can also act as part of the LVDS 6-bit RX differential input bus (with internal LVDS termination); in TDD mode this pin (RX_D0_N) can also act as part of the LVDS 12-bit TX or RX differential input bus (with internal LVDS termination)
L3, M3	O	PAD_RXIFQP PAD_RXIFQN	Receive channel intermediate frequency differential Q input, please leave it unconnected when not in use
L4	I	RBIAS	Bias input reference. Connect this pin to ground through a 14.3 kΩ (1% tolerance) resistor.
L5	O	PADTIP (AUXADC1)	Test pin, can be used to see analog signal. Can also be used for AUXADC; if this pin is not used, please ground it
L6	O	SPI_DO	SPI serial data input in 4-wire mode
L7, L9	O	TX_EXT_DAC_I_IOutB TX_EXT_DAC_I_Iout	Transmitter channel DAC I differential input, please ground when not in use
M1, M2	I	RXA_N, RXA_P	Receive channel differential input A, each pin can also be used as a single-ended input; if this pin is not used, please connect a DC blocking capacitor to the ground
M4, M6	O	TX_EXT_DAC_Q_Iout TX_EXT_DAC_Q_IOutB	Transmitter channel DAC Q differential input, please ground when not in use
M5	I	TX_MON	Transmit channel power monitoring input. If this pin is not used, please connect a DC blocking capacitor to ground.
M7, M8	O	TXA_P, TXA_N	Transmitter channel 1 differential input A, leave it unconnected if not used
M9, M10	O	TXB_P, TXB_N	Transmitter channel 1 differential input B, please leave it unconnected if not used
M11, M12	I	XTALP, XTALN	Reference frequency crystal connection. When using a crystal, connect it between these two pins. When using an external clock source, connect it to XTALN and leave XTALP disconnected

Table 8. Pin Definition (Continued)

## 6. Technical specifications

### Receiver Specifications

Unless otherwise noted, electrical characteristics are measured at VDD\_GPO = 3.3 V, VDD\_INTERFACE = 2.5 V, all other VDDx pins = 1.3 V, T<sub>A</sub> = 25°C.

Parameter	Logo	Minimum value	Typical value	Maximum value	Unit	Test conditions
Receiver center frequency		30		6000	MHz	
Support RF bandwidth		0.012		100	MHz	
Analog gain minimum			8		dB	
Analog gain maximum		48	50	52	dB	52 dB @ 2.4 GHz
Analog Gain Step			1		dB	
Digital gain minimum			0		dB	
Digital gain maximum			50		dB	
Digital gain stepping			0.25		dB	
<b>Receiver 800 MHz</b>						
Noise figure	NF		4		dB	Maximum RX Gain
Third-order input intermodulation point	IIP3		-4.5		dBm	Maximum RX Gain
Second-order input intermodulation point	IIP2		50		dBm	Maximum RX Gain
Local Oscillator (LO) Leakage			-82		dBm	RX front-end input
Modulation accuracy (EVM)			-40		dB	30.72 MHz reference clock; LTE20M, 64QAM
Input S11			-10		dB	
<b>Receiver 2400 MHz</b>						
Noise figure	NF		4		dB	Maximum RX Gain
Third-order input intermodulation point	IIP3		-5		dBm	Maximum RX Gain
Second-order input intermodulation point	IIP2		50		dBm	Maximum RX Gain
Local Oscillator (LO) Leakage			-78		dBm	RX front-end input
Modulation accuracy (EVM)			-39.7		dB	30.72 MHz reference clock; LTE20M, 64QAM
Input S11			-10		dB	
<b>Receiver 5500 MHz</b>						
Noise figure	NF		6.5		dB	Maximum RX Gain
Third-order input intermodulation point	IIP3		-6		dBm	Maximum RX Gain
Second-order input intermodulation point	IIP2		50		dBm	Maximum RX Gain
Local Oscillator (LO) Leakage			-59		dBm	RX front-end input
Modulation accuracy (EVM)			-36.3		dB	30.72 MHz reference clock; LTE20M, 64QAM
Input S11			-10		dB	

Table 9. Receiver Specifications

## Transmitter Specifications

Unless otherwise noted, electrical characteristics are measured at VDD\_GPO = 3.3 V, VDD\_INTERFACE = 2.5 V, all other VDDx pins = 1.3 V, T<sub>A</sub> = 25°C.

Parameter	Logo	Minimum value	Typical value	Maximum value	Unit	Test conditions
Transmitter center frequency		30		6000	MHz	
Support RF bandwidth		0.012		100	MHz	
Analog power control range		46	48	50	dB	48 dB @ 2.4 GHz
Analog power control step			1		dB	
Digital power control range			50		dB	
Digital power control step			0.125		dB	
<b>TX Monitor (TX_MON1)</b>						
Maximum input level			9		dBm	
Dynamic range			41		dB	
Accuracy			1		dB	
<b>Transmitter 800 MHz</b>						
Lose S22			-10		dB	
Maximum power transmission			4		dBm	Single tone
Modulation accuracy (EVM)			-44		dB	30.72 MHz reference clock; LTE20M, QPSK
Third-order transmission and load regulation point	OIP3		17		dBm	
Carrier leakage			-63		dBc	0 dB Attenuation
Carrier leakage			-34		dBc	40 dB Attenuation
Image suppression			-75		dBc	
Noise floor			-158		dBm/Hz	
<b>Transmitter 2400 MHz</b>						
Lose S22			-10		dB	
Maximum power transmission			5		dBm	Single tone
Modulation accuracy (EVM)			-42		dB	30.72 MHz reference clock; LTE20M, QPSK
Third-order transmission and load regulation point	OIP3		17		dBm	
Carrier leakage			-57		dBc	0 dB Attenuation
Carrier leakage			-31		dBc	40 dB Attenuation
Image suppression			-67		dBc	
Noise floor			-158		dBm/Hz	
<b>Transmitter 5500 MHz</b>						
Lose S22			-10		dB	
Maximum power transmission			7		dBm	Single tone
Modulation accuracy (EVM)			-38		dB	30.72 MHz reference clock; LTE20M, QPSK
Third-order transmission and load regulation point	OIP3		16.9		dBm	
Carrier leakage			-60		dBc	0 dB Attenuation
Carrier leakage			-30		dBc	40 dB Attenuation
Image suppression			-62		dBc	
Noise floor			-153		dBm/Hz	

Table 10. Transmitter Specifications

## Frequency Synthesis Index

Unless otherwise noted, electrical characteristics are measured at VDD\_GPO = 3.3 V, VDD\_INTERFACE = 2.5 V, all other VDDx pins = 1.3 V, T<sub>A</sub> = 25°C.

Parameter	Minimum value	Typical value	Maximum value	Unit	Test conditions
<b>Reference clock</b>					
Reference clock (crystal or external oscillator)	7.68		122.88	MHz	
<b>Local Oscillator Frequency Synthesizer</b>					
local oscillator resolution		2.4		Hz	
Integrated phase noise (10KHz~100MHz)		0.073		°rms	800 MHz
		0.213		°rms	2400 MHz
		0.574		°rms	5500 MHz
<b>Baseband Frequency Synthesizer</b>					
Input frequency range	1600		3600	MHz	

Table 11. Frequency Synthesis Index

## Power consumption index

Unless otherwise noted, electrical characteristics are measured at VDD\_GPO = 3.3 V, VDD\_INTERFACE = 2.5 V, all other VDDx pins = 1.3 V, T<sub>A</sub> = 25°C.

Parameter	Minimum value	Typical value	Maximum value	Unit	Test conditions
1T1R_LTE20M Power Consumption		793		mW	B3 Band LTE20M FDD
1T1R_100M_FDD Power Consumption		1059		mW	N41 Band NR100M FDD
1T_NR100_TDD Power Consumption		555		mW	N41 Band NR100M TDD
1R_NR100_TDD Power Consumption		750		mW	N41 Band NR100M TDD
Sleep mode power consumption		0.14		mW	Sleep Mode

Table 12. Power consumption indicators

# Typical performance parameters

## 800 M Band

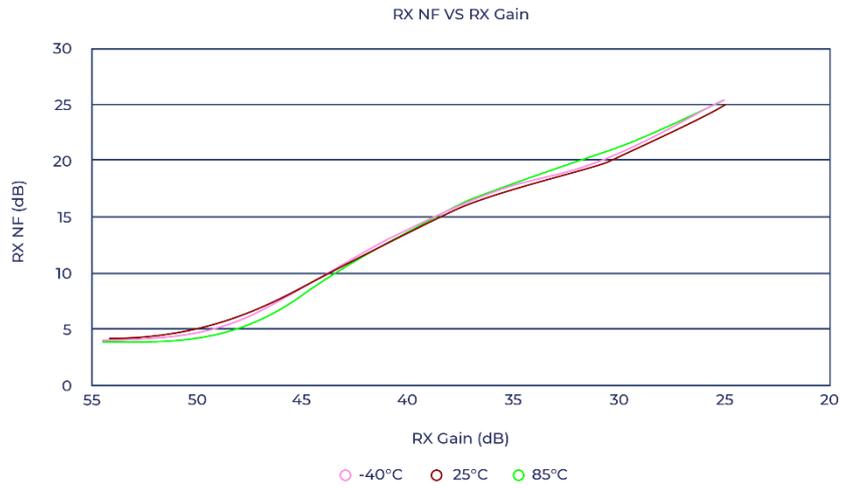


Figure 3. Relationship between RX NF and RX Gain (RX LO = 800 M)

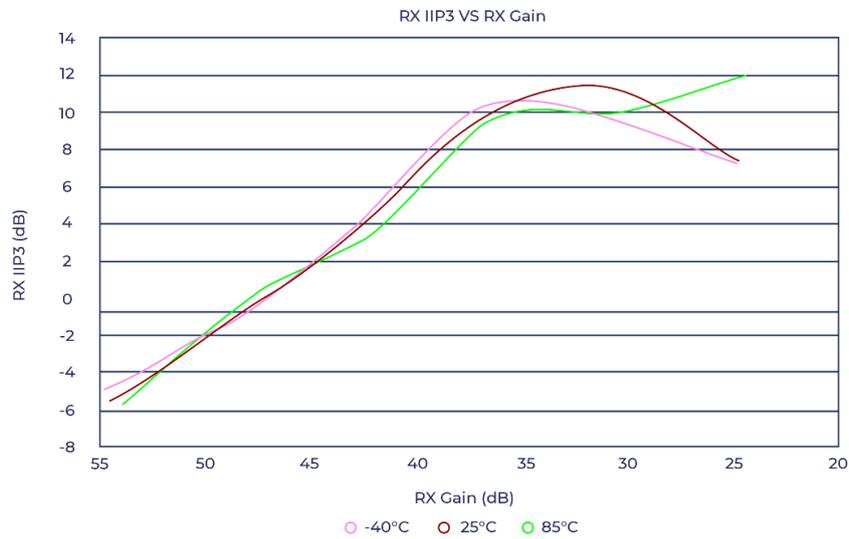


Figure 4. Relationship between RX IIP3 and RX Gain (RX LO = 800 M)

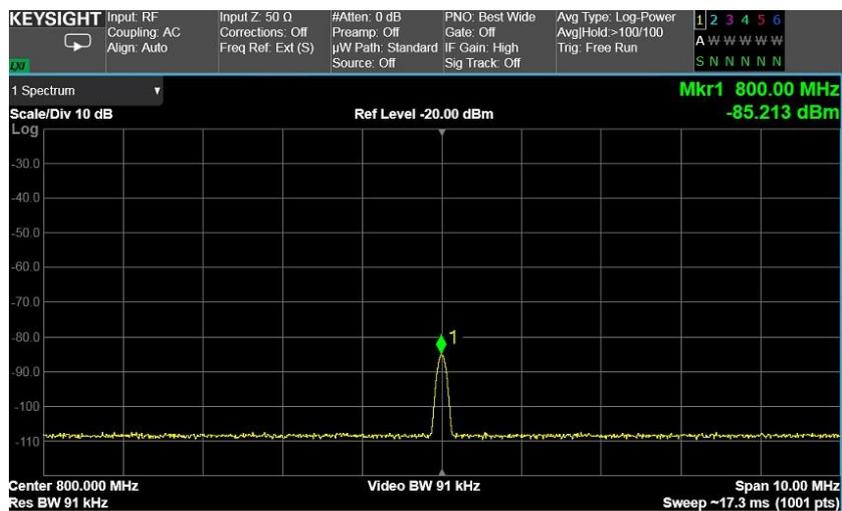


Figure 5. RX LO leakage (RX LO = 800 M)

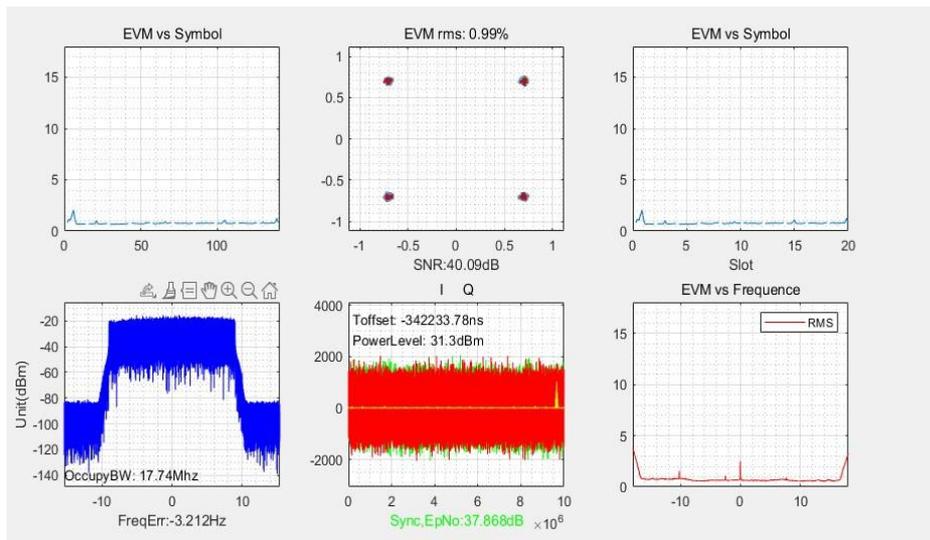


Figure 6. RX EVM@-50dBm input, Max Gain (RX LO = 800 M)

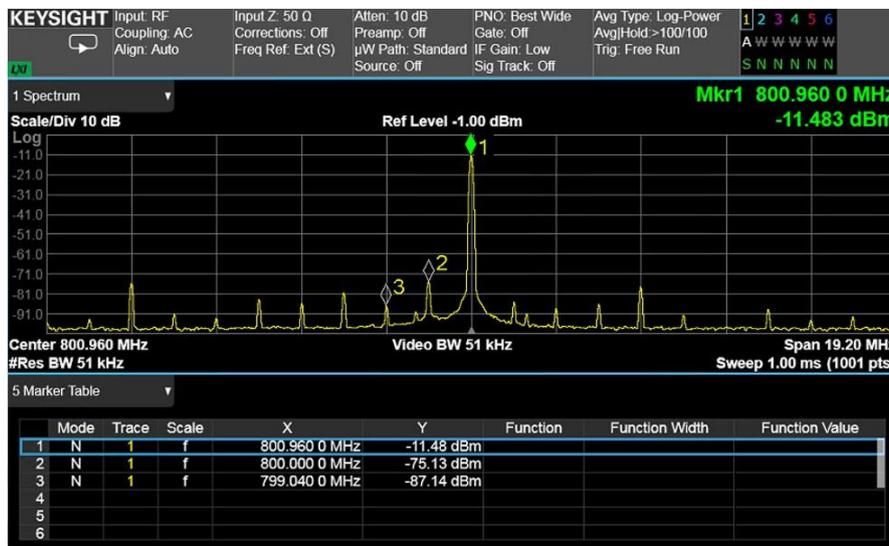


Figure 7. TX QEC&LOL (TX LO = 800 M, 0 dB attenuation)

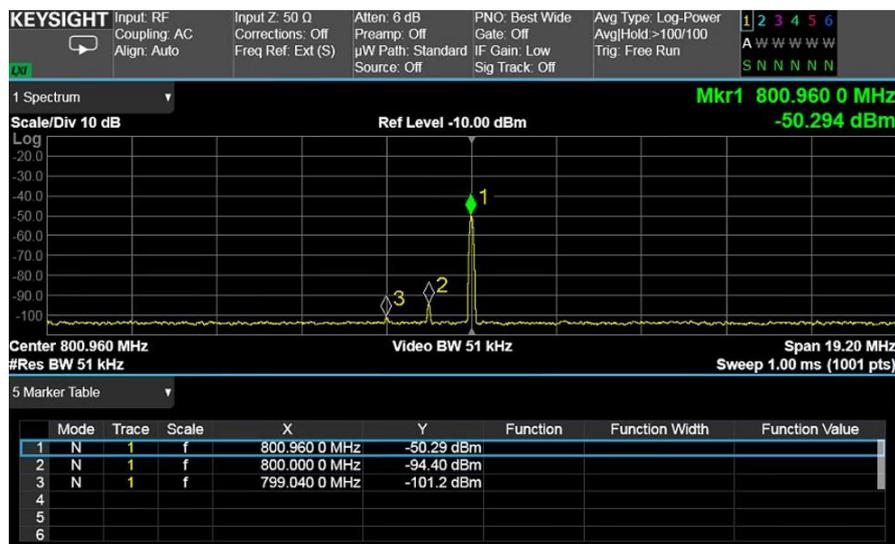


Figure 8. TX QEC&LOL (TX LO = 800 M, 40 dB attenuation)

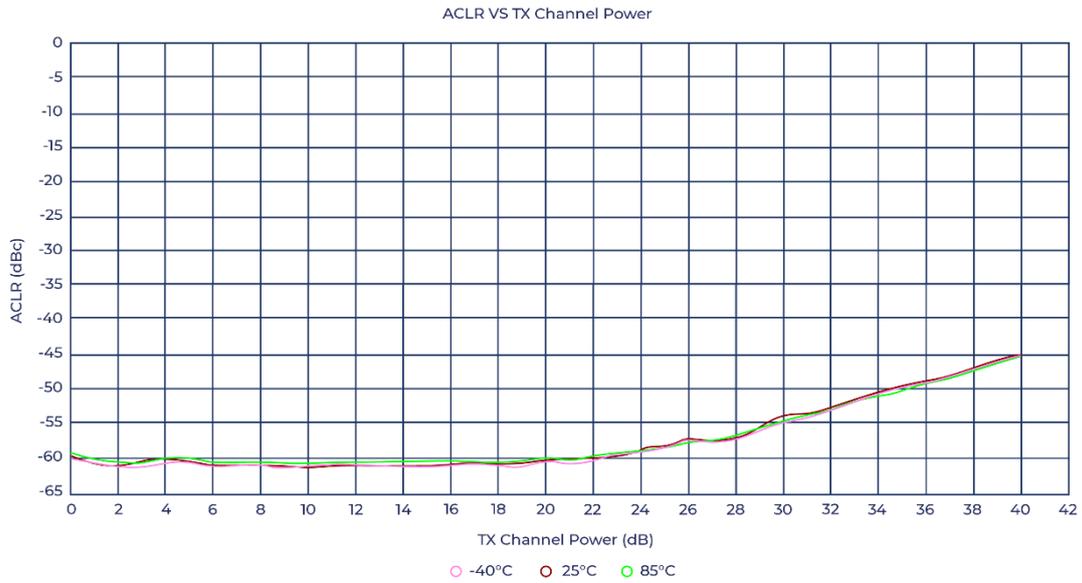


Figure 9. Relationship between TX ACLR and TX Channel Power (TX LO = 800 M)

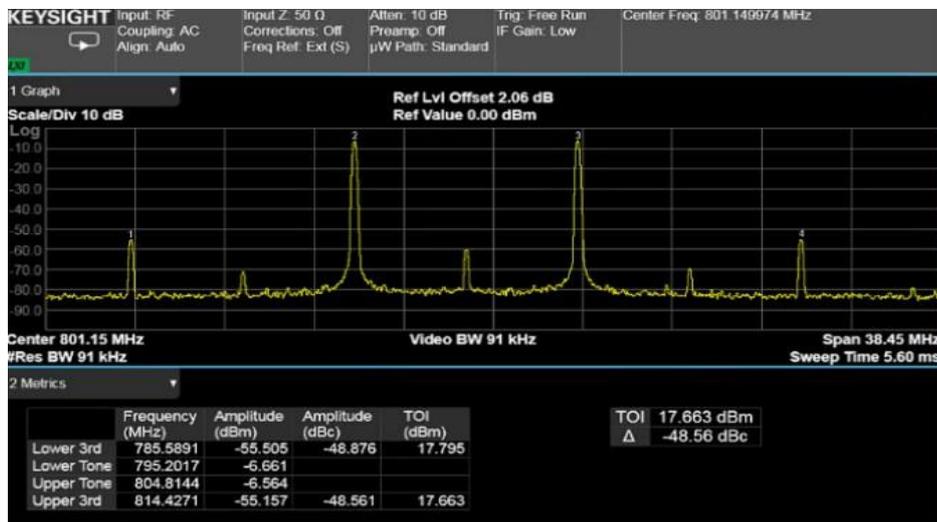


Figure 10. TX OIP3 (TX LO = 800 M)

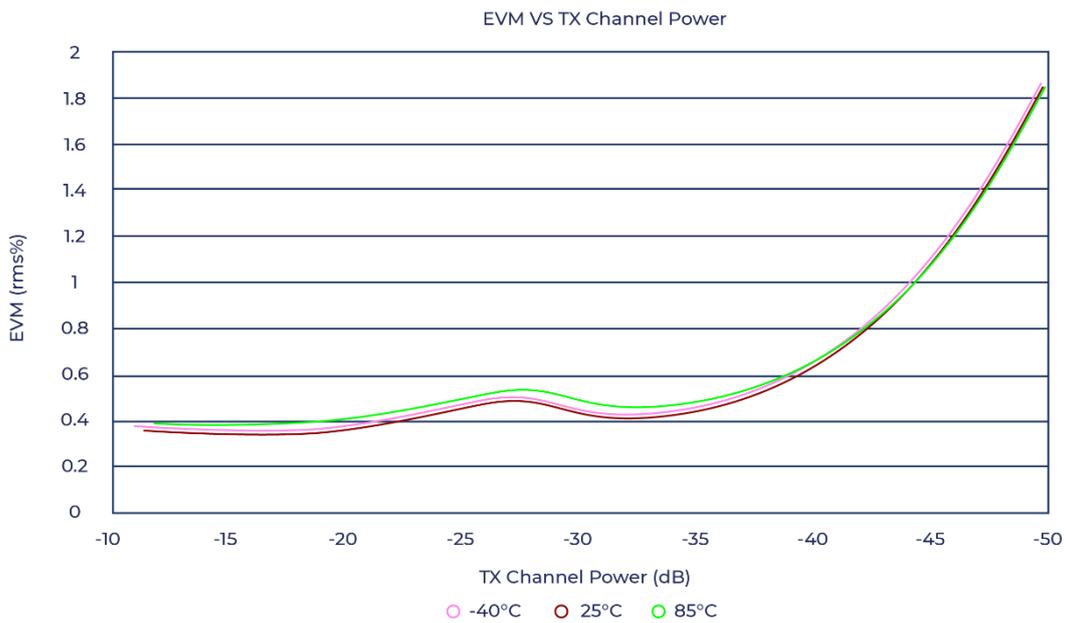


Figure 11. Relationship between TX EVM and TX Channel Power (TX LO = 800 M)

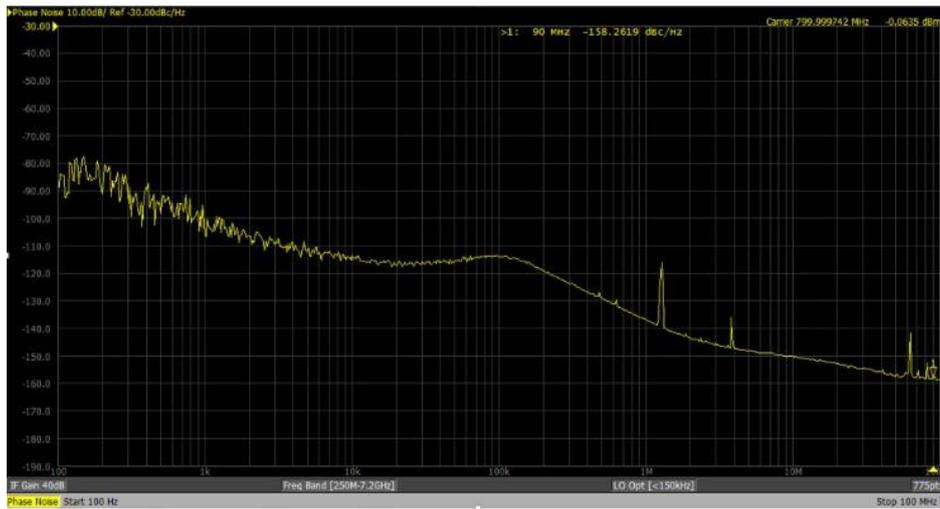


Figure 12. Noise floor (TX LO = 800 M)

### 2.4G frequency band

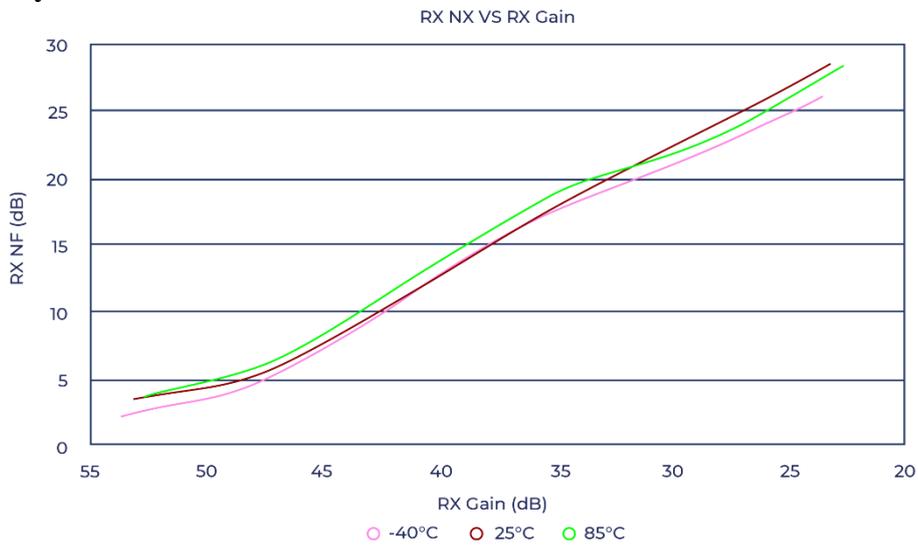


Figure 13. Relationship between RX NF and RX Gain (RX LO = 2.4G)

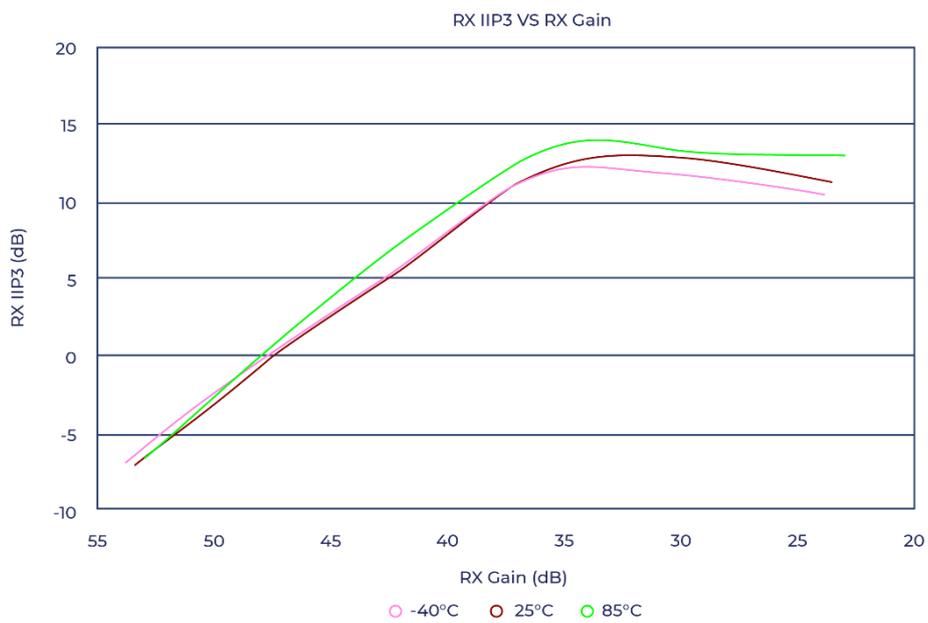


Figure 14. Relationship between RX IIP3 and RX Gain (RX LO = 2.4G)

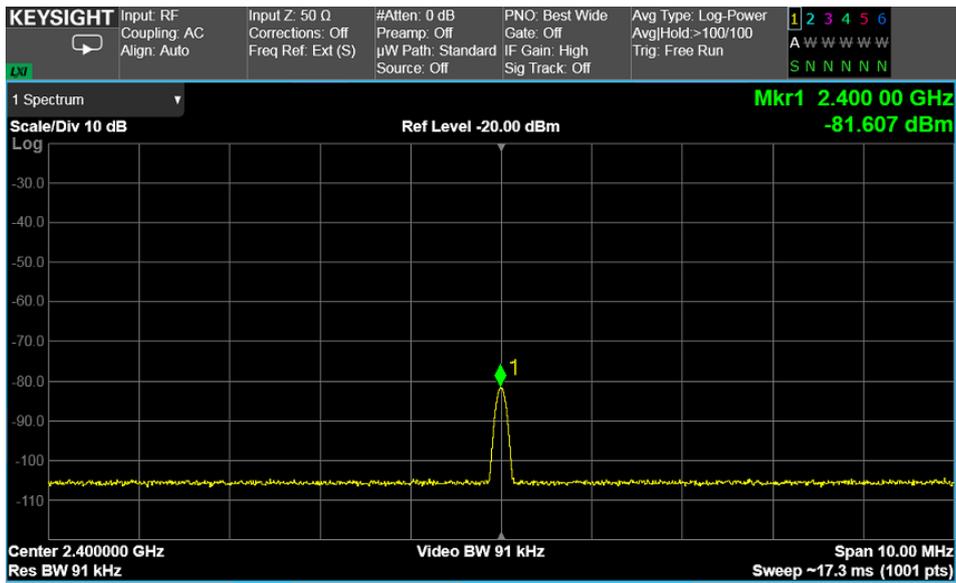


Figure 15. RX LO leakage (RX LO = 2.4G)

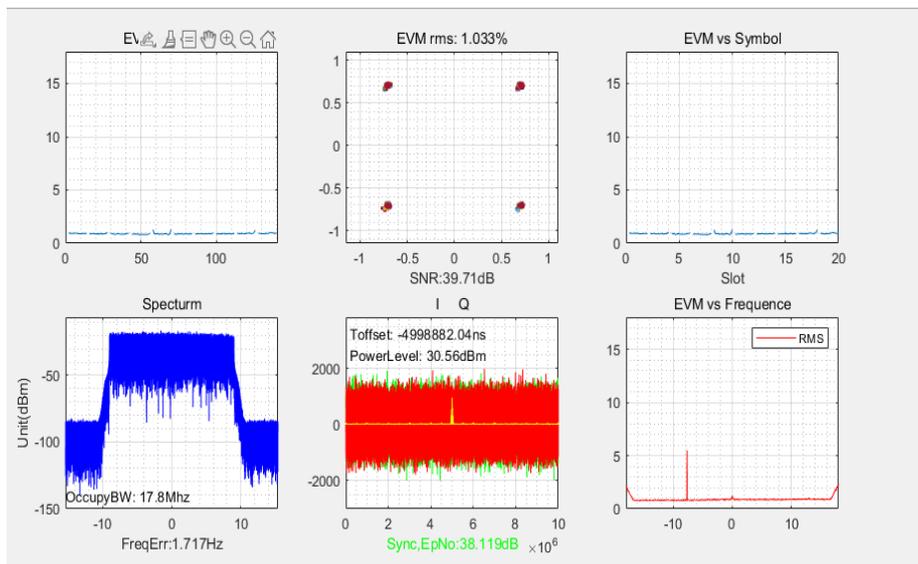


Figure 16. RX EVM@-50dBm input, Max Gain (RX LO = 2.4G)

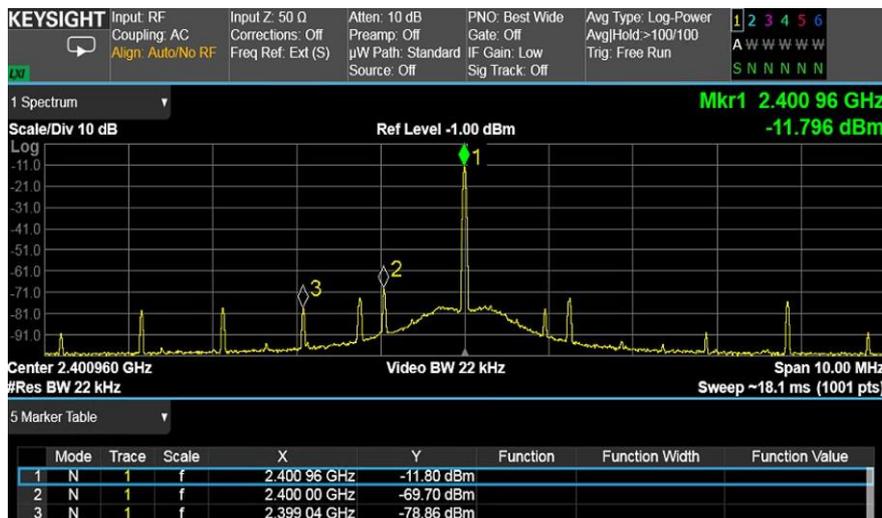


Figure 17. TX QEC&LOL (TX LO = 2.4G, 0 dB attenuation)

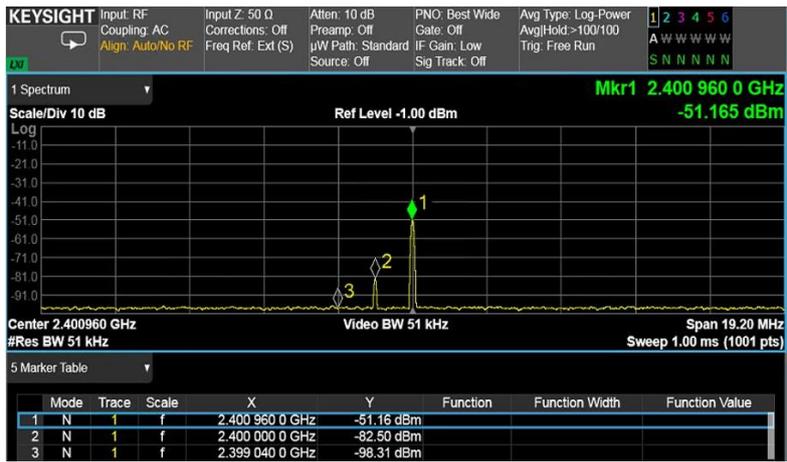


Figure 18. TX QEC&LOL (TX LO = 2.4G, 40 dB attenuation)

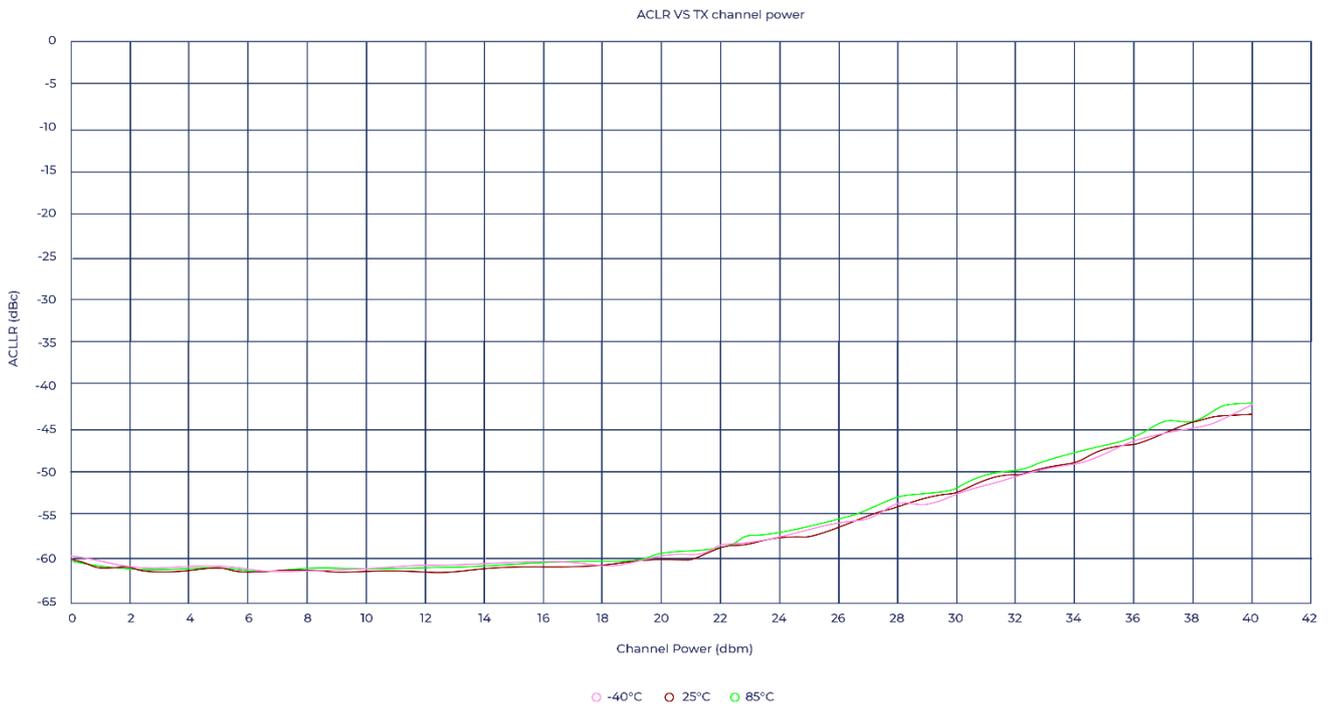


Figure 19. Relationship between TX ACLR and TX Channel Power (TX LO = 2.4G)

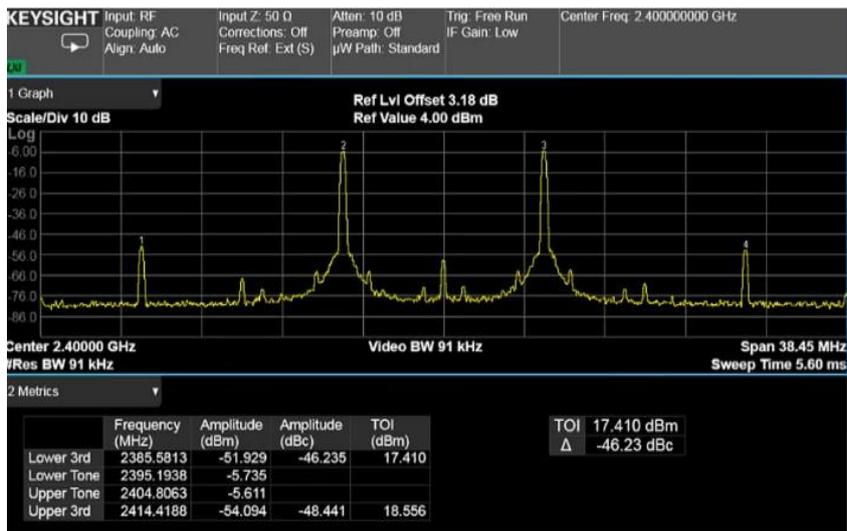


Figure 20. TX OIP3 (TX LO = 2.4G)

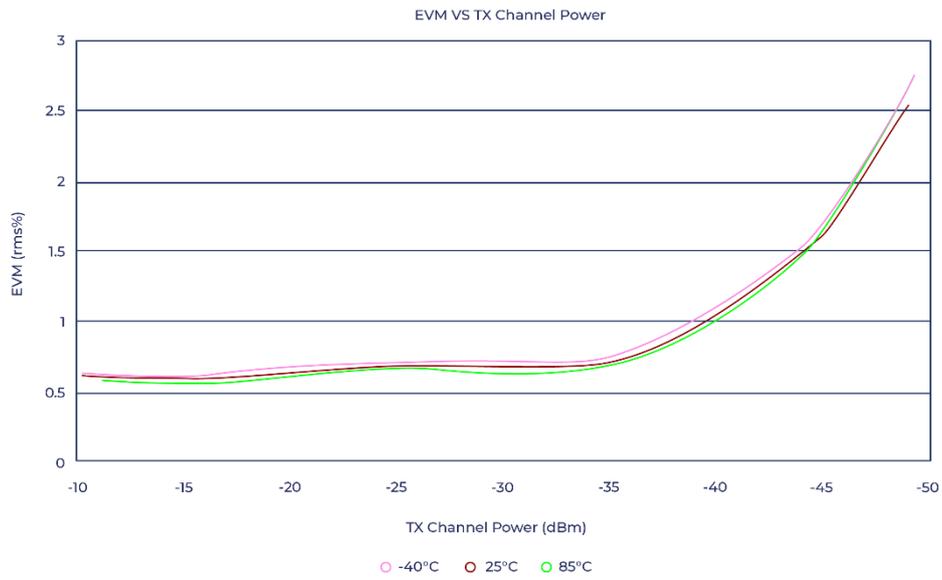


Figure 21. Relationship between TX EVM and TX Channel Power (TX LO = 2.4G)

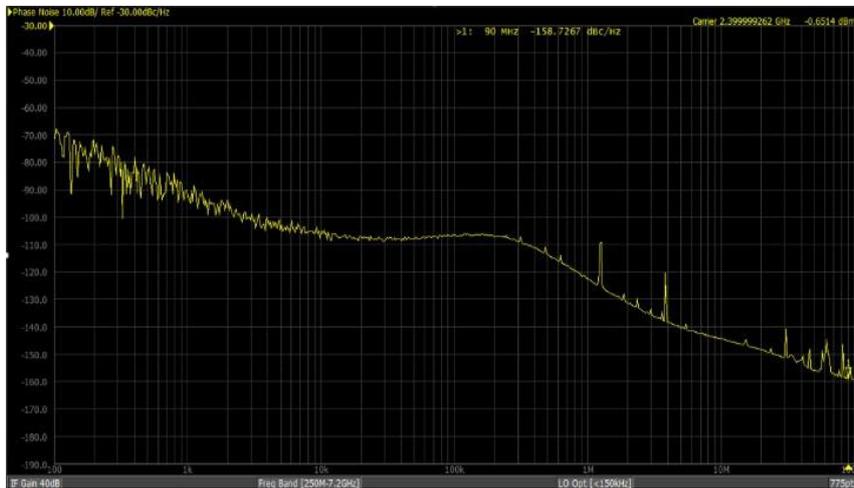


Figure 22. TX noise floor (TX LO = 2.4G)

### 5.5G frequency band

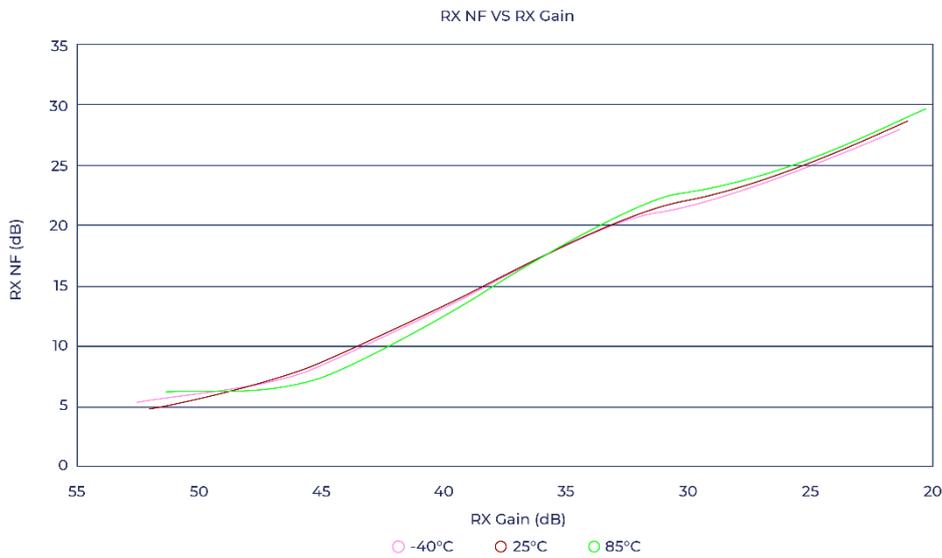


Figure 23. Relationship between RX NF and RX Gain (RX LO = 5.5G)

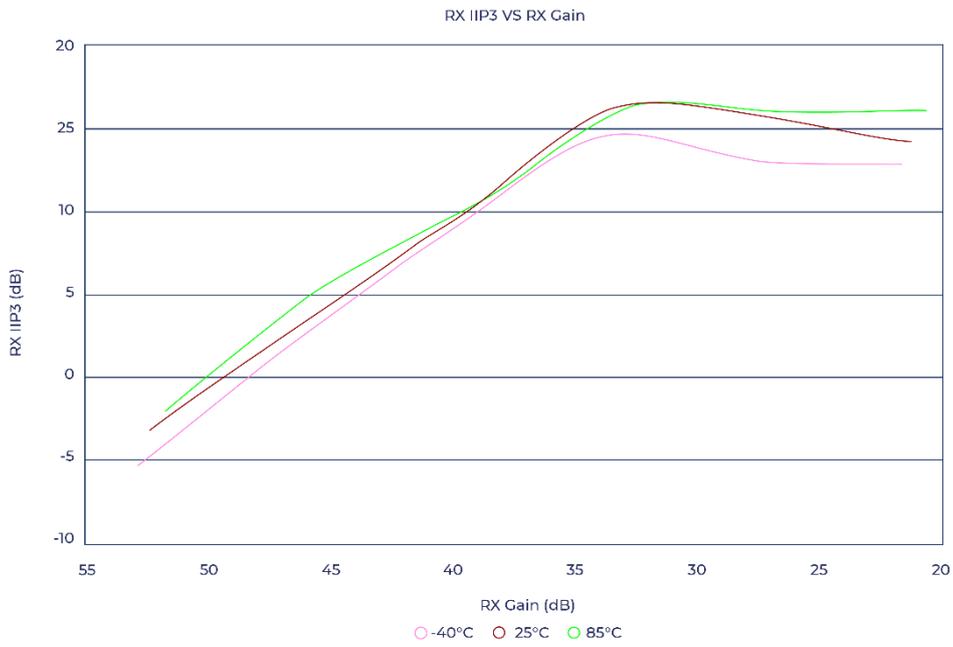


Figure 24. Relationship between RX IIP3 and RX Gain (RX LO = 5.5G)

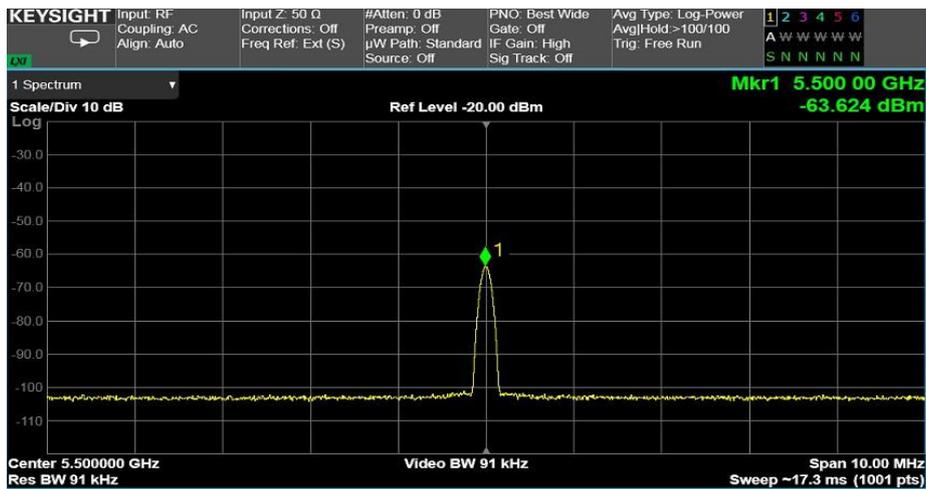


Figure 25. RX LO leakage (RX LO = 5.5G)

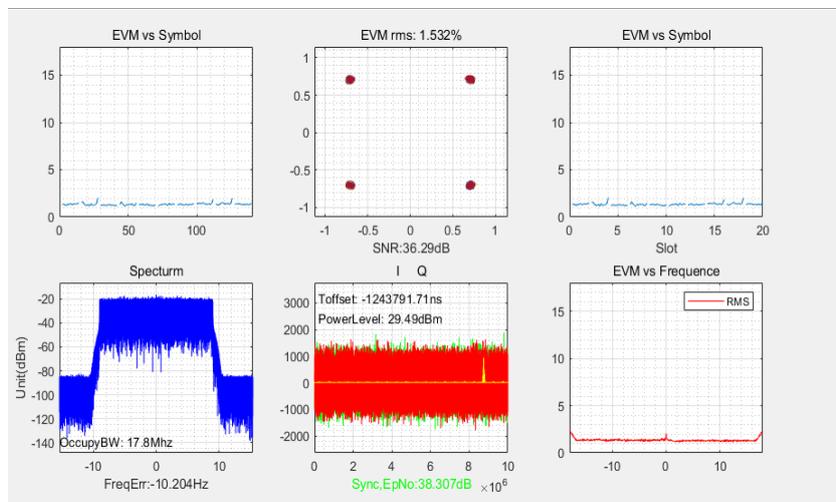


Figure 26. RX EVM@-50dBm input, Max Gain (RX LO = 5.5G)

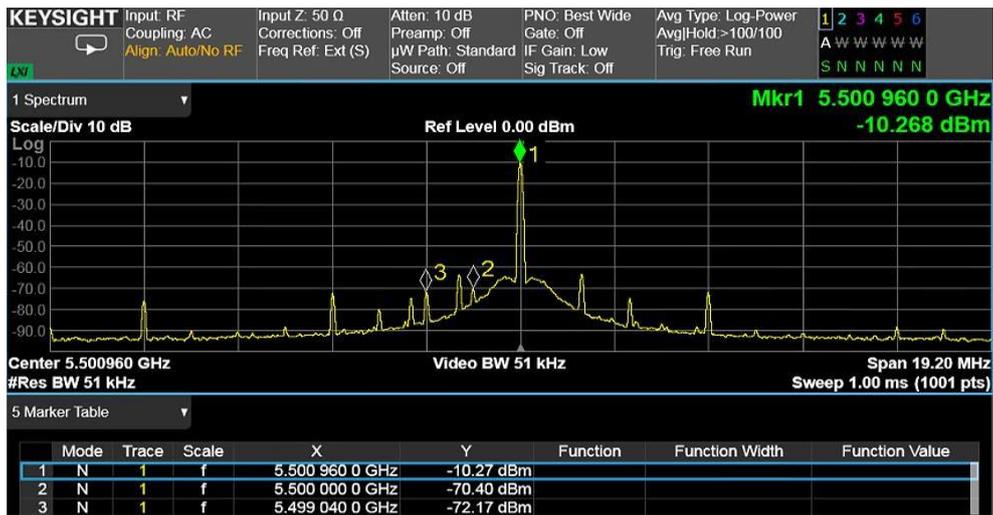


Figure 27. TX QEC&LOL (TX LO = 5.5G, 0 dB attenuation)

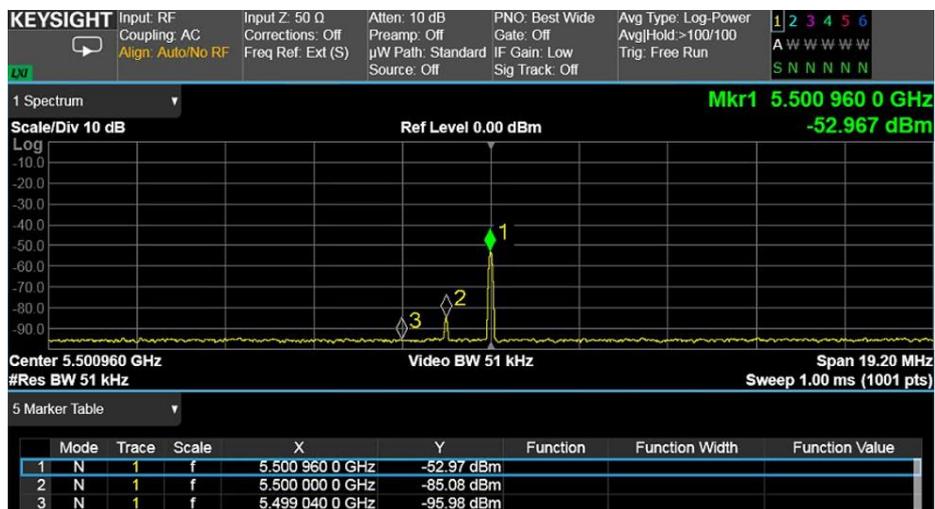


Figure 28. TX LOL leakage (TX LO = 5.5G)

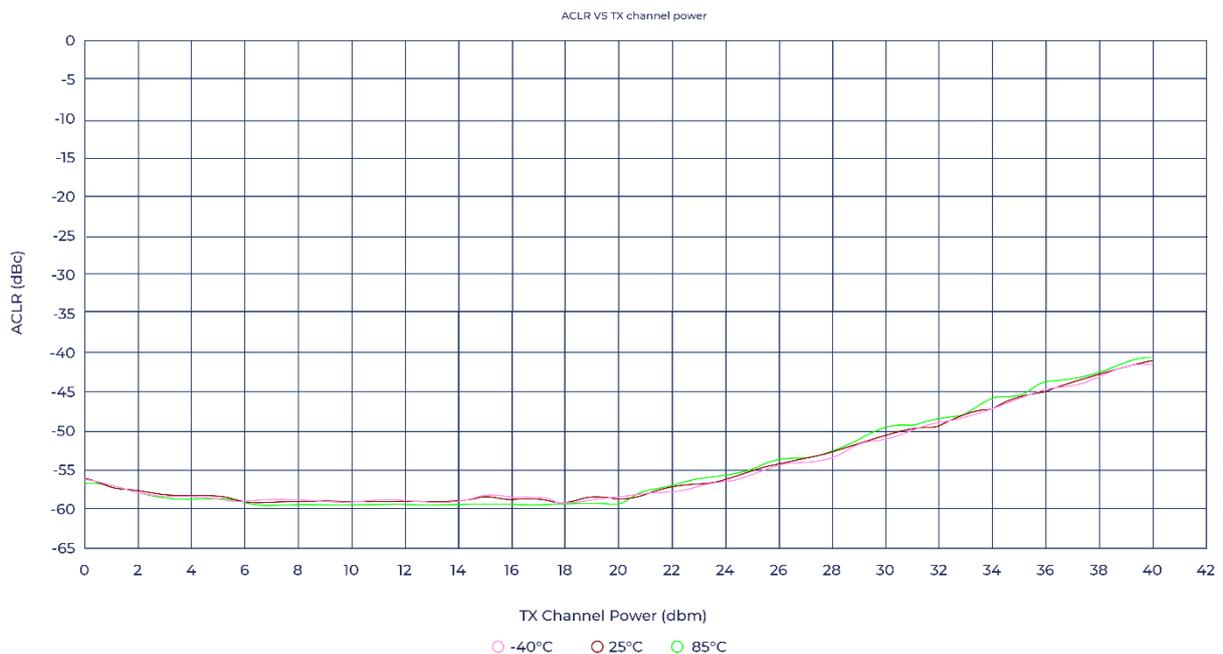


Figure 29. Relationship between TX ACLR and TX Channel Power (TX LO = 5.5 G)

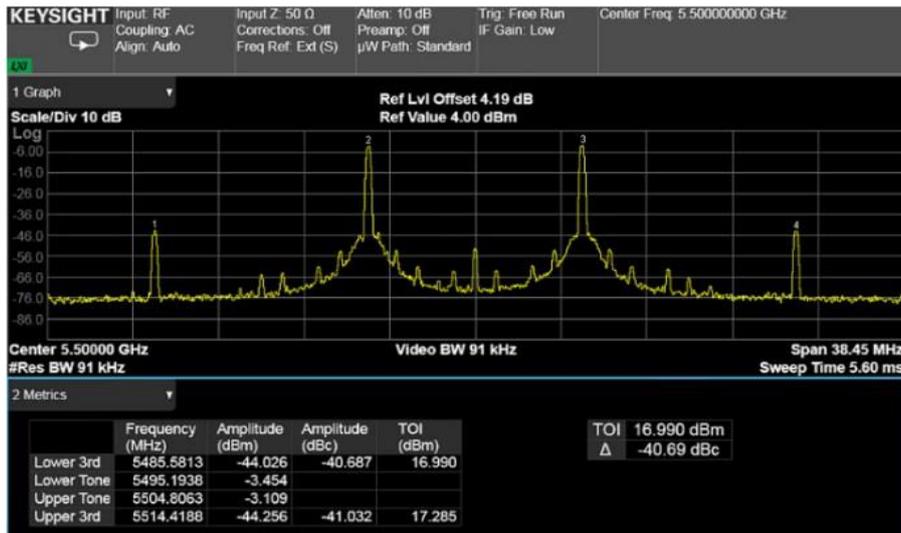


Figure 30. TX OIP3 (TX LO = 5.5 G)

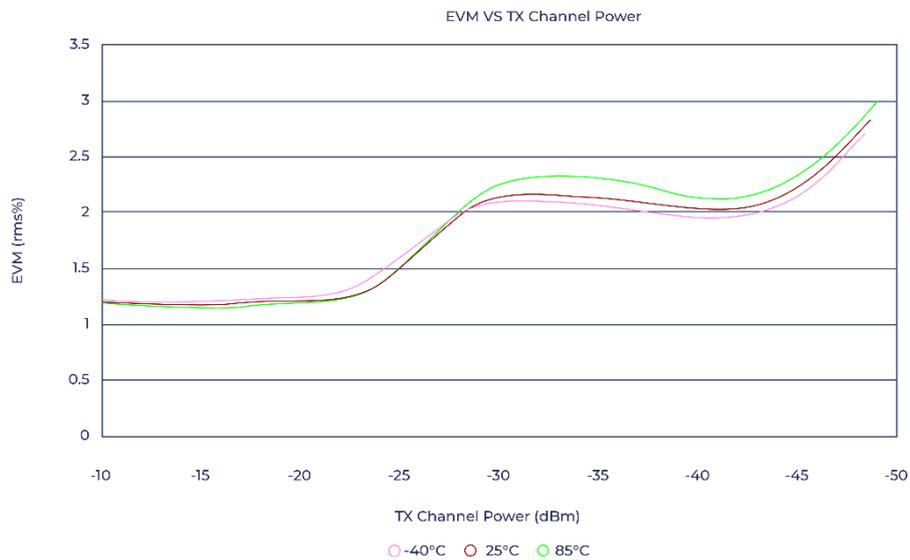


Figure 30. Relationship between TX EVM and TX Gain Index (TX LO = 5.5 G)



Figure 31. TX noise floor (TX LO = 5.5 G)

## 7. Working Principle

### General characteristics

The TGS9364 is a highly integrated radio frequency (RF) transceiver that can be configured for a wide range of applications, integrating all the necessary RF, mixed signal and digital blocks that provide all transceiver functions in a single device. Programmability enables this wideband transceiver to be suitable for a variety of communication standards, including frequency division duplex (FDD) and time division duplex (TDD) systems. In addition, this programmability also allows connection to various baseband processors (BBPs) through a single-channel 12-bit parallel data port, a dual-channel 12-bit parallel data port, or a 12-bit low voltage differential signaling (LVDS) interface.

The TGS9364 also provides a self-calibration and automatic gain control (AGC) system to maintain high performance levels over a wide range of temperature and input signal conditions.

### Receiver

The receiver section contains all the necessary blocks to receive the RF signal and convert it into digital data for use by the BBP. The receive path contains three differential inputs or six single-ended inputs that can be multiplexed into the signal chain, allowing the TGS9364 to be used in diversity systems with multiple antenna inputs. The receiver is a direct conversion system that contains mixers and band-shaping filters that down-convert the received signal to baseband for digitization.

Gain control is achieved based on a pre-programmed gain index map that distributes the gain between the blocks to optimize performance at each level. This can be achieved by enabling the internal AGC in fast or slow mode, or by manual gain control, allowing the BBP to adjust the gain as needed. In addition, each channel has independent RSSI measurement capabilities, DC offset tracking capabilities, and all the necessary circuitry to perform self-calibration.

The receiver includes a 12-bit SAR ADC with an adjustable sampling rate to produce a data stream from the received signal. The digitized signal can be further conditioned through a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sampling rate of each digital filter block can be adjusted by changing the decimation factor to produce the desired output data rate.

### Transmitter

The transmitter section provides all the necessary digital processing, mixed signal and RF blocks to implement a direct conversion system using a general-purpose frequency synthesizer. The digital data received from the BBP passes through a fully programmable 128-tap FIR filter without interpolation options. The FIR input is sent to a series of interpolation filters that provide additional filtering and data rate interpolation before the output reaches the DAC. Each 12-bit DAC has an adjustable sampling rate. Both the I and Q channels feed the RF block for up-conversion.

Each transmit channel has built-in self-calibration circuitry to support automatic real-time adjustments. The transmitter module also provides a TX monitor module for each channel. This module monitors the transmitter input and sends it back to the BBP through an unused receiver channel for signal monitoring. The TX monitor module is only available in TDD mode when the receiver is idle.

### Clock Input Options

The reference clock input level range used by TGS9364 when running is 0.5Vpp – 2.5Vpp, and the recommended value is 1.3Vpp, XTALN single-ended input. When single-ended input, please connect a 0.1 uF capacitor in series to the XTALN input terminal; XTALP is recommended to connect a capacitor in series to the ground. The recommended circuit is as follows:

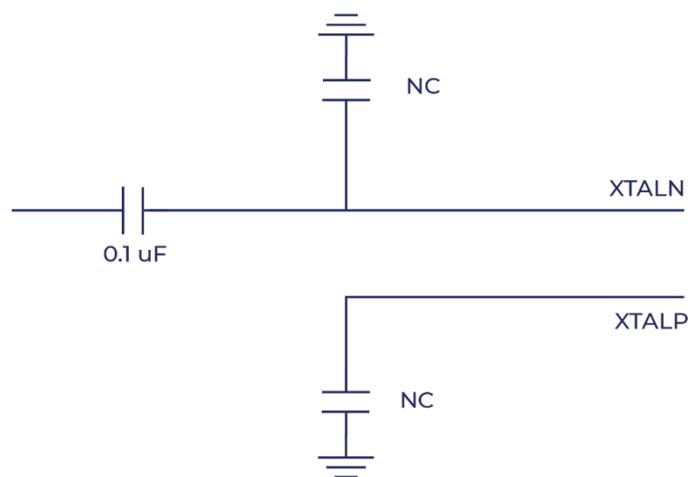


Figure 32.

The reference clock can be provided by two different clock sources. The first option is to use a dedicated crystal with a frequency between 7.68 MHz and 122.88 MHz, typically connected between the XTALP and XTALN pins. The second option is to connect an external oscillator or clock distribution device, typically connected to the XTALN pin (with the XTALP pin left disconnected). If an external oscillator is used, the frequency can vary between 7.68 MHz and 122.88 MHz.

This reference clock is used to power the frequency synthesizer blocks that generate all data clocks, sampling clocks, and local oscillators within the device. Crystal frequency errors can be eliminated by adjusting the on-chip variable capacitor using the digitally programmable, digitally controlled crystal oscillator (DCXO) feature. This capacitor can tune out crystal frequency variations in the system, resulting in a more accurate reference clock from which all other frequencies are generated. This feature can also be used in conjunction with the on-chip temperature sensing feature to provide temperature compensation of the oscillator frequency during normal operation.

## Frequency Synthesizer

### RF PLL

The TGS9364 contains two identical frequency synthesizers to generate the required LO signals for the RF signal path: one for the receiver and one for the transmitter, and the transmit one can be switched for receive use. The phase-locked loop (PLL) frequency synthesizer is a fractional-N design that incorporates a fully integrated voltage-controlled oscillator (VCO) and loop filter. In TDD mode of operation, the frequency synthesizer is turned on and off as needed for the RX and TX frames. In FDD mode, the TX PLL and RX PLL can be activated simultaneously. These PLLs require no external components.

### BB PLL

The TGS9364 also contains a baseband PLL frequency synthesizer that is used to generate all baseband related clock signals. These include the ADC and DAC sampling clocks, the DATA\_CLK signal, and all data framing signals. The PLL can be programmed to operate in the range of 1600 MHz to 3600 MHz, depending on the data rate and sampling rate requirements of the system.

## Digital Data Interface

The TGS9364 data interface uses parallel data ports (P0 and P1) to transfer data between the device and the BBP. The data port can be configured as a single-ended CMOS format or a differential LVDS format. Both formats can be configured in a variety of ways to meet system requirements for data sorting and data port connections. Specifically, single-port data bus, dual-port data bus, single data rate, dual data rate, and various data sorting combinations are included to pass data from different channels through the bus at the appropriate time.

The bus transfer is controlled by simple hardware handshake signaling. The two ports can operate in bidirectional (TDD) mode or full-duplex (FDD) mode, in which half the number of bits is used to

transmit data and half is used to receive data.

The interface can also be configured to use only one of the data ports for applications that do not require high data rates and prefer to use fewer interface pins.

### DATA\_CLK signal

The RX data provides the DATA\_CLK signal, which the BBP can use when receiving data. DATA\_CLK can be set to a rate that provides single data rate (SDR) timing, where data is sampled on each rising clock edge, or double data rate (DDR) timing, where data is captured on both rising and falling edges. This timing is applicable to operating modes using either a single port or two ports.

### FB\_CLK signal

For transmit data, the interface uses the FB\_CLK signal as the timing reference. For burst control signals, FB\_CLK allows the source to be synchronized with the rising edge capture timing, and for transmit signal bursts, it allows synchronization with the rising edge (SDR mode) or dual edge capture (DDR mode). The FB\_CLK signal must have the same frequency and duty cycle as DATA\_CLK.

### RX\_FRAME signal

The device generates an RX\_FRAME input signal whenever the receiver outputs valid data. This signal has two modes: level mode (RX\_FRAME remains high while the data is valid) and pulse mode (RX\_FRAME pulses with a 50% duty cycle). Similarly, the BBP must provide a TX\_FRAME signal with a rising edge to indicate the start of valid data transmission. Similar to RX\_FRAME, the TX\_FRAME signal may remain high throughout the burst, or it may pulse with a 50% duty cycle.

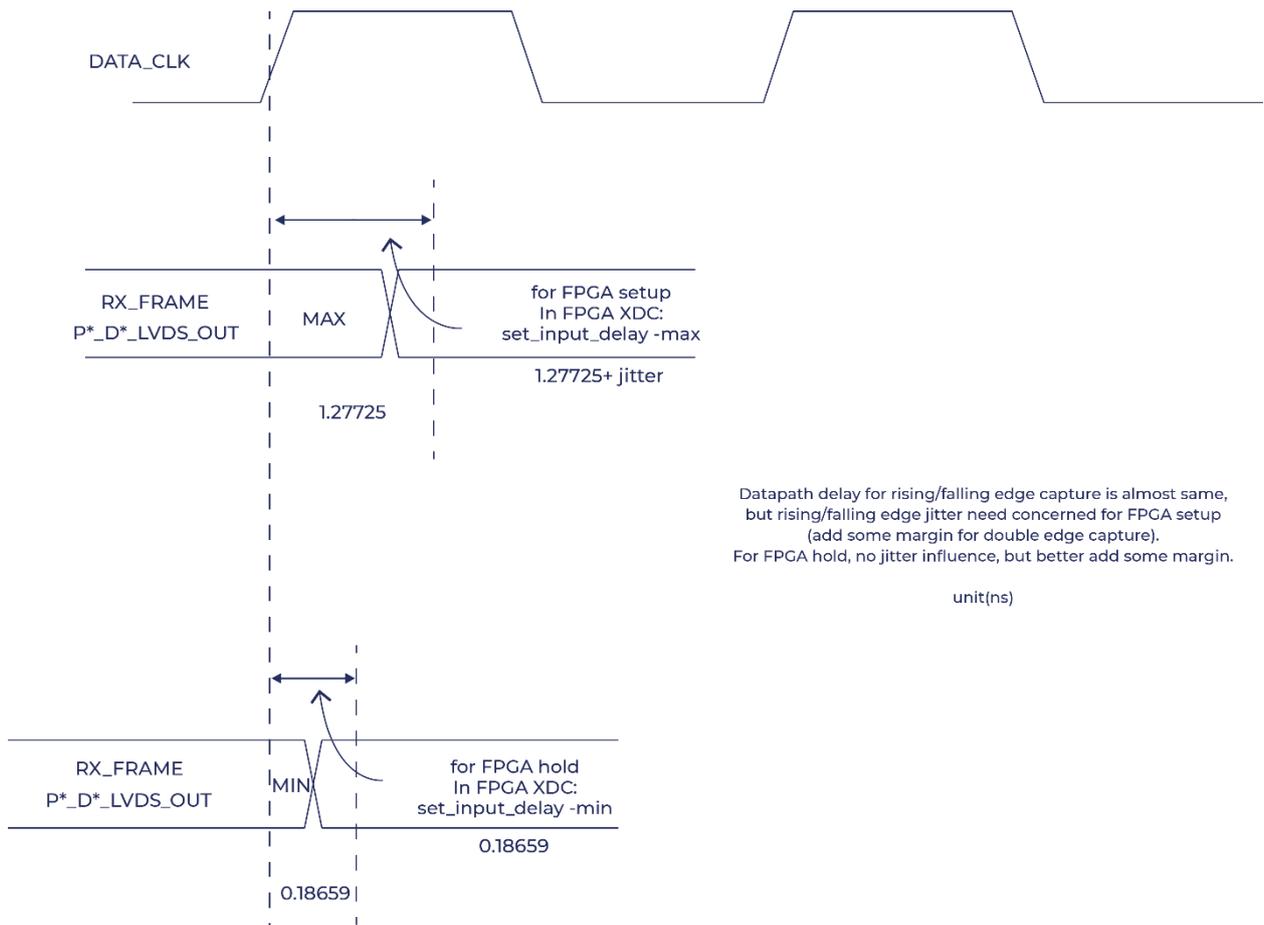


Figure 33. TGS9364 to FPGA timing

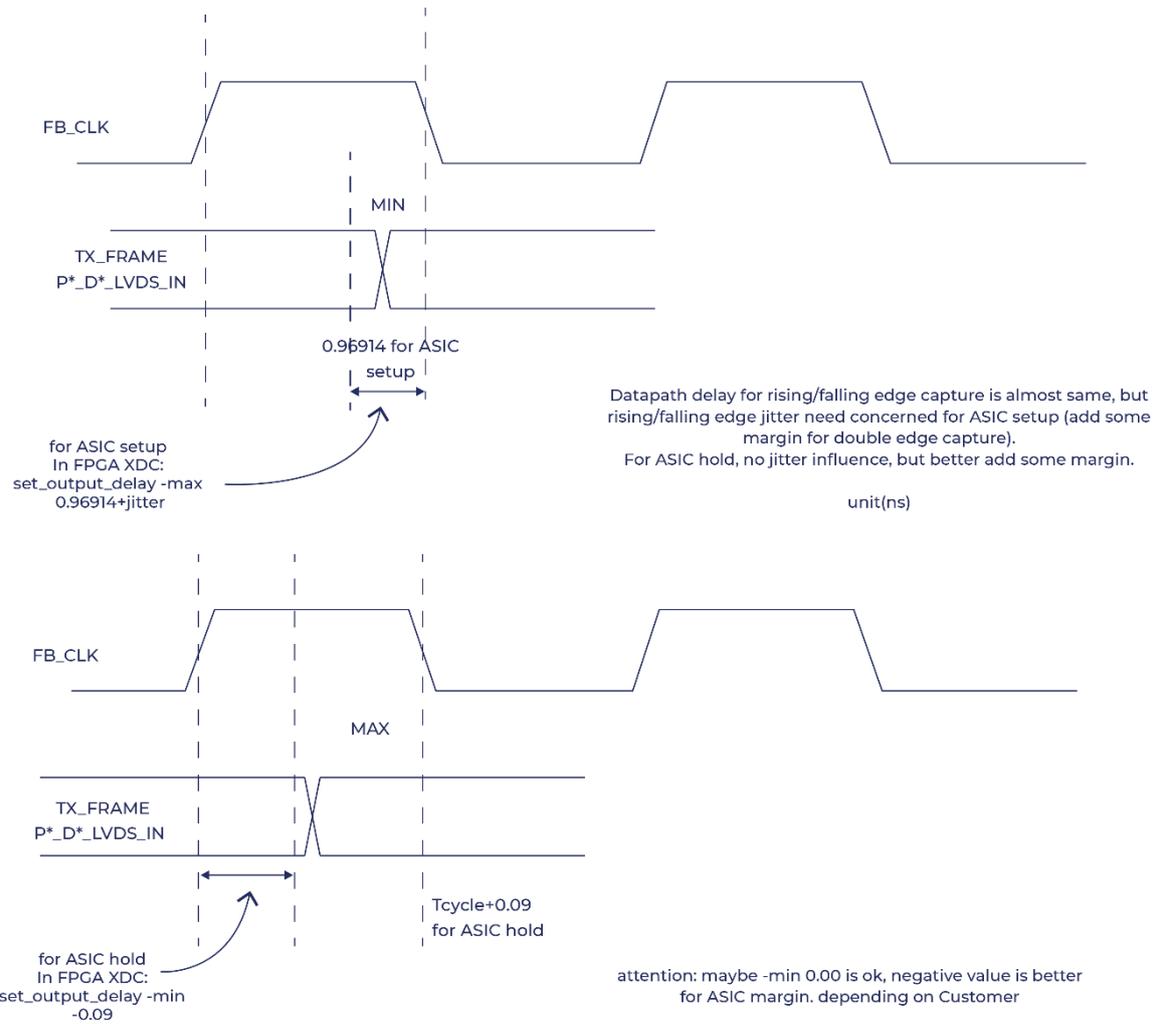


Figure 34. FPGA to TGS9364 timing

Parameter	Minimum value	Typical value	Maximum value	Unit
Logic input voltage range	825		1575	mV
Logic Input Differential Voltage Threshold	-100		100	mv
Receive differential input impedance		100		$\Omega$
Receive differential voltage range	100	350	600	mV
Logic input voltage			1375	mV
Logic input low voltage	1025			mV
Logic input differential voltage	150			mV
Logic input mode voltage		1200		mV

Table 13. LVDS parameter indicators

Parameter	Symbol	Minimum value	Typical value	Maximum value	Unit
DATA_CLK clock period	Tcp	4.069			ns
DATA_CLK and FB_CLK pulse bandwidth	Tmp	45%		55%	ns
TX data set up to FB_CLK	Tstx	1.25			ns
TX data is held until FB_CLK	Thtx	0			ns
DATA_CLK to data bus output delay	Tddrx	0.18		1.28	ns
DATA_CLK to RX_FRAME Delay	Tddrv	0.18		1.28	ns

Table 14. LVDS timing specifications

## Enabling State Machine

The TGS9364 transceiver includes an Enable State Machine (ENSM) that allows real-time control of the current state of the device. During normal operation, the device can be placed in a number of different states, including

- Standby — power saving, frequency synthesizer disabled
- Sleep — standby, all clock BB PLLs disabled
- TX — TX signal chain enabled
- RX — RX signal chain enabled
- FDD — TX and RX signal chains enabled
- Alarm — frequency synthesizer enabled

There are two possible control methods for the ENSM: SPI control and pin control.

### SPI Control Mode

In SPI control mode, asynchronous control of the ENSM is achieved by writing to the SPI registers to go from the current state to the next state. SPI control is considered asynchronous to DATA\_CLK because SPI\_CLK may be derived from a different reference clock and still function properly. The SPI control ENSM method is recommended when real-time control of the frequency synthesizer is not required. SPI control can be used for real-time control as long as the BBIC can accurately perform SPI write operations.

### Pin control mode

In pin control mode, the enable functions of the ENABLE pin and the TXNRX pin allow real-time control of the current state. ENSM supports TDD or FDD modes of operation, depending on the configuration of the corresponding SPI registers. If the BBIC has additional control inputs that can be controlled in real time, allowing a simple two-wire interface to control the device state, the ENABLE and TXNRX pin control method is recommended.

To change the current state of ENSM to the next state, the enable function of the ENABLE pin can be activated by a pulse (edge is detected internally) or level. When using a pulse, its minimum pulse width must be at least two FB\_CLK cycles. In level mode, the ENABLE and TXNRX pins are also detected by the TGS9364 for their edges and must meet the same minimum pulse width requirement, which is one FB\_CLK cycle. In FDD mode, the ENABLE and TXNRX pins must be remapped as real-time RX and TX data transmission control signals. In this mode, the ENABLE pin enables or disables the receive signal path, and the TXNRX pin enables or disables the transmit signal path. In this mode, the ENSM is removed from the system so that all data flow is controlled by these pins.

### SPI Interface

The TGS9364 communicates with the BBP via a Serial Peripheral Interface (SPI). This interface can be configured as a 4-wire interface with dedicated receive and transmit ports. This bus allows the BBP to set all device control parameters through a simple address data serial bus protocol. Write commands follow a 24-bit format. The first 4 bits are used to set the bus direction and the number of bytes to be transferred. The next 12 bits are the write address of the data. The last 8 bits are the data to be transferred to the specified register address (MSB to LSB).

The TGS9364 also supports LSB first format, allowing commands to be written in LSB to MSB format. In this mode, the register address will increment for multi-byte write commands. Read commands follow a similar format, except that the first 16 bits are transmitted on the SPI\_DI pin and the last 8 bits are read from the TGS9364, if in 4-wire mode, on the SPI\_DO pin.

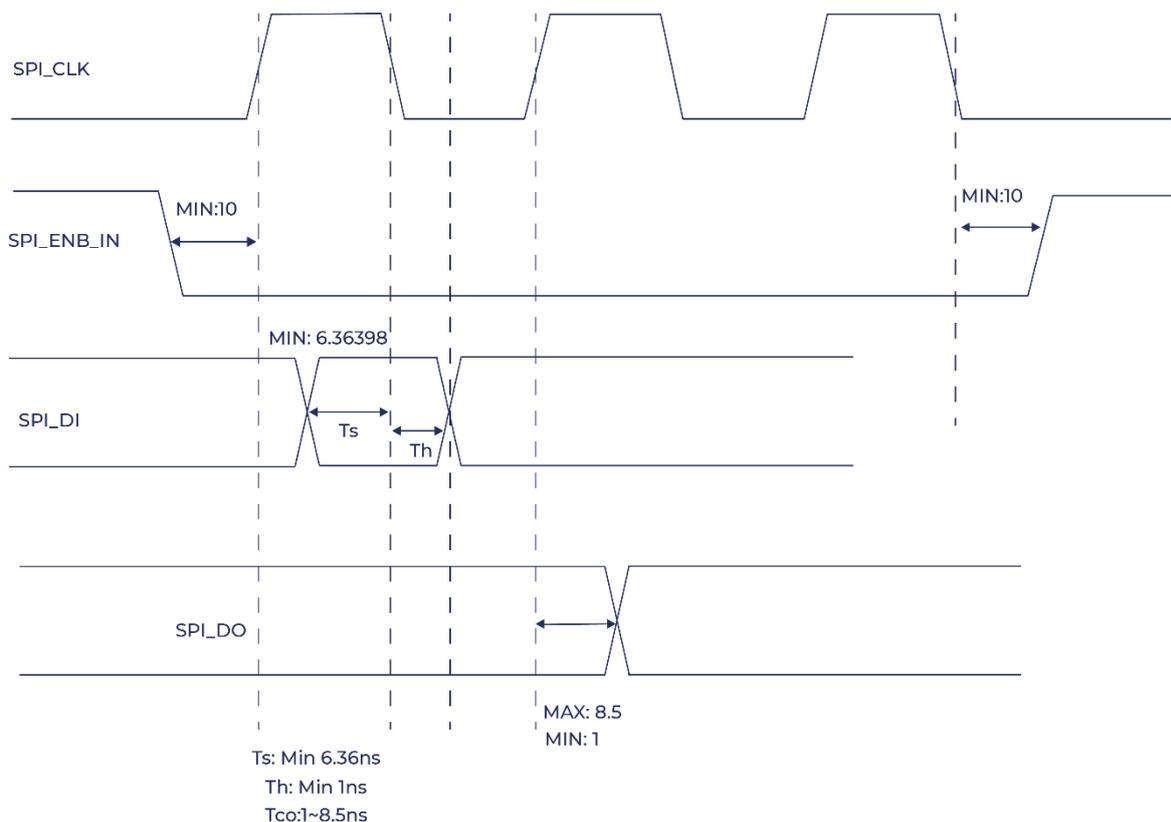


Figure 35. SPI Timing

	Minimum value	Typical value	Maximum value	Unit
High level	VDD_INTERFACE*0.9		VDD_INTERFACE	V
Low level	0		VDD_INTERFACE*0.1	V
SPI_CLK period		40		ns
SPI_CLK pulse width	25			ns
SPI_CLK Rising transition:	0		4	ns
SPI_CLK Falling transition:	0		4	ns
SPI_ENB is set to the first SPI_CLK rising edge	10			ns
Last SPI_CLK falling edge to SPI_ENB hold	10			ns

Table 15. SPI Timing

## General Control Pins

### Control input (CTRL\_OUT [7:0])

The TGS9364 provides eight synchronous real-time input signals that serve as interrupts to the BBP. These inputs can be configured to output some of the internal settings and measurements that the BBP can use when monitoring the performance of the transceiver under different circumstances. The control input pointer register selects what information is output to these pins, while the control input enable register determines which signals the BBP will activate for monitoring. Signals for manual gain mode, calibration flags, state machine status, and ADC inputs are some of the inputs that can be monitored on these pins.

### Control input (CTRL\_IN [3:0])

The TGS9364 provides 4 edge detection control input pins. In manual gain mode, the BBP can use these pins to change the gain table index in real time. In transmit mode, the BBP can use two of these pins to change the transmit gain in real time.

### GPO pins (GPO\_3 to GPO\_0)

The TGS9364 provides four 3.3 V-capable general-purpose logic input pins: GPO\_3, GPO\_2, GPO\_1, and GPO\_0. These pins can be used to control other peripheral devices such as regulators, switches, etc. through the TGS9364 SPI bus, or they can act as slaves to the internal TGS9364 state machine.

### Auxiliary Converter AUXADC

The TGS9364 contains two auxiliary ADCs that can be used to monitor system functions such as temperature and power input. The converter is 12 bits wide and has an input range of 0 V to 1 V. When enabled, the ADC is in a free-running state. The SPI read operation provides the last value latched at the ADC input. With a multiplexer located before the ADC, the user can select between the AUXADC input pin and the built-in temperature sensor. The AUXADC cannot be used during initialization or calibration, or when doing RX peak detection, but can be used at other times;

### Power Supply of TGS9364

The TGS9364 must be powered by three power supplies: analog power (VDDD1P3\_DIG/VDDAx = 1.3 V), interface power (VDD\_INTERFACE = 1.8 V or 2.5 V), and GPO power (VDD\_GPO = 3.3 V). For applications that require optimized noise performance, it is recommended to separate and provide the 1.3 V power supply with a low-noise, low-dropout (LDO) regulator.

For applications where board space is a premium and optimal noise performance is not an absolute requirement, the 1.3 V module rail can be provided directly by a switch and a more integrated power management unit (PMU) can be employed.

## 8. Ordering Information

Product model	Package form	Packaging	Minimum Order Quantity
TGS9364	TFBGA-144 10*10	Tray	240