Tegsemi

TGS9361

SDR transceiver

Data sheet

Product Applications and Scope

- Point-to-Point Communication Systems
- Microcell Base Stations
- General Radio Systems

Standard

- Quality Grade / Quality Assurance Requirements: Controlled according to Level N1 specified in the trial version of the "Assessment and Evaluation Plan for Military Plastic-Encapsulated Integrated Circuits."

Product Features

- Analog Power Supply Voltage: 3.3 V, 1.8 V, 1.3 V
- Digital Power Supply Voltage: 1.3 V
- RF 2×2 Transceiver Integrated with 12-bit DAC and ADC
- Frequency Range: 70 MHz to 6.0 GHz
- Supports TDD and FDD
- Tunable Channel Bandwidth: < 200 kHz to 56 MHz
- TX EVM: −40 dB
- Circuit Interface: CMOS/LVDS Digital Interface
- ESD Rating: HBM 500 V
- Weight: 0.32 g ± 0.02 g

Product Description

The TGS9361 is a high-performance, highly integrated radio frequency (RF) agile transceiver designed for 3G and 4G base station applications. Its programmability and wideband capability make it an ideal choice for various transceiver applications. The device integrates an RF front end with a flexible mixed-signal baseband section, incorporates frequency synthesizers, and provides a configurable digital interface to the processor, thereby simplifying design integration.

The TGS9361 operates over a frequency range of 70 MHz to 6.0 GHz, covering most licensed and unlicensed frequency bands, and supports channel bandwidths from less than 200 kHz up to 56 MHz. Two independents direct- conversion receivers deliver industry-leading noise figure and linearity. Each receive (RX) subsystem features independent automatic gain control (AGC), DC offset correction, quadrature correction, and digital filtering, eliminating the need for these functions in the digital

baseband. The TGS9361 also offers a flexible manual gain mode, supporting external control.

Each channel is equipped with two high-dynamic-range ADCs that digitize the received I and Q signals, which are then passed through configurable decimation filters and a 128-tap finite impulse response (FIR) filter, producing a 12-bit output signal at the corresponding sample rate

The transmitter employs a direct-conversion architecture, achieving high modulation accuracy and ultra-low noise. This transmitter design results in low TX EVM, measuring < −40 dB, providing substantial system margin for external power amplifier selection. The on-board transmit (TX) power monitor can function as a power detector, enabling highly accurate TX power measurements.
Fully integrated phase-locked loop (PLL) provides low-power fractional-N frequency synthesis for all receive and transmit channels. Channel isolation required for frequency division duplex (FDD) systems is integrated into the design. All VCO and loop filter components are also integrated

The circuit adopts a 10 mm × 10 mm, 144-pin chip-scale ball grid array (CSP_BGA) package. This product serves as an effective alternative to Analog Devices Inc.'s AD9361.

The functional block diagram of the product is as follows:

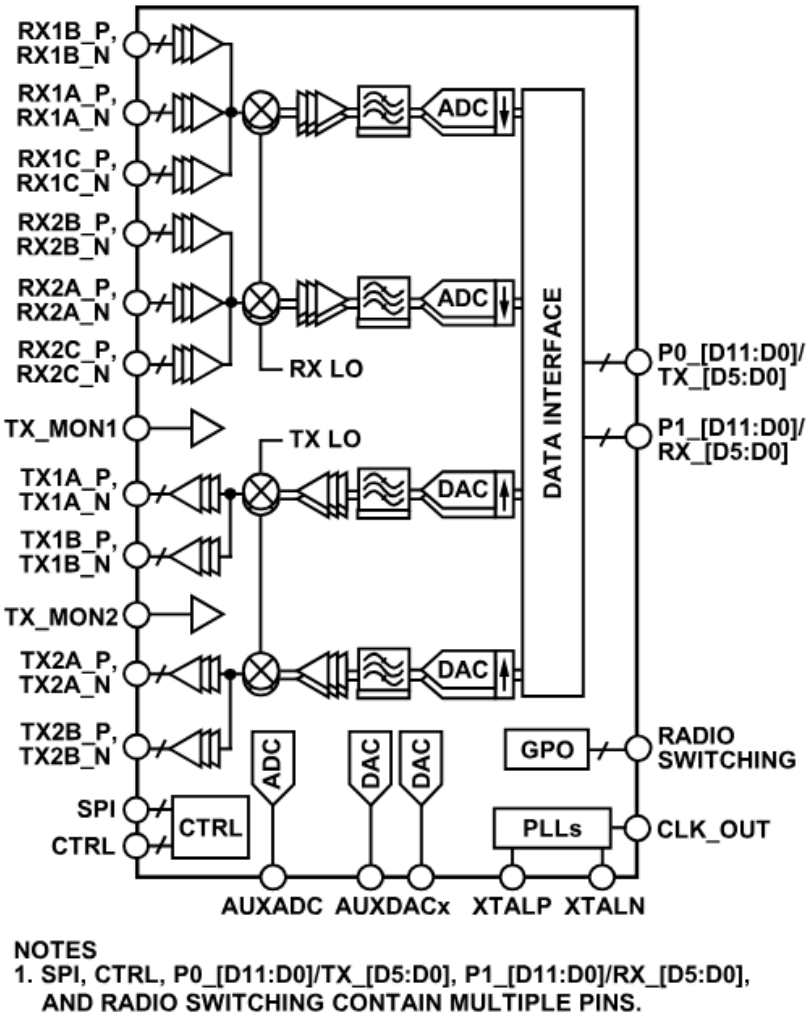


Figure 1. Functional Block Diagram

Precautions:

1) RX and TX Baseband Bandwidth Calibration

The clock for baseband bandwidth calibration is derived by dividing the main clock. The division factor for RX is determined by Reg1F8 [7:0] (BBF Tune Divide), and for TX by Reg0D6 [7:0]. This division factor must not be an odd number, meaning Reg1F8 [0] and Reg0D6 [0] cannot be set to 1.

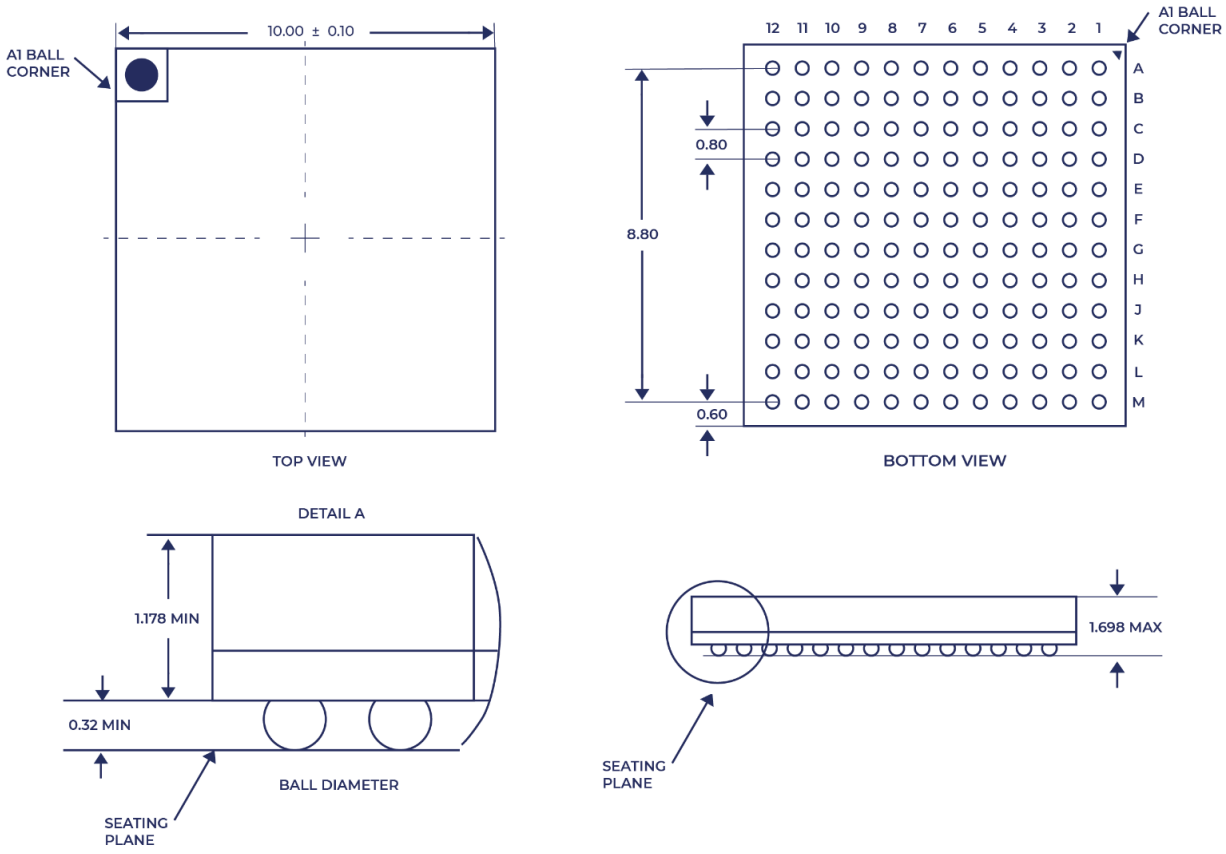
The division factor is determined by the BBPLL frequency and the baseband bandwidth, calculated as follows:

BBF Tune Divide [8:0] = ceil((BBPLL Freq*ln(2))/(BBBW*1.4*2*π))

There are two methods to avoid this issue:

1) After initialization, verify the values of these two registers. If either value is 1, adjust the baseband bandwidth and reinitialize the chip. Since changes in baseband bandwidth will alter the division ratio, this method can convert an erroneous odd division ratio into an even one, thereby avoiding the issue.
2) If it is possible to modify the register values during the initialization process, directly set Reg1F8[0] and Reg0D6[0] to 0 before initializing the chip. This will also prevent the problem from occurring.

Product Outline and Physical Images



Unit: Millimeter (mm)

Figure 2. Product outline dimension drawing

Pinout Arrangement (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	RX2A_N	RX2A_P	NC	VSSA	TX_MON2	VSSA	TX2A_N	TX2A_P	TX2B_N	TX2B_P	VDDA1P1_TX_VCO	TX_EXT_LO_IN
B	VSSA	VSSA	AUXDAC1	GPO_3	GPO_2	GPO_1	GPO_0	VDD_GPO	VDDA1P3_TX_LO	VDDA1P3_TX_VCO_LDO	TX_VCO_LDO_OUT	VSSA
C	RX2C_P	VSSA	AUXDAC2	TEST/ENABLE	CTRL_IN0	CTRL_IN1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
D	RX2C_N	VDDA1P3_RX_RF	VDDA1P3_RX_TX	CTRL_OUT0	CTRL_IN3	CTRL_IN2	P0_D9/TX_D4_P	P0_D7/TX_D3_P	P0_D5/TX_D2_P	P0_D3/TX_D1_P	P0_D1/TX_D0_P	VSSD
E	RX2B_P	VDDA1P3_RX_LO	VDDA1P3_TX_LO_BUFFER	CTRL_OUT1	CTRL_OUT2	CTRL_OUT3	P0_D11/TX_D5_P	P0_D8/TX_D4_N	P0_D6/TX_D3_N	P0_D4/TX_D2_N	P0_D2/TX_D1_N	P0_D0/TX_D0_N
F	RX2B_N	VDDA1P3_RX_VCO_LDO	VSSA	CTRL_OUT6	CTRL_OUT5	CTRL_OUT4	VSSD	P0_D10/TX_D5_N	VSSD	FB_CLK_P	VSSD	VDDD1P3_DIG
G	RX_EXT_LO_IN	RX_VCO_LDO_OUT	VDDA1P1_RX_VCO	CTRL_OUT7	EN_AGC	ENABLE	RX_FRAME_N	RX_FRAME_P	TX_FRAME_P	FB_CLK_N	DATA_CLK_P	VSSD
H	RX1B_P	VSSA	VSSA	TXNRX	SYNC_IN	VSSA	VSSD	P1_D11/RX_D5_P	TX_FRAME_N	VSSD	DATA_CLK_N	VDD_INTERFACE
J	RX1B_N	VSSA	VDDA1P3_RX_SYNTH	SPI_DI	SPI_CLK	CLK_OUT	P1_D10/RX_D5_N	P1_D9/RX_D4_P	P1_D7/RX_D3_P	P1_D5/RX_D2_P	P1_D3/RX_D1_P	P1_D1/RX_D0_P
K	RX1C_P	VSSA	VDDA1P3_TX_SYNT	VDDA1P3_BB	RESETB	SPI_ENB	P1_D8/RX_D4_N	P1_D6/RX_D3_N	P1_D4/RX_D2_N	P1_D2/RX_D1_N	P1_D0/RX_D0_N	VSSD
L	RX1C_N	VSSA	VSSA	RBIAS	AUXADC	SPI_DO	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
M	RX1A_P	RX1A_N	NC	VSSA	TX_MON1	VSSA	TX1A_P	TX1A_N	TX1B_P	TX1B_N	XTALP	XTALN

GROUND | NO CONNECT | DC POWER | DIGITAL I/O | ANALOG I/O

Figure 3. Pinout Arrangement

Pin Function Symbol Table

Pin Number	Type [1]	Pin Name	Description
A1, A2	I	RX2A_N, RX2A_P	Channel 2 Differential Input A (Receive). Alternatively, each pin can serve as a single-ended input or be combined to form a differential pair. Connect unused pins to ground.
A3, M3	NC	NC	No Connect. Do not connect to these pins.
A4, A6, B1, B12, C2, C7, C12, F3, H2, H3, H6, J2, L2, L3, L7 to L12, M4, M6	I	VSSA	Analog Ground. Connect these pins directly to the VSSD digital ground (i.e., a ground plane) on the printed circuit board.
A5	I	TX_MON2	Channel 2 Power Monitoring Input (Transmit). If unused, connect this pin to ground.
A7, A8	O	TX2A_N, TX2A_P	Channel 2 Differential Output A (Transmit). Connect unused pins to 1.3 V.
A9, A10	O	TX2B_N, TX2B_P	Channel 2 Differential Output B (Transmit). Connect unused pins to 1.3 V.
A11	I	VDDA1P1_TX_VCO	Transmit VCO Power Supply Input. Connect to B11.
A12	I	TX_EXT_LO_IN	External Transmit LO Input. If unused, connect this pin to ground.
B3	O	AUXDAC1	Auxiliary DAC 1 Output.
B4 to B7	O	GPO_3 to GPO_0	General-Purpose Output supporting 3.3 V.
B8	I	VDD_GPO	Power Supply for AUXDAC and General-Purpose Output pins (2.5 V to 3.3 V). When not using the VDD_GPO supply, it must be set to 1.3 V.
B9	I	VDDA1P3_TX_LO	Transmit LO 1.3 V Power Supply Input.
B10	I	VDDA1P3_TX_VCO_LDO	Transmit VCO LDO 1.3 V Power Supply Input. Connect to B9.
B11	O	TX_VCO_LDO_OUT	Transmit VCO LDO Output. Connect to A11, with a 1 µF bypass capacitor in series with a 1 Ω resistor connected to ground.
C1, D1	I	RX2C_P, RX2C_N	Channel 2 Differential Input C (Receive). Each pin can serve as a single-ended input or be combined to form a differential pair. Performance of these inputs degrades above 3 GHz. Connect unused pins to ground.
C3	O	AUXDAC2	Auxiliary DAC 2 Output.
C4	I	Test / Enable	Test Input. Under normal operation, connect this pin to ground.
C5, C6, D5	I	CTRL_IN0 to CTRL_IN3	Control Input. Used for manual RX gain and TX attenuation control.
D2	I	VDDA1P3_RX_RF	Receiver 1.3 V Power Supply Input. Connect to D3.
D3	I	VDDA1P3_RX_TX	1.3 V Power Supply Input.
D4, E4 to F4 to F6	O	CTRL_OUT0，CTRL_OUT3, CTRL_OUT4	Control Output. These pins are multifunctional outputs with programmable features.
D7	I/O	P0_D9/TX_D4_P	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D9, it acts as part of a 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D4_P) can also act as part of an LVDS 6-bit TX differential input bus (with internal LVDS terminals).
D8	I/O	P0_D7/TX_D3_P	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D7, it acts as part of a 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D3_P) can also act as part of an LVDS 6-bit TX differential input bus (with internal LVDS terminals).
D9	I/O	P0_D5/TX_D2_P	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D5, it acts as part of a 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D2_P) can also be part of an LVDS 6-bit TX differential input bus (with internal LVDS terminals).
D10	I/O	P0_D3/TX_D1_P	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D3, it acts as part of a 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D1_P) can also be part of an LVDS 6-bit TX differential input bus (with internal LVDS terminals).

D11	I/O	P0_D1/TX_D0_P	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D1, it acts as part of a 12-bit bidirectional parallel CMOS level data port 0. Alternatively, this pin (TX_D0_P) can also be part of an LVDS 6-bit TX differential input bus (with internal LVDS terminals).
D12, F7, F9, F11, G12, H10, K12	I	VSSD	Digital Ground. Connect these pins directly to the VSSA analog ground (i.e., a ground plane) on the printed circuit board.
E1, F1	I	RX2B_P, RX2B_N	Channel 2 Differential Input B (Receive). Each pin can serve as a single-ended input or be combined to form a differential pair. Performance of these inputs degrades above 3 GHz. Connect unused pins to the ground.
E2	I	VDDA1P3_RX_LO	Receive LO 1.3 V Power Supply Input.
E3	I	VDDA1P3_TX_LO_BUFFE	1.3 V Power Supply Input.
E7	I/O	P0_D11/TX_D5_P	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D11, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D5_P) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
E8	I/O	P0_D8/TX_D4_N	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D8, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D4_N) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
E9	I/O	P0_D6/TX_D3_N	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D6, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D3_N) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
E10	I/O	P0_D4/TX_D2_N	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D4, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D2_N) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
E11	I/O	P0_D2/TX_D1_N	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D2, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D1_N) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
E12	I/O	P0_D0/TX_D0_N	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D0, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D0_N) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
F2	I	VDDA1P3_RX_VCO_LDO	Receive VCO LDO 1.3 V Power Supply Input. Connect to E2.
F8	I/O	P0_D10/TX_D5_N	Digital Data Port P0 / Transmit Differential Input Bus. This is a dual-function pin. For P0_D10, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 0. Alternatively, this pin (TX_D5_N) can also function as part of the LVDS 6-bit TX differential input bus (with internal LVDS termination).
F10, G10	I	FB_CLK_P, FB_CLK_N	Feedback Clock. These pins receive the FB_CLK signal as the TX data clock. In CMOS mode, use FB_CLK_P as input and connect FB_CLK_N to ground.
F12	I	VDDD1P3_DIG	1.3 V Digital Power Supply Input.
G1	I	RX_EXT_LO_IN	External Receive LO Input. If unused, connect this pin to ground.
G2	O	RX_VCO_LDO_OUT	Receive VCO LDO Output. Connect this pin directly to G3, with a 1 μF bypass capacitor in series with a 1 Ω resistor connected to ground.
G3	I	VDDA1P1_RX_VCO	Receive VCO Power Supply Input. Connect this pin directly to G2 only.
G5	I	EN_AGC	Manual Control Input for Automatic Gain Control (AGC).
G6	I	Enable	Control Input. This pin enables the device to transition between various operating states.
G7, G8	O	RX_FRAME_N, RX_FRAME_P	Receive Digital Data Frame Output Signal. These pins transmit the RX_FRAME signal to indicate whether the RX output data is valid. In CMOS mode, use RX_FRAME_P as the output and leave

			RX_FRAME_N disconnected.
G9, H9	I	TX_FRAME_P, TX_FRAME_N	Transmit Digital Data Frame Input Signal. These pins receive the TX_FRAME signal, which indicates when TX dat is valid. In CMOS mode, use TX_FRAME_P as the input and connect TX_FRAME_N to ground.
G11, H11	O	DATA_CLK_P, DATA_CLK_N	Receive Data Clock Output. These pins output the DATA_CLK signal, which the baseband processor (BBP) use to clock the RX data. In CMOS mode, use DATA_CLK_P as the output and leave DATA_CLK_N disconnected.
H1, J1	I	RX1B_P, RX1B_N	Channel 1 Differential Input B (Receive). Alternatively, each pin can be used as a single-ended input. Performance of these inputs degrades above 3 GHz. Connect unused pins to ground.
H4	I	TXNRX	Enable State Machine Control Signal. This pin controls the data port bus direction. A logic low level selects the RX direction, while a logic high level selects the TX direction.
H5	I	SYNC_IN	Input for Synchronizing Digital Clocks Across Multiple TGS9361 Devices. If unused, connect this pin to ground.
H8	I/O	P1_D11/RX_D5_P	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D11, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D5_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
H12	I	VDD_INTERFACE	Digital I/O pins, power supply from 1.2 V to 2.5 V (1.8 V to 2.5 V in LVDS mode).
J3	I	VDDA1P3_RX_SYNTH	1.3 V power supply input.
J4	I	SPI_DI	SPI serial data input.
J5	I	SPI_CLK	SPI clock input.
J6	O	CLK_OUT	Output clock. This pin can be configured to output either a buffered version of the external input clock (DCXO) or a divided version of the internal ADC_CLK.
J7	I/O	P1_D10/RX_D5_N	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D10, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D5_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
J8	I/O	P1_D9/RX_D4_P	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D9, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D4_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
J9	I/O	P1_D7/RX_D3_P	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D7, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D3_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
J10	I/O	P1_D5/RX_D2_P	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D5, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D2_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
J11	I/O	P1_D3/RX_D1_P	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D3, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D1_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
J12	I/O	P1_D1/RX_D0_P	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D3, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D1_P) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
K1, L1	I	RX1C_P, RX1C_N	Channel 1 Differential Input C (Receive). Alternatively, each pin can be used as a single-ended input. Performance of these inputs degrades above 3 GHz. Connect unused pins to ground.
K3	I	VDDA1P3_TX_SYNTH	1.3 V Power Supply Input.
K4	I	VDDA1P3_BB	1.3 V Power Supply Input.
K5	I	RESETB	Asynchronous Reset. A logic low level resets the device.

K6	I	SPI_ENB	SPI Enable Input. Set this pin to a logic low level to enable the SPI bus.
K7	I/O	P1_D8/RX_D4_N	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D8, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D4_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
K8	I/O	P1_D6/RX_D3_N	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D6, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D3_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
K9	I/O	P1_D4/RX_D2_N	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D4, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D2_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
K10	I/O	P1_D2/RX_D1_N	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D2, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D1_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
K11	I/O	P1_D0/RX_D0_N	Digital Data Port P1 / Receive Differential Output Bus. This is a dual-function pin. For P1_D0, it serves as part of the 12-bit bidirectional parallel CMOS-level Data Port 1. Alternatively, this pin (RX_D0_N) can also function as part of the LVDS 6-bit RX differential output bus (with internal LVDS termination).
L4	I	RBIAS	Bias Input Reference. Connect this pin to ground through a 14.3 kΩ resistor (1% tolerance).
L5	I	AUXADC	Auxiliary ADC Input. If unused, connect this pin to ground.
L6	O	SPI_DO	SPI Serial Data Output in 4-wire mode, or High-Z in 3-wire mode.
M1, M2	I	RX1A_P, RX1A_N	Channel 1 Differential Input A (Receive). Alternatively, each pin can be used as a single-ended input. Connect unused pins to ground.
M5	I	TX_MON1	Channel 1 Power Monitor Input (Transmit). If unused, connect this pin to ground.
M7, M8	O	TX1A_P, TX1A_N	Channel 1 Differential Output A (Transmit). Connect unused pins to 1.3 V.
M9, M10	O	TX1B_P, TX1B_N	Channel 1 Differential Output B (Transmit). Connect unused pins to 1.3 V.
M11, M12	I	XTALP, XTALN	Reference Frequency Crystal Oscillator Connection. When using a crystal oscillator, connect it between these two pins. When using an external clock source, connect it to XTALN and leave XTALP disconnected.

[1] I = Input, O = Output, I/O = Input/Output, NC = No Connect.

Recommended Operating Conditions

- VDD_GPO = 3.3 V
- VDD_INTERFACE = 1.8 V
- All other VDDx pins = 1.3 V
- Temperature: 25°C
- Input reference clock: 40 MHz

Absolute Maximum Ratings

Parameter	Absolute Maximum Ratings
VDDx to VSSx	−0.3 V to +1.4 V
VDD_INTERFACE to VSSx	−0.3 V to +3.0 V
VDD_GPO to VSSx	−0.3 V to +3.9 V
Logic input/output to VSSx	−0.3 V to VDD_INTERFACE+
Input current to any pin except supply pins	±10 mA
RF input (peak power)	2.5 dBm
TX monitor input power (peak)	9 dBm
Package power dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Maximum junction temperature (T_{JMAX})	110°C
Operating temperature range	−40°C to +85°C

Note:

Storage Temperature Range: -65°C to +150°C. Exceeding the above absolute maximum ratings may cause permanent damage to the device.

These ratings are stress limits only and do not imply that the device will function properly under these or any other conditions exceeding the operational specifications indicated in this technical manual. Continuous operation under absolute maximum rating conditions may affect the reliability of the device.

Specifications

Table 1.

Parameter [1]	Symbol	Min.	Typ.	Max.	Unit	Test conditions / comments
Receiver, general						
Center frequency		70		6000	MHz	
Gain						
Minimum value			0		dB	
Maximum value			71.5		dB	800 MHz
			70		dB	2300 MHz (RX1A, RX2A)
			70		dB	2300 MHz (RX1B, RX1C, RX2B, RX2C)
			62(testedoverseas62)		dB	5500 MHz (RX1A, RX2A)
Gain step			1		dB	
Received Signal Strength Indicator	RSSI					
Gear / Level			95		dB	
Accuracy			±2.5		dB	
Receiver, 800 MHz						
Noise figure	NF		2.8		dB	Maximum RX gain
Third-order input intercept point (IIP3)	IIP3		−11 (tested overseas 11)		dBm	Maximum RX gain
Second-order input intercept point (IIP2)	IIP2		−55 (tested overseas 57)		dBm	Maximum RX gain
Local oscillator (LO) leakage			−82 (tested overseas -82)		dBm	RX front-end input
Quadrature						
Gain error			0.2		%	
Phase error			0.2		degree	
Error vector magnitude (EVM)			(Not tested)		dB	19.2MHz reference clock
Input S_{11}			(Not tested)		dB	
RX1 toRX2 isolation						
RX1A to RX2A, RX1C to			68		dB	
RX1B to RX2B			55		dB	
RX2 to RX1 isolation						
RX2A to RX1A, RX2C to			68		dB	
RX2B to RX1B			55		dB	
Receiver, 2.4 GHz						
Noise figure	NF		3.5		dB	Maximum RX gain
Third-order input intercept point (IIP3)	IIP3		−10 (tested overseas -9)		dBm	Maximum RX gain
Second-order input intercept point (IIP2)	IIP2		48 (tested overseas 55)		dBm	Maximum RX gain
Local oscillator (LO) leakage			−82 (tested overseas-82)		dBm	Receiver front-end input
Quadrature						
Gain error			0.2		%	
Phase error			0.2		degree	
Error vector magnitude (EVM)			(Not tested)		dB	40 MHz reference clock
Input S_{11}			(Not tested)		dB	
RX1 to RX2 isolation						
RX1A to RX2A, RX1C to			55 (tested overseas 55)		dB	
RX1B toRX2B			50		dB	
RX2 to RX1 isolation						
RX2A to RX1A, RX2C to			55 (tested overseas 55)		dB	
RX2B to RX1B			50		dB	

Parameter[1]	Symbol	Min.	Typ.	Max.	Unit	Test conditions / comments
Receiver, 5.5 GHz						
Noise figure	NF		4		dB	Maximum RX gain
Third-order input intercept point (IIP3)	IIP3		−4 (tested overseas -26)		dm	Gain, maximum RX Gain, maximum
Second-order input intercept point (IIP2)	IIP2		58 (tested overseas 62)		dm	RX gain RX
Local oscillator (LO) leakage Quadrature			−75 (tested overseas -75)		dm	Front-end input
Gain error			0.2			
Phase error			0.2		%	
Error vector magnitude (EVM)			(Not tested)		Degree	
					dB	
Input S_{11}			(Not tested)		dB	40 MHz reference clock (for RF frequency synthesizer internal doubling)
RX1A to RX2A isolation			50		dB	
RX2A to RX1A isolation			37 (tested overseas 37)		dB	
Transmitter — General						
Center frequency		70		6000	MHz	
Power control range			90		dB	
Power control resolution			0.25		dB	
Transmitter, 800 MHz						
Output S_{22}			(Not tested)		dB	
Maximum output power			8		dBm	1 MHz tone (50 0 load)
Error vector magnitude (EVM)			-45		dB	19.2 MHz reference clock
Third-order output intercept point	OIP3		17 (tested overseas 17)		dBm	
Carrier leakage			−50		dBc	0 dB attenuation
			−40 (tested overseas -40)		dBc	40 dB attenuation
Noise floor			−148 (tested overseas -148)		dBm/Hz	90 MHz offset
Isolation						
TX1 to TX2			50		dB	
TX2 to TX1			50		dB	
Transmitter, 2.4 GHz						
Output S_{22}			(Not tested)		dB	
Maximum output power			7		dBm	1 MHz tone (50 0 load)
Error vector magnitude (EVM)			-40		dB	40 MHz reference clock
Third-order output intercept point	OIP3		17.5 (tested overseas 19)		dBm	
Carrier leakage			−50		dBc	0 dB attenuation
			−44		dBc	40 dB attenuation
Noise floor			−138 (tested overseas -138)		dBm/Hz	90 MHz offset
Isolation						
TX1 to TX2			50		dB	
TX2 to TX1			50		dB	
Transmitter, 5.5 GHz						
Output S_{22}			(Not tested)		dB	
Maximum output power			4.2 (tested overseas 3)		dBm	7 7 MHz tone (50 0 load)
Error vector magnitude (EVM)			-34.5		dB	40 MHz reference clock (for RF frequency synthesizer internal doubling)
Third-order output intercept point						
Carrier leakage	OIP3		13 (tested overseas 11)		dBm	
			−50		dBc	0 dB attenuation
			−42		dBc	40 dB attenuation
Noise floor			−137 (tested overseas -137)		dBm/Hz	90 MHz offset
Isolation						
TX1 to TX2			50		dB	
TX2 to TX1			50		dB	

Characteristic Curves (Electrical Performance Test Charts)

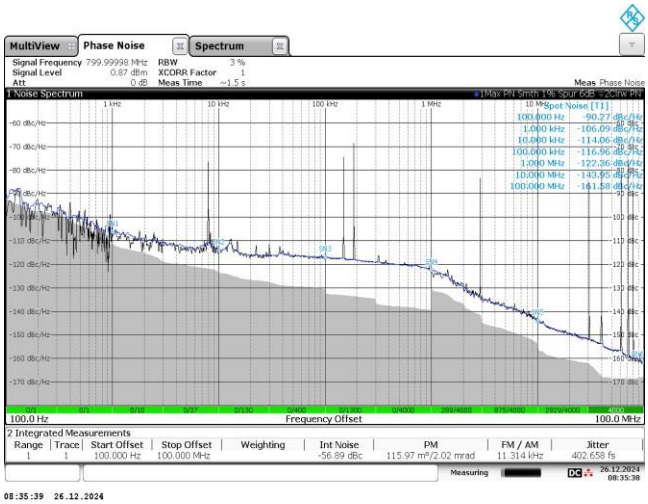


Figure 5. LO phase noise (800 MHz band)

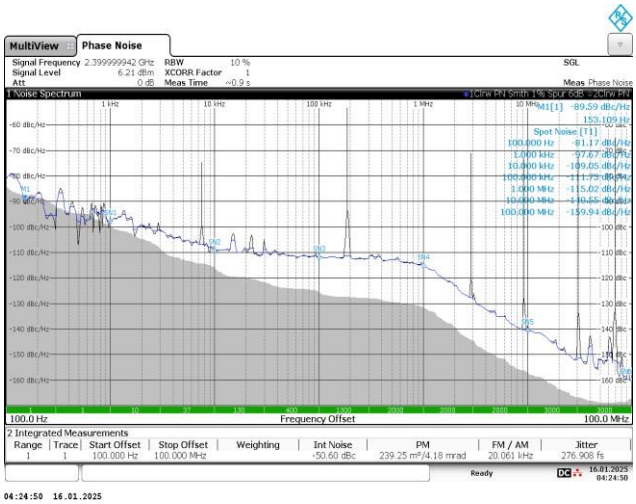


Figure 6. LO phase noise (2.4 GHz band)

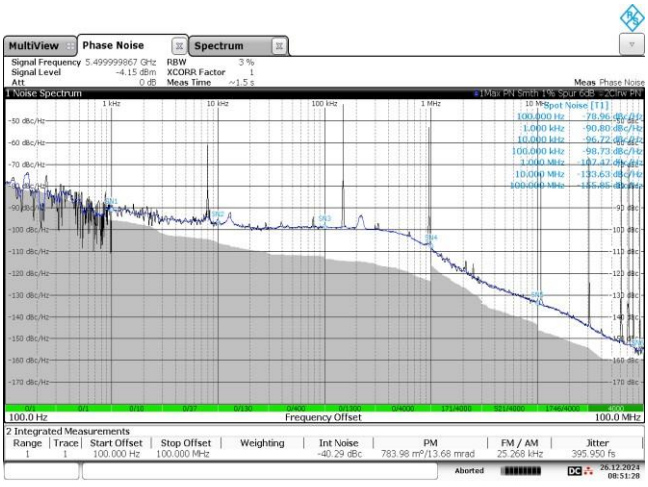


Figure 7. LO phase noise (5.5 GHz band)

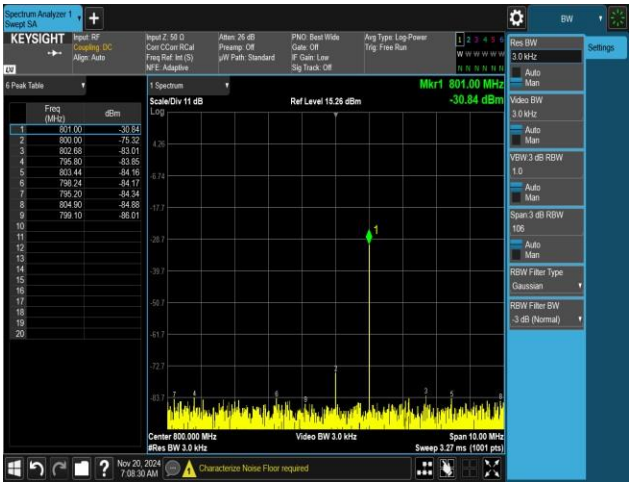


Figure 8. TX 40 dB attenuated output (800 MHz band)

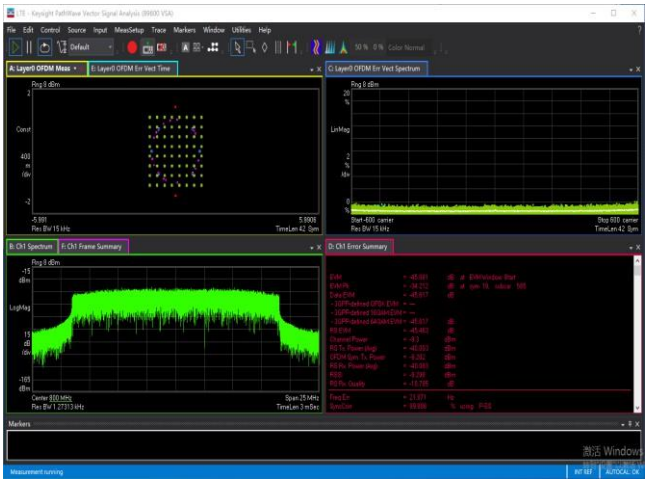


Figure 9. TX EVM (800 MHz band)

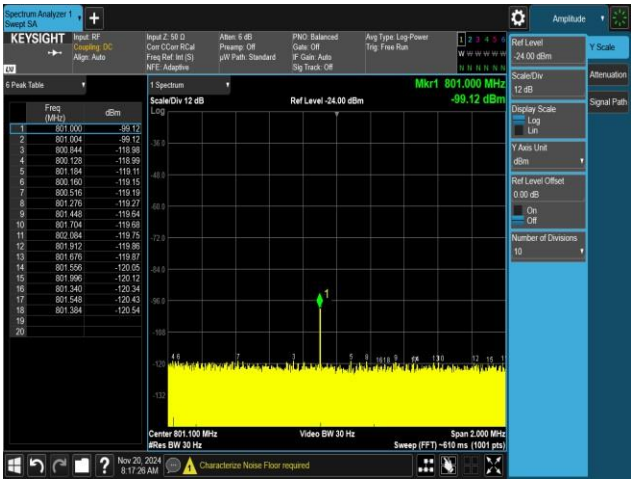


Figure 10. TX isolation (800 MHz band)

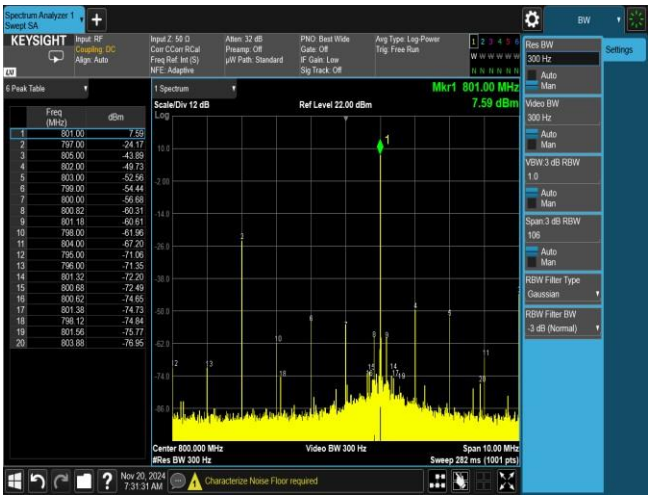


Figure 11. TX Max output (800 MHz band)

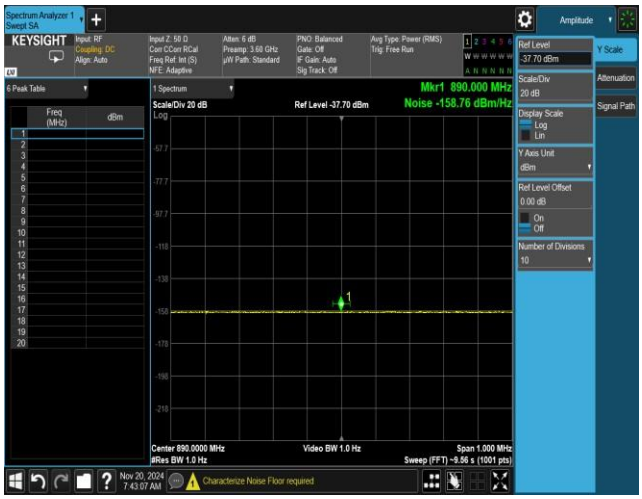


Figure 12. TX Noise Floor (800 MHz band)

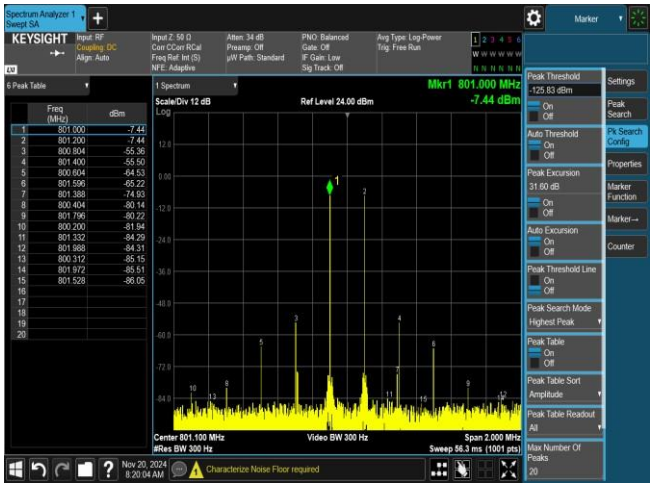


Figure 13. TX OIP3 (800 MHz band)

Figure 14. TX 40 dB attenuated output (2.4 GHz band)

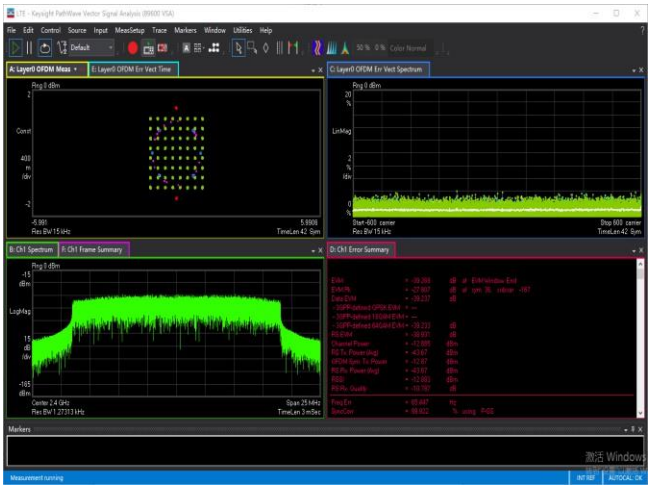


Figure 15. TX EVM (2.4 GHz band)

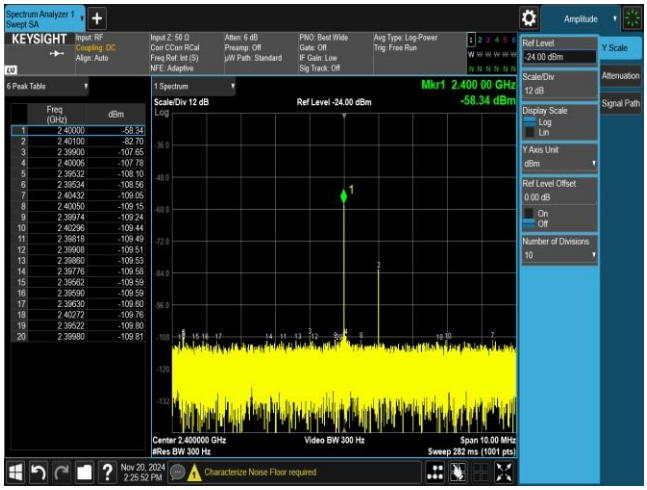


Figure 16. TX isolation (2.4GHz band)

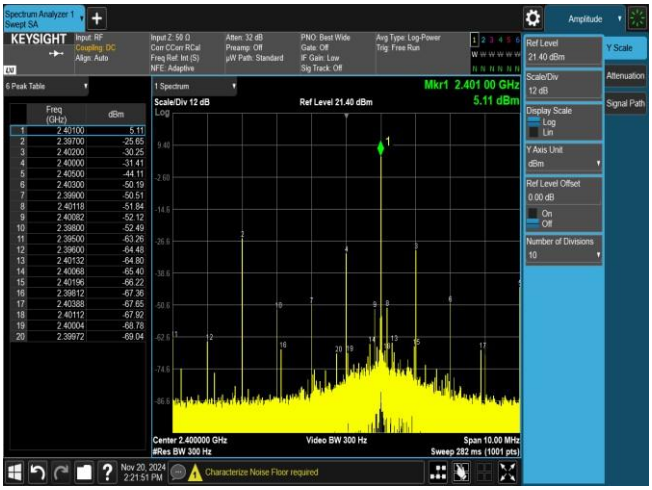


Figure 17. TX Max output (2.4 GHz band)

Figure 18. TX Noise Floor (2.4 GHz band)

Figure 19. TX OIP3 (2.4 GHz band)

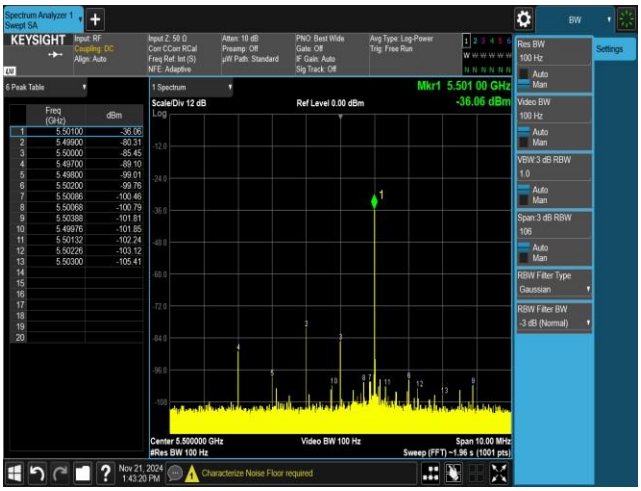


Figure 20. TX 40 dB attenuated output (5.5 GHz band)

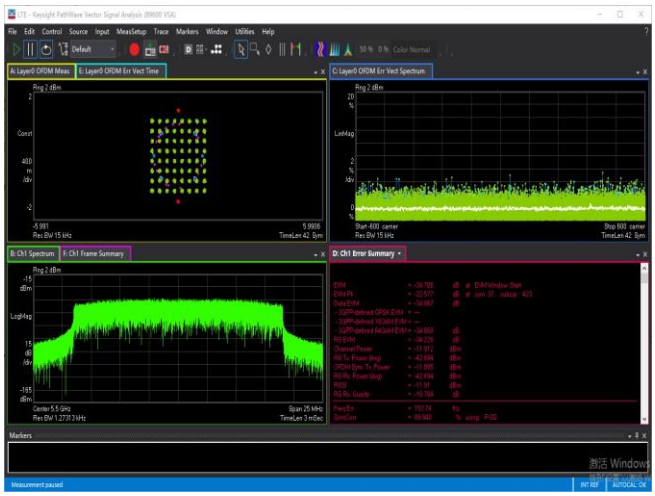


Figure 21. TX EVM (5.5 GHz band)

Figure 22. TX isolation (5.5 GHz band)

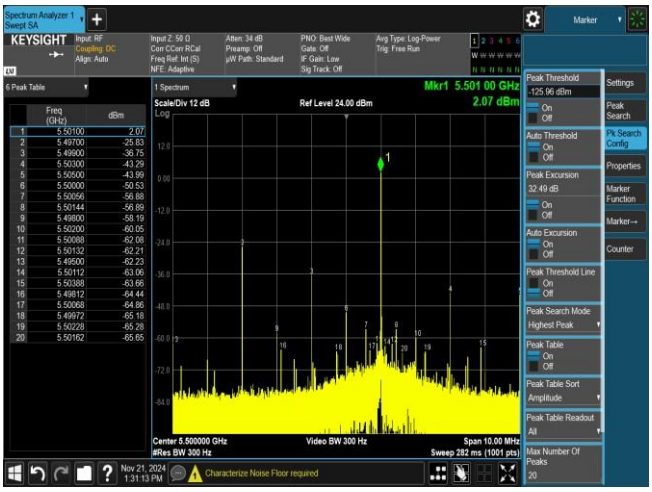


Figure 23. TX Max output (5.5 GHz band)

Figure 24. TX Noise Floor (5.5 GHz band)

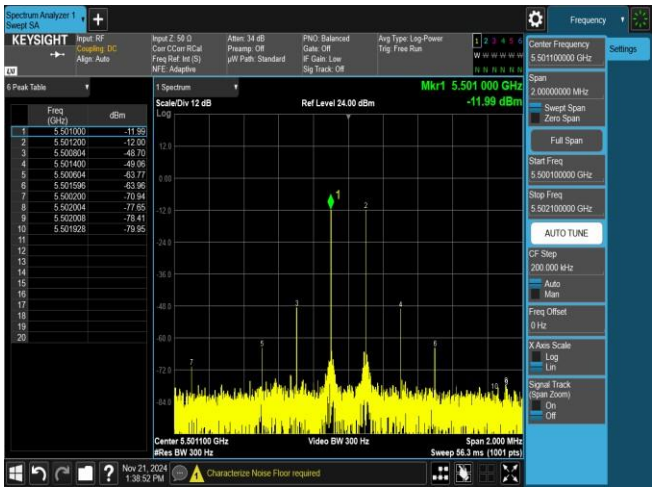


Figure 25. TX OIP3 (5.5 GHz band)

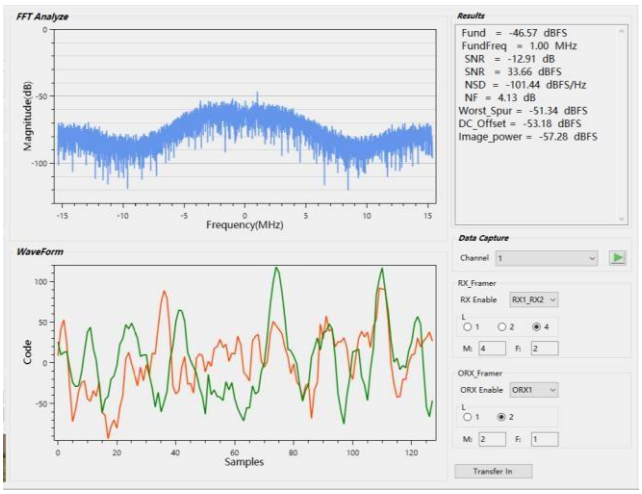


Figure 26. RX NF (800 MHz band)

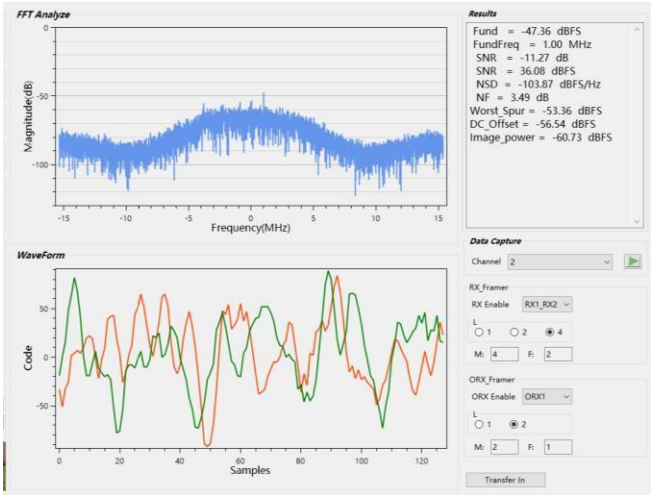


Figure 27. RX NF (2400 MHz band)

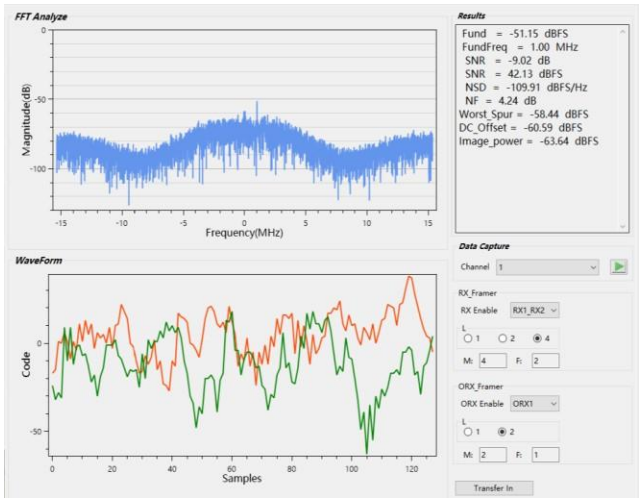


Figure 28. RX NF (5500 MHz band)

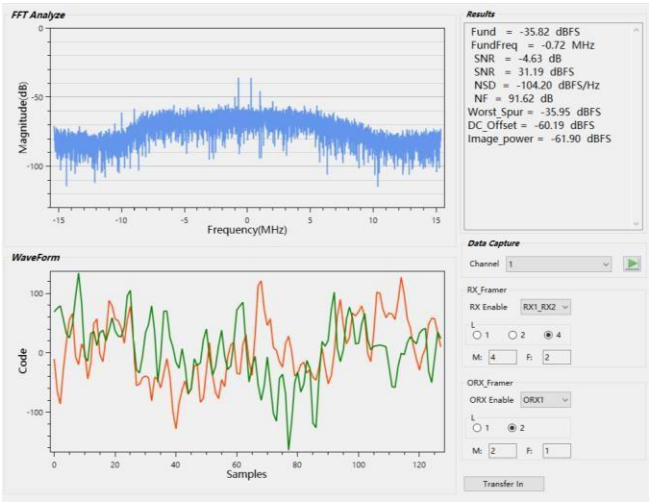


Figure 29. RX IIP2 (800 MHz band)

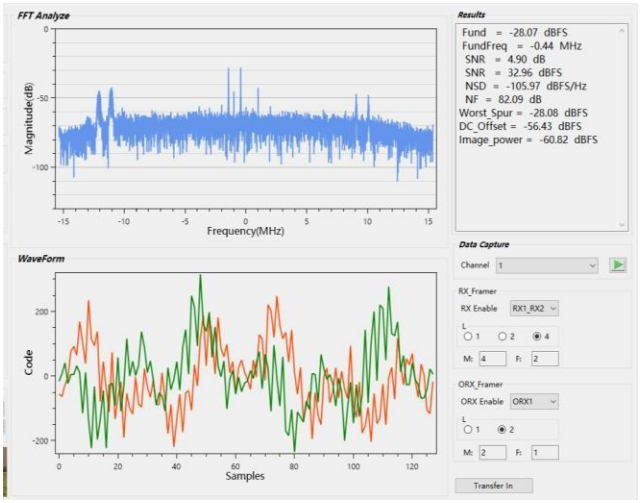


Figure 30. RX IIP2 (2400 MHz band)

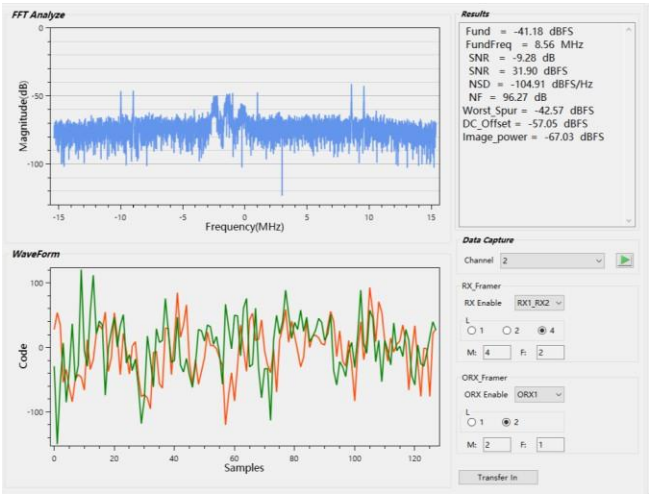


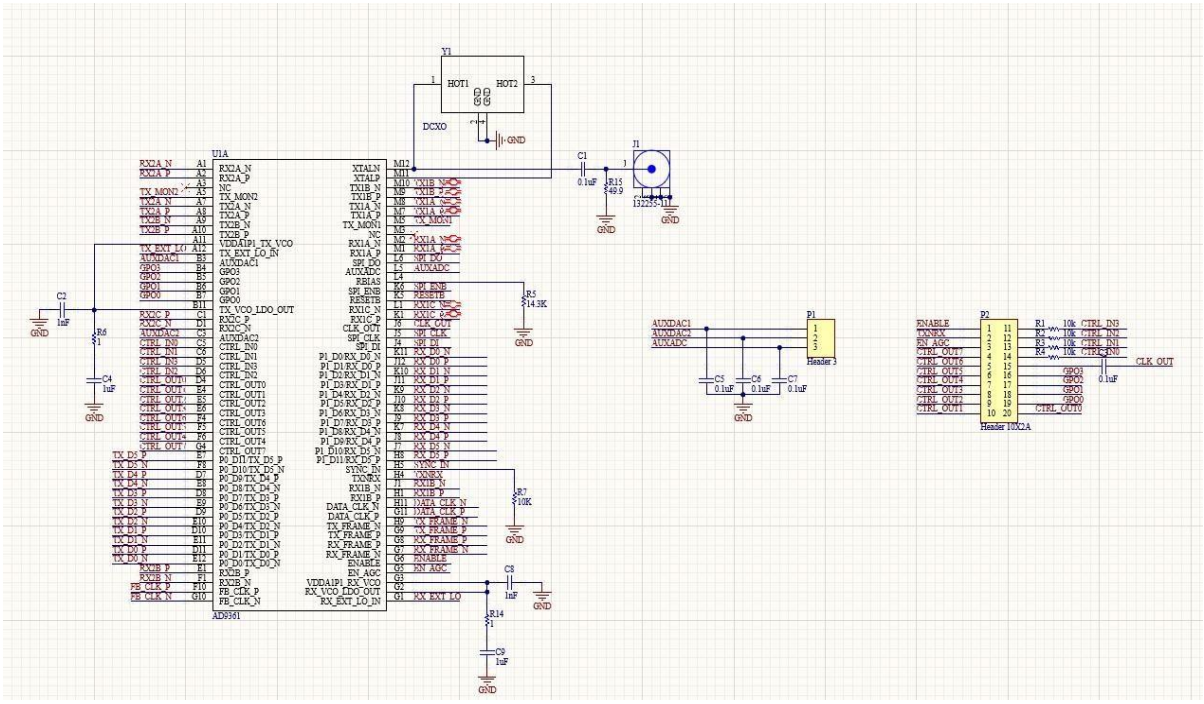
Figure 31. RX IIP2 (5500 MHz band)

Note: For IIP2 testing:
For 800 MHz, input two-tone frequencies are 830 MHz and 831 MHz (bandwidth: 10 MHz), with second-order intermodulation located at baseband ±1 MHz.

For 2400 MHz, input two-tone frequencies are 2460 MHz and 2461 MHz (bandwidth: 20 MHz), with second-order intermodulation located at baseband ±1 MHz.

For 5500 MHz, input two-tone frequencies are 5570 MHz and 5571 MHz (bandwidth: 50 MHz), with second-order intermodulation located at baseband ±1 MHz.

Typical application circuit diagram



Precautions

1. Product Installation Precautions:

1) During soldering, please pay attention to the orientation of components to avoid incorrect soldering.

2) All instruments and equipment used for circuit debugging must have proper and uniform grounding. PCB design must ensure good grounding and adequate power supply decoupling.

3) Care should be taken to avoid reverse power connection and short circuits between input/output terminals and the power supply, as these can easily damage the circuit.

4) Assembly Instructions:

1. This product has a Moisture Sensitivity Level (MSL) of MSL3. The allowable exposure time after removal from the moisture barrier bag, dry storage, or baking until reflow soldering is: ≤ 30°C/60% RH, 168 hours.

2. If the storage conditions of the component cannot be controlled or traced, strictly follow baking at 125°C for 8 hours before assembly.

3. If the assembly environment cannot guarantee ≤ 30°C/60% RH, complete soldering within 12 hours after baking.

4. After baking, the product is highly susceptible to electrostatic discharge (ESD). All handling processes must include ESD protection measures.

5. For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is 210° C–235°C. The maximum peak temperature should not exceed 235°C, with the time within ±5°C of the peak temperature not exceeding 20 seconds. The time above the liquidus line should be 60–

90 seconds, with a heating rate of 2–4°C/s and a cooling rate of 2–6°C/s.

6. For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is 230° C–245°C. The maximum peak temperature should not exceed 260°C, with the time within ±5°C of the peak temperature not exceeding 20 seconds. The time above the liquidus line should be 60–90 seconds, with a heating rate of 2–4°C/s and a cooling rate of 2–6°C/s.

7. If mixed assembly processes require elevated temperatures, ensure the component body temperature does not exceed 260°C (measured at the top surface of the component during reflow soldering).

8. This product uses lead-free/leaded solder balls made of SAC305/Sn63Pb37.

2. Product Usage Precautions:

1. Power-up Requirements: It is recommended to power up the analog and digital supplies simultaneously, or to power up the analog supply first.

2. LDO Output Decoupling: Use capacitors with low ESR at the LDO output.

3. PCB Grounding: In application, it is advised to implement a large-area ground plane on the PCB. This helps eliminate potential differences due to separate ground points and reduces the influence of board-generated capacitance on the circuit.

4. Power Pin Decoupling: Each power pin should be decoupled with a 1 μF or 0.1 μF capacitor placed as close as possible to the pin.

5. Analog Input (Differential): If differential input is used, the traces of the differential pair must be length-matched.

6. Power Separation: Digital and analog power supplies must be kept separate.

3. Product Protection Precautions:

All terminals of this circuit are designed with ESD protection structures; however, high-energy electrical pulses may still damage the circuit. Therefore, electrostatic discharge protection should be observed during testing, handling, and storage.

Common Faults and Solutions

1. No Output Signal: Check whether a clock signal is present at the clock terminal; verify that power and ground connections are correct, and ensure the input voltage and reference voltage are accurate.

2. Output Data Jitter: Inspect external circuits and connections to ensure the reference voltage is stable.

3. Unstable Device Operation: Check the power supply to ensure the supply voltage is stable.

Additional Notes

1. Product Status:

    - Production (This product model is currently in production and formal products are available.)
    - Pre-release (This product model has not yet entered mass production; samples are available.)

2. Model Suffix Variation Explanation

3. Replacement of Foreign/International Products Explanation

Replacement Comparison Table for Foreign/International Products

		Domestic Product	Foreign Product	Comparison Result
Absolute Maximum Ratings	VDDx to VSSx	-0.3 V to +1.4 V	-0.3 V to +1.4 V	Consistent
	VDD_INTERFACE toVSSx	-0.3 V to +3.0 V	-0.3 V to +3.0 V	Consistent
	VDD_GPO to VSSx	-0.3 V to +3.9 V	-0.3 V to +3.9 V	Consistent
	Logic input and output to VSSx	-0.3 V to VDD_INTERFACE + 0.3 V	-0.3 V to VDD_INTERFACE + 0.3 V	Consistent
	Input current to any pin except supply pins	±10 mA	±10 mA	Consistent
	RF input (peak power)	2.5 dBm	2.5 dBm	Consistent
	TX monitor input power (peak power)	9 dBm	9 dBm	Consistent
	Package power dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$	$(T_{JMAX} - T_A)/\theta_{JA}$	Consistent
	Maximum junction temperature (T_{JMAX})	110℃	110℃	Consistent
	Operating temperature range	-40℃ to +85℃	-40℃ to +85℃	Consistent
	Storage temperature range	-65℃ to +150℃	-65℃ to +150℃	Consistent
Recommended Operating Conditions	VDD_GPO	3.3V	3.3V	Consistent
	VDD_INTERFACE	1.8V	1.8V	Consistent
	Other VDD	1.3V	1.3V	Consistent
	Temperature	25 degrees	25 degrees	Consistent
	Reference clock frequency	40MHz	40MHz	Consistent
Performance Indicator	RX Center Frequency	70MHz-6000MHz	70MHz-6000MHz	Consistent
	TX Center Frequency	46.875MHz-6000MHz	46.875MHz-6000MHz	Consistent
	Noise Figure (800 MHz)	2dB	2dB	Consistent
	IIP3 (800 MHz)	-18dBm	-18dBm	Consistent
	Maximum Output Power (800 MHz)	8dBm	8dBm	Consistent
	OIP3 (800 MHz)	19dBm	19dBm	Consistent
Package Form		144-Ball Chip Scale Package Ball Grid Array	144-Ball Chip Scale Package Ball Grid Array	Consistent
Dimensions		10mm x 10mm x 1.7mm	10mm x 10mm x 1.7mm	Consistent
Replacement Suggestion		1. Direct replacement 2. Effective replacement 3. Functional replacement		