TGS9011

14-Bit, 125 MSPS, 8 Channel ADC

Data sheet

Features

- Channel synchronized sampling rate no missing codes
- 74.8 dB SNR
- 88 dB SFDR
- 1.8 V single-supply power
- Low power: 1272 mW/ total, 159 mW/ each channel
- Optional input range:1Vp-p to 2Vp-p
- 800 MHz full-power bandwidth sample-and-hold
- Serial LVDS output: each channel 1 lane or 2 lanes
- Shutdown and standby (sleep) modes
- 140 Pins (11.25 mm × 9 mm) BGA package
- Serial SPI port for programming configuration

Application

- Communication
- Cellular base station
- Software-defined radio
- Portable medical imaging
- Multi-channel data acquisition
- Non-destructive testing

Description

The TGS9011 is an 8-channel, synchronous sampling 14-bit ADC converter, designed for digitizing high-frequency and wide dynamic range signals. Its dynamic performance indicators reach up to 74 dB signal-to-noise ratio (SNR) and 88 dB spurious-free dynamic range (SFDR). Its static performance indicators achieve ±1LSB INL (typical value), ±0.3LSB DNL (typical value), and no missing codes. The conversion noise is as low as 1.2LSB RMS.

The digital output is serial LVDS, minimizing the number of data lines. Each ADC channel can be configured to output through two LVDS outputs (dual-lane mode) at the nominal sampling rate or through one LVDS output (single-lane mode) under lower sampling rate conditions.

The signal sources for the encoding clock input pins ENC+ and ENC− can be sine wave, PECL, LVDS, or TTL, with differential drive mode for all signal driving. The chip integrates a clock duty-cycle stabilizer, ensuring excellent overall performance even in the face of large duty cycle fluctuation ranges at full-speed clock frequencies.

Block Diagram

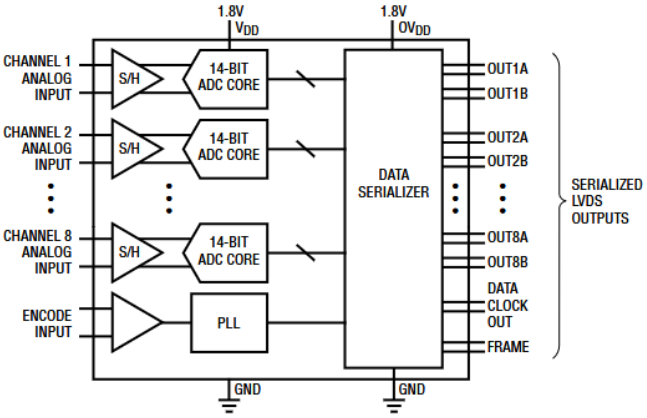


Figure 1. Block Diagram

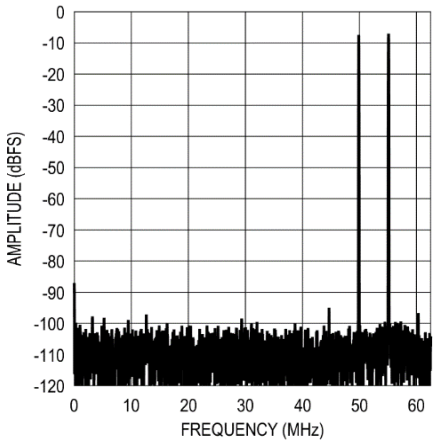


Figure 2. 125 MSPS, two-tone FFT f_{IN} = 70 MHz and 75 MHz

Absolute Maximum Ratings

Table 1. (Note 1, Note 2).

Parameters	Range	Unit
Power Supply Voltage V_{DD}, OV_{DD}	-0.3 ~ 2	V
Analog input voltage (AIN+, AIN-, PAR/$\overline{SER}$, SENSE) (Note 3)	-0.3 ~ OV_{DD} + 0.2	V
Digital input voltage (ENC+, ENC-, CS, SDI, SCK) (Note 4)	–0.3 ~ 3.9	V
Digital output voltage (SDO) (Note 4)	–0.3 ~ 3.9	V
Digital output voltage	-0.3 ~ V_{DD} + 0.3	V
Operating temperature range	–40 ~ +85	℃
Storage temperature range	–65 ~ 150	℃
ESD (HBM)	2000	V

Static Characteristic Conversion

Table 2.
If marked, ● this pointer is suitable for the entire operating temperature range; otherwise, it only refers to T_A = 25℃ (Note 5).

Symbol	Parameters	Condition		Minimum	Typical	Maximum	Unit
	Resolution (no missing codes)				14		Bits
INL	Integral Nonlinearity	Differential Analog Input (Note 6)	●	–4	t1	4	LSB
DNL	Differential Nonlinearity	Differential Analog Input	●	–0.9	t0.6	0.9	LSB
VOS	Offset Error	(Note 7)	●	–12	Float	12	mV
E_G	Gain error	Internal reference	●		0.3		%FS
		External reference	●	0		1	%FS
	Offset drift				t20		μtV/℃
	Full-scale drift	Internal reference			Tach		ppm/℃
		External reference			t25		ppm/℃
	Gain matching	External reference			t0.2		%FS
	Offset matching				Come on		mV
	Conversion noise	External reference			1.2		LSB_{RMS}

Analog Input Characteristics

Table 3.
If marked, ● this pointer is suitable for the entire operating temperature range; otherwise, it only refers to T_A = 25°C (Note 5).

Symbol	Parameters	Condition		Minimum	Typ.	Maximum	Unit
V_{IN}	Analog Input Range (AIN^+ - AIN^-)	1.7 V < V_{DD} < 1.9 V	●	1 to 2			V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode (AIN^+ - AIN^-)/2	Differential Analog Input (Note 8)	●	V_{CM} – 100 mV	V_{CM}	V_{CM} – 100 mV	V
V_{SENSE}	Apply SENSE external voltage reference	External reference mode	●	0.625	1.25	1.3	V
It_{INCM}	Analog input common-mode current			155			µA
I_{IN1}	Analog input leakage current (no encoding)		●	–1		1	µA
I_{IN2}	PAR/$\overline{SER}$, Input Leakage Current		●	–3		3	µA
I_{IN3}	SENSE Input Leakage Current	1.7 V < SENSE < 1.9 V	●	–6		6	µA
t_{AP}	Sample and Hold Acquisition Delay Time			0			ns
$t_{JIITTER}$	Sample and Hold Acquisition Delay Jitter			0.15			ps_{RMS}
CMRR	Common Mode Rejection Ratio of Analog Input			80			dB
BW-	Full-Power Bandwidth	Figure 11		800			MHz

Dynamic Characteristics

Table 4.
Any ● indication means that the pointer is suitable for the entire operating temperature range; otherwise, it only refers to T_A = 25°C A_{IN} = -1 BFS (Note 5).

Symbol	Parameters	Condition		Minimum	Typical	Maximum	Unit
SNR	Signal-to-Noise Ratio	5 MHz Input			75.4		dBFS
		70 MHz Input	●	73.2	74.8		dBFS
		140 MHz Input			73.2		dBFS
SFDR	Spurious-Free Dynamic RangSeecond or third harmonics	5 MHz Input			91		dBFS
		70 MHz Input	●	80	88		dBFS
		140 MHz Input			85		dBFS
	Spurious-Free Dynamic Range Fourth or higher harmonics	5 MHz Input			94		dBFS
		70 MHz Input	●	88	94		dBFS
		140 MHz Input			94		dBFS
S/(N+D)	Signal to "Noise + Distortion" Ratio	5 MHz Input			75.3		dBFS
		70 MHz Input	●	72.8	74.6		dBFS
		140 MHz Input			72.8		dBFS
	Crosstalk, near channel	10 MHz Input (Note 12)			–90		dBc
	Crosstalk, far channel	10 MHz Input (Note 12)			–100		dBc

Internal Reference Characteristics

Table 5.
Any ● indication means that the pointer is suitable for the entire operating temperature range; otherwise, it only refers to T_A = 25°C A_{IN} = -1 BFS (Note 5).

Parameters	Condition	Minimum	Typical	Maximum	Unit
V_{CM} Output voltage	I_{OUT} = 0	0.5●V_{DD} – 25 mW	0.5t●V_{DD}	0.5●V_{DD} + 25 mW	V
V_{CM} output temperature drift		t25			ppm/°C
V_{CM} output resistance	– 600 uA < I_{OUT} t < 1 mA	4			Ω
V_{REF} output voltage	I_{OUT} = 0	1.225	1.250	1.275	V
V_{REF} output temperature drift		t25			ppm/°C
V_{REF} output resistance	– 400 uA < I_{OUT} < 1 mA	7			Ω
V_{REF} Voltage Regulation	1.7 V < V_{DD} < 1.9 V	0.6			mV/V

Digital Input / Output

Table 6.
● indicates that the pointer is suitable for the entire operating temperature range; otherwise, it only refers to T_A = 25 °C (Note 5).

Symbol	Parameters	Condition		Min.	Typ.	Max.	Unit
Encoding Input (ENC+, ENC−)							
Differential Encoding Mode (ENC− not connected to GND)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common mode input voltage	Set internally	●		1.2		V
		Set externally (Note 8)		1.1		1.6	V
V_{IN}	Input voltage range	ENC+, ENC− to GND	●	0.2		3.6	V
R_{IN}	Input resistance	(Figure 15)			12		ktΩ
C_{IN}	Input capacitance				2.4		pF
Digital input (CS, SDI, SCK in serial or parallel programming mode. SDO in parallel programming mode)							
V_{IH}	High-level input voltage	V_{DD} = 1.8 V	●	1.3			V
V_{IL}	Low-level input voltage	V_{DD} = 1.8 V	●			0.6	V
I_{IN}	Input current	V_{IN} = 0 V to 3.6 V		–10		10	µA
C_{IN}	Input capacitance	(See Figure 15)			3		pF
SDO Output (Serial programming mode. Open-drain output. If using SDO, a 2 kΩ pull-up resistor)							
R_{OL}	Logic low output level to GND	VDD = 1.8 V, SDO = 0 V			200		Ω
I_{OH}	Logic high output leakage current	SDO = 0 V to 3.6 V	●	–10		10	µA
C_{OUT}	Output capacitance				3		pF
Digital data output							
V_{OD}	Differential output voltage	100 Ω differential load, 3.5 mA mode	●	247	350	454	mV
		100 Ω differential load, 1.75 mA mode	●	125	175	250	mV
V_{OS}	Common-mode output voltage	100 Ω differential load, 3.5 mA mode	●	1.125	1.25	1.375	V
		100 Ω differential load, 1.75 mA mode	●	1.125	1.25	1.375	V
R_{TERM}	On-chip termination resistance	Termination enabled, OV_{DD} = 1.8 V		100			Ω

Power Characteristics

Table 7.
Any pointer marked with ● indicates suitability for the entire operating temperature range; otherwise, it only refers to T_A = 25 ℃ (Note 9).

Symbol	Parameters	Condition		Min.	Typ.	Max.	Unit
V_{DD}	Analog Power Supply Voltage	(Note 10)	●	1.7	1.8	1.9	V
OV_{DD}	Output Power Supply Voltage	(Note 10)	●	1.7	1.8	1.9	V
I_{VDD}	Analog Power Supply Current	Sine wave input	●		576		mA
I_{OVDD}	Digital power current	Dual-lane mode, 1.75 mA mode	●		130		mA
		Dual-lane mode, 3.5 mA mode	●		144		mA
P_{DISS}	Power dissipation	Dual-lane mode, 1.75 mA mode	●		1272		mW
		Dual-lane mode, 3.5 mA mode	●		1296		mW
P_{SLEEP}	Sleep mode power consumption				1		mW
P_{NAP}	Standby mode power consumption	Enable encoding input signal			428		mW
		Disable encoding input signal			152		mW
		Disable encoding clock receiving module			86		mW

Timing Characteristics

Table 8.
Any pointer marked with ● indicates suitability for the entire operating temperature range; otherwise, it only refers to T_A = 25 ℃ (Note 5).

Symbol	Parameters	Condition		Minimum	Typical	Maximum	Unit
f_S	Sampling frequency	Dual-lane mode (Note 10, Note 11)	●	80		125	MHz
		Single-lane mode (Note 10, Note 11)	●	40		62.5	MHz
t_{ENCL}	ENC low-level time (Note 8)	duty-cycle stabilizer off	●	3.8	4	100	ns
		duty-cycle stabilizer on		2	4	100	ns
t_{ENCH}	ENC high-level time (Note 8)	duty-cycle stabilizer off	●	3.8	4	100	ns
		duty-cycle stabilizer on		2	4	100	ns
t_{AP}	Sample and Hold Acquisition Delay Time			0			ns

Table 9.

Symbol	Parameters	Condition		Minimum	Typical	Maximum	Unit
Digital data output (RTERM = 100 Ω Differential, CL = 2 pF to GND [at each output])							
t_{SER}	Serial data bit period	Dual-lane, 14-bit serialization			1/(7 ● f_S)		s
		Single-lane, 14-bit serialization			1/(14 ● f_S)		s
t_{FRAME}	FR to DCO delay		●	0.35● t_{SER}	0.5● t_{SER}	0.65● t_{SER}	s
t_{DATA}	DATA to DCO delay		●	0.35● t_{SER}	0.5● t_{SER}	0.65● t_{SER}	s
t_{PD}	Propagation delay		●	0.7n + 2● t_{SER}	1.1n + 2● t_{SER}	1.5n + 2● t_{SER}	s
t_R	Output rise time	Data, DCO, FR, 20% to 80%			0.17		ns
t_F	Output fall time	Data, DCO, FR, 20% to 80%			0.17		ns
	DCO per cycle jitter	t_{SER} = 1 ns			60		psP-P
	Pipeline delay				8		Cycle

Table 10.

Symbol	Parameters	Condition		Minimum	Typical	Maximum	Unit
SPI port timing (Note 8)							
t_{SCK}	SCK period	Write mode	●	40			ns
		Readback mode, C_{SDO} = 20 pF, R_{PULLUP} = 2 K	●	250			ns
t_S	$\overline{CS}$ to SCK setup time		●	5			ns
t_H	SCK to $\overline{CS}$ setup time		●	5			ns
t_{DS}	SDI Establishment Time		●	5			ns
t_{DH}	SDI Hold Time		●	5			ns
t_{DO}	SCK Falling toSDO Valid	Readback mode, C_{SDO} = 20 pF, R_{PULLUP} = 2 K	●			125	ns

Note 1: Stresses above the values listed in the "Absolute Maximum Ratings" section may cause permanent damage to the device. Prolonged exposure to any absolute maximum rating condition may affect the reliability and lifespan of the device.

Note 2: All voltage values are referenced to GND (GND and OGND are shorted, unless otherwise specified).

Note 3: When the voltage on these pins is pulled below GND or above VDD, they will be clamped by internal diodes. Under conditions below GND or above VDD this product can handle input currents greater than100mA without latch-up.

Note 4: When the voltage of these pins is pulled below GND, they will be clamped by internal diodes. When the voltage of these pins is pulled above VD, they will not be clamped by internal diodes. In cases below GND , this product can handle input currents greater than 100 mA without locking up.

Note 5: V_{DD} = OV_{DD} = 1.8 V, f_{SAMPLE} = 125 MHz, dual-lane output mode, differential ENC+/ENC- = 2VP-P, sine wave, input range = 2VP-P (using differential drive), unless otherwise specified.

Note 6: Integral nonlinearity is defined as the best fit of a code relative to a transfer function curve. The degree of deviation from the ideal straight line. This deviation is measured from the center of the quantization band.

Note 7: offset error is the output code between 00 0000 0000 0000 and 11 1111 1111 1111 when swinging between, (using two's complement output mode) starting from -0.5 LSB measured offset voltage.

Note 8: Guaranteed by design, untested.

Note 9: V_{DD} = OV_{DD} =1.8 V, f_{SAMPLE} = 125 MHz, dual-lane output mode, ENC+ = single-ended 1.8 V square wave, ENC- = 0 V, input range = 2VP-P (using differential drive), unless otherwise specified. The power supply current and power consumption specifications are the total values for the entire chip (not per channel).

Note 10: Recommended operating conditions.

Note 11: The maximum sampling frequency depends on the speed grade of the device and the serialization mode used. The maximum serial data rate is 1000 Mbps, so t_{SER} must be greater than or equal to 1 ns.

Note 12: Near-channel crosstalk refers to the crosstalk from channel 1 to channel 2 and from channel 3 to channel 4. Far-channel crosstalk refers to the crosstalk from channel 1 to channel 3 or 4, and from channel 2 to channel 3 or 4.

Timing Diagram

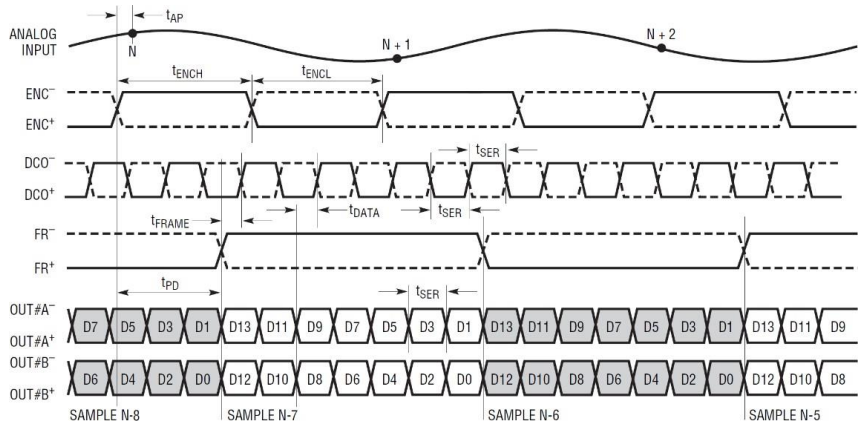


Figure 3. Dual-lane 14-bit serialization output mode

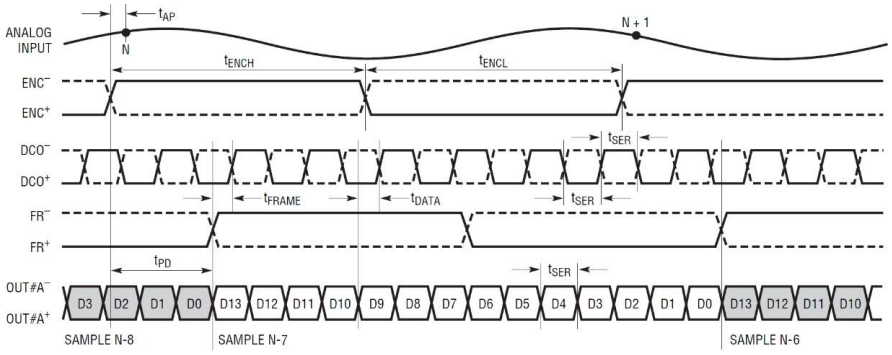


Figure 4. Single-lane 14-bit serialization output mode

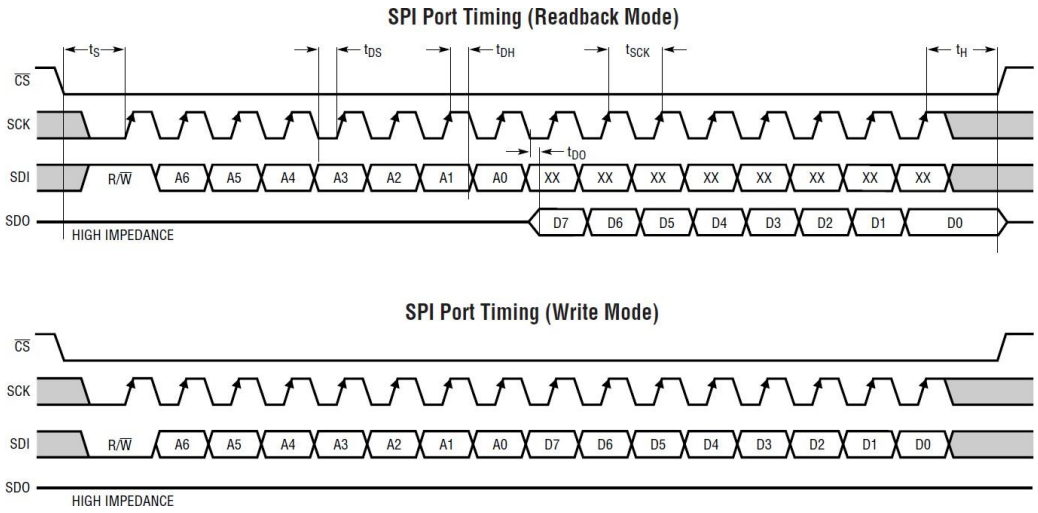
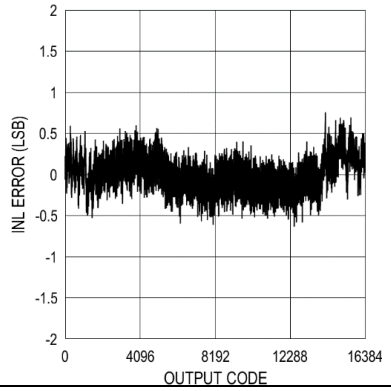
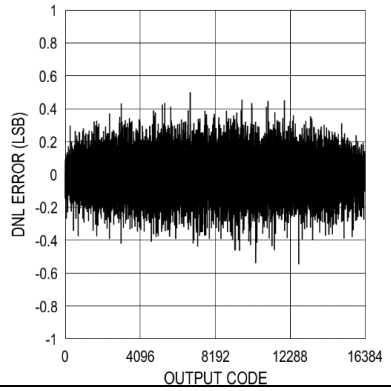
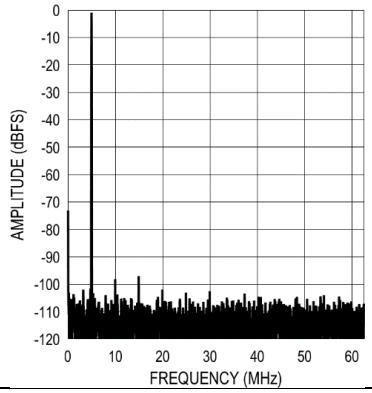
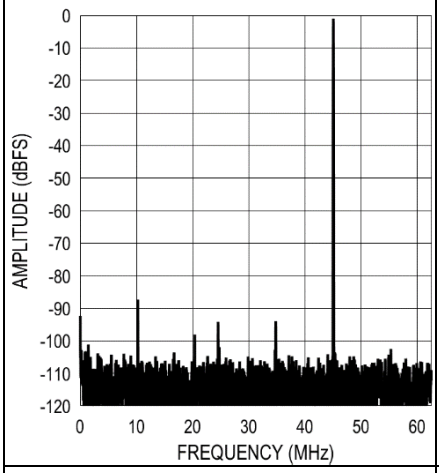
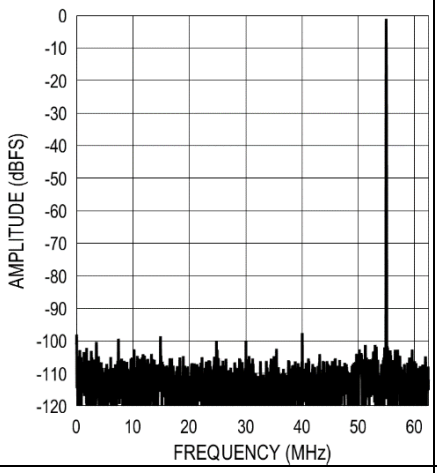
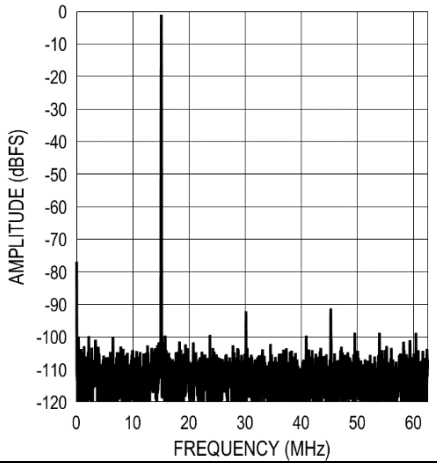
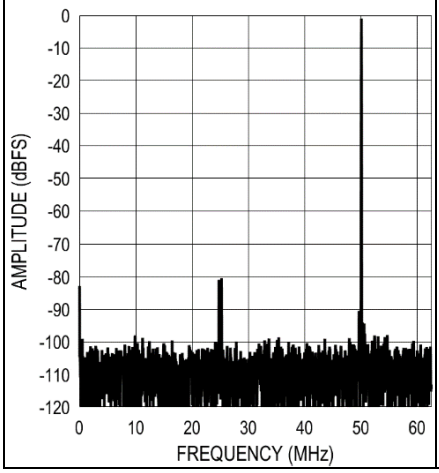
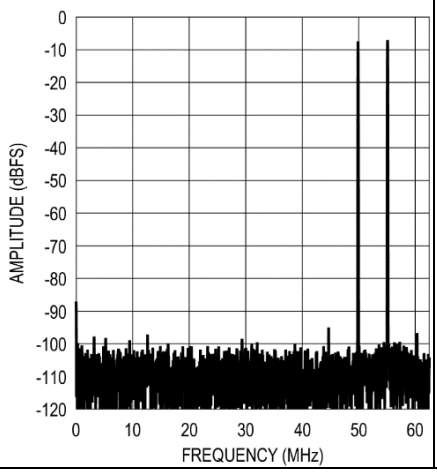
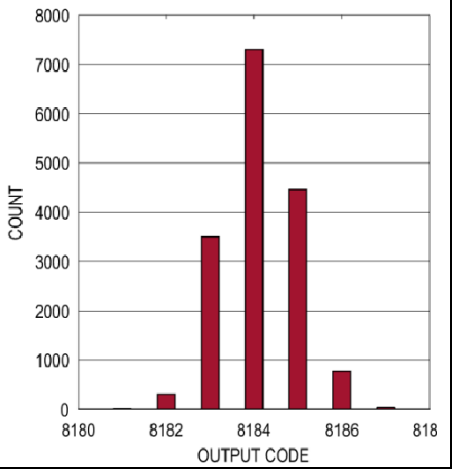


Figure 5. SPI port read/write timing

Typical Performance Characteristics

Integral Nonlinearity	Differential Nonlinearity	8k points FFT, f_{IN} = 5 MHz, -1 dBFS, 125 Msps
		
8k points FFT, f_{IN} = 45 MHz, - 1dBFS, 125 Msps	8k points FFT, f_{IN} = 70 MHz, - 1 dBFS, 125 Msps	8k points FFT, f_{IN} = 140 MHz, - 1 dBFS, 125 Msps
		
8k points FFT, f_{IN} = 300 MHz, -1 dBFS, 125 Msps	8k points dual-tone FFT, f_{IN} = 70 MHz, 75 MHz, -1 dBFS, 125 Msps	Short-circuit input histogram
		

Application Information

Functional Block Diagram

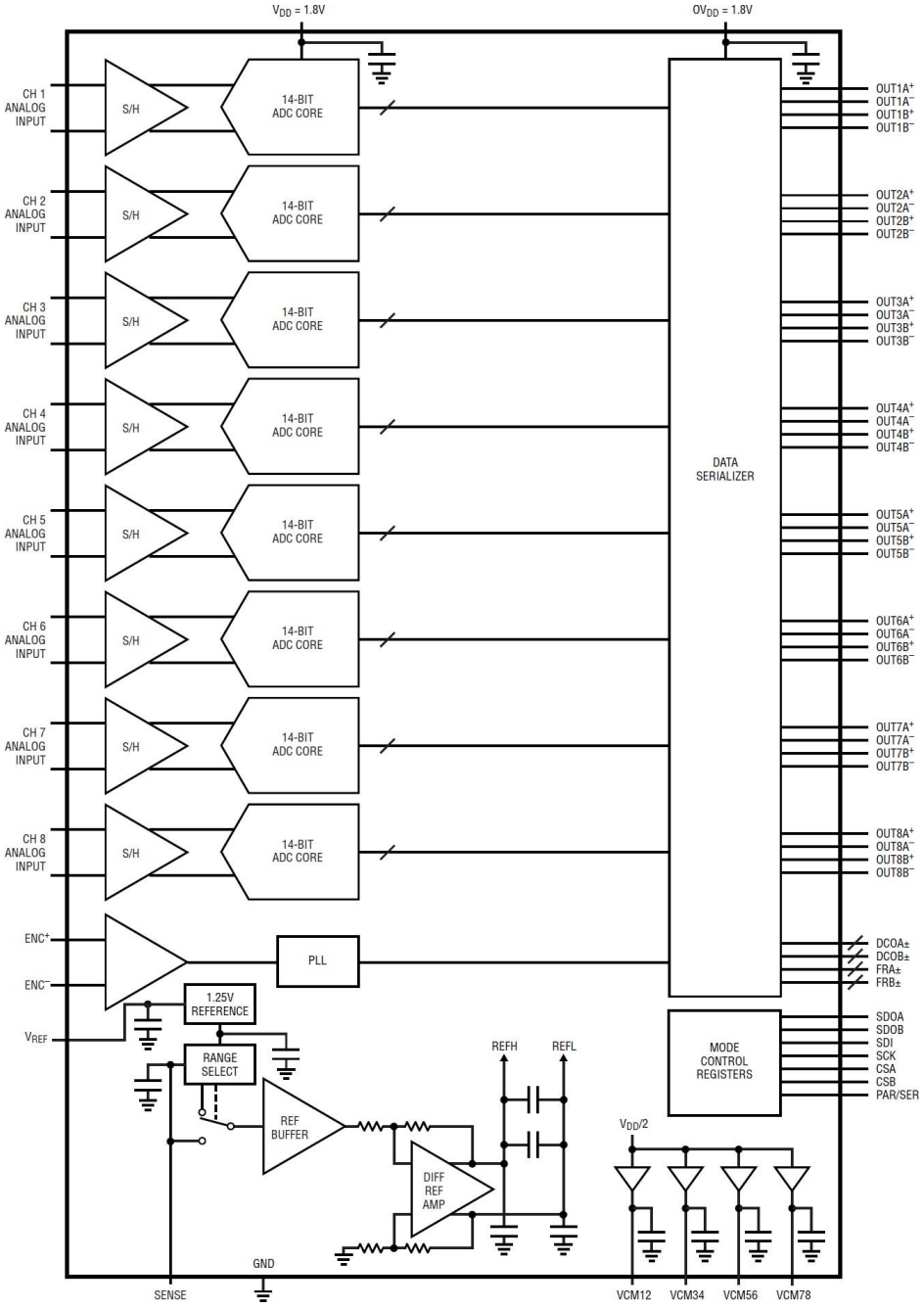


Figure 6.

Analog Input

Analog input is a differential CMOS sample-and-hold circuit (Figure 7). It should be differentially driven by a common-mode voltage set by the V_{CM} output pin (nominal value is $V_{DD}/2$) for the input. For a 2 V input range, the input signal should swing between V_{CM} - 0.5 V and V_{CM} + 0.5 V. There should be a 180° phase difference between the differential inputs.

Each channel shares a common encoding clock circuit for simultaneous sampling (Figure 7).

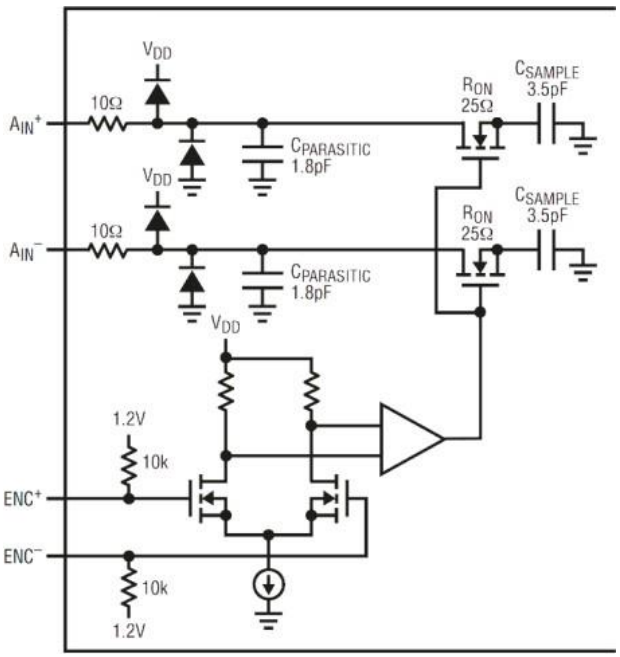


Figure 7. Equivalent input circuit, showing only one of the 4 analog channels.

Input Driver Circuit

Input Filtering

If possible, a RC low-pass filter should be directly placed at the analog input. This low-pass filter will isolate the driver circuit from the ADC sample-and-hold switch and can also suppress broadband noise interference on the driver circuit. Figure 8 shows an example of an input RC filter. The parameter values of the RC components should be selected based on the input frequency of the application circuit.

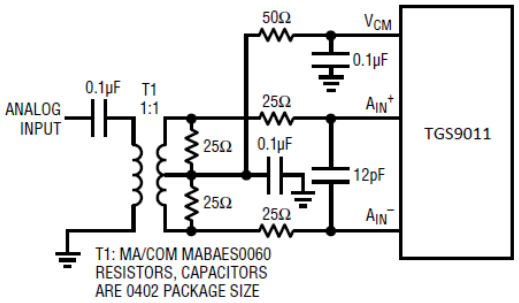


Figure 8. Analog input circuit using a transformer. Recommended for input circuits from 5 MHz to 70 MHz.

Transformer Coupling Circuit

Figure 8 shows the analog input driven by an RF transformer with a center-tapped secondary winding. A bias is applied to the center tap by VCM, setting the ADC input to its optimal DC level. At higher input frequencies, the transmission line balanced-unbalanced transformer (Figures 9 to 11) exhibits better balance characteristics, reducing ADC distortion.

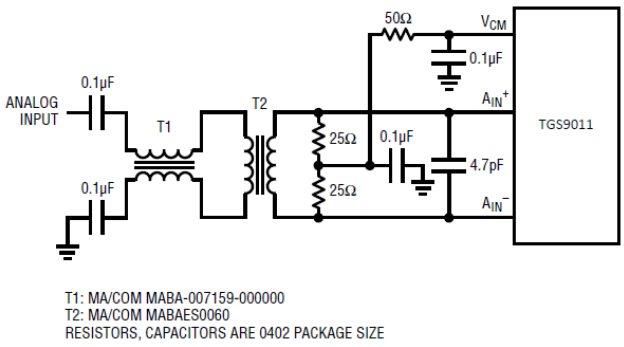


Figure 9. Recommended front-end circuit for input frequencies from 70 MHz to 170 MHz

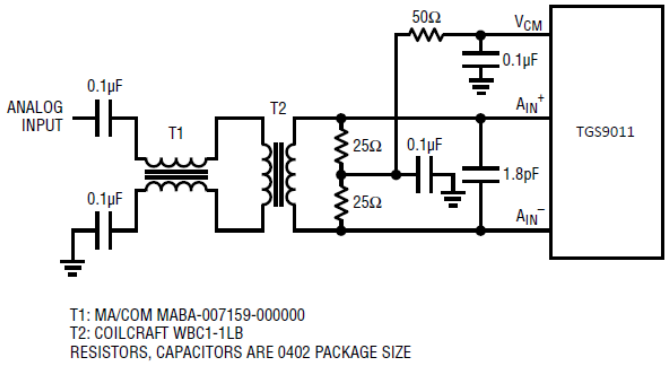


Figure 10. Recommended front-end circuit for input frequencies from 170 MHz to 300 MHz

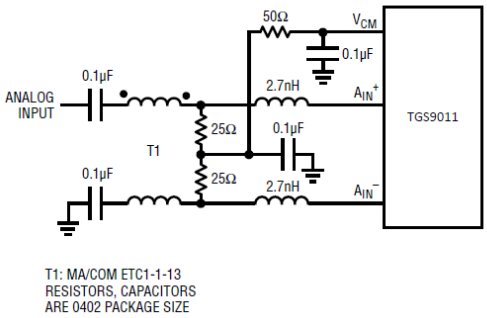


Figure 11. Recommended front-end circuit for input frequencies above 300 MHz

Amplifier Circuit

Figure 12 shows the analog input driven by a high-speed differential amplifier. The amplifier's input is AC coupled to the ADC, allowing for optimal setting of the amplifier's output common-mode signal to minimize distortion.

At very high frequencies, the distortion of the RF gain component is often smaller than that of the differential amplifier. If the gain component is single-ended, it should be connected through a transformer circuit (Figure 9 to Figure 11) converts the signal to differential type before driving ADC.

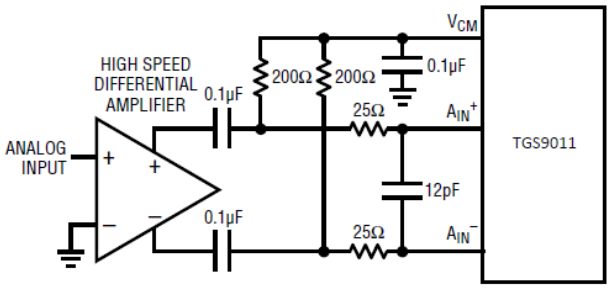


Figure 12 shows the front-end circuit using a high-speed differential amplifier.

Reference

TGS9011 has an internal 1.25 V voltage reference. When selecting a 2 V input range based on the internal reference, the SENSE pin must be connected to V_{DD}. When selecting a 1 V input range based on the internal reference, the SENSE pin must be grounded. When selecting a 2 V input range based on an external reference, a 1.25 V reference voltage must be connected to the SENSE pin (see Figure 14). Applying a voltage between 0.625 V and 1.30 V to the SENSE pin can adjust the input range, and the corresponding input range will be 1.6 • V_{SENSE}.

The 4 channels of the ADC share a common reference, so the input range of each channel cannot be adjusted individually.

As shown in Figure 13, the V_{REF}, REFH, and REFL pins should be bypassed. The 0.1 µF capacitor between REFH and REFL should be placed as close to the pins as possible (not on the back of the circuit board).

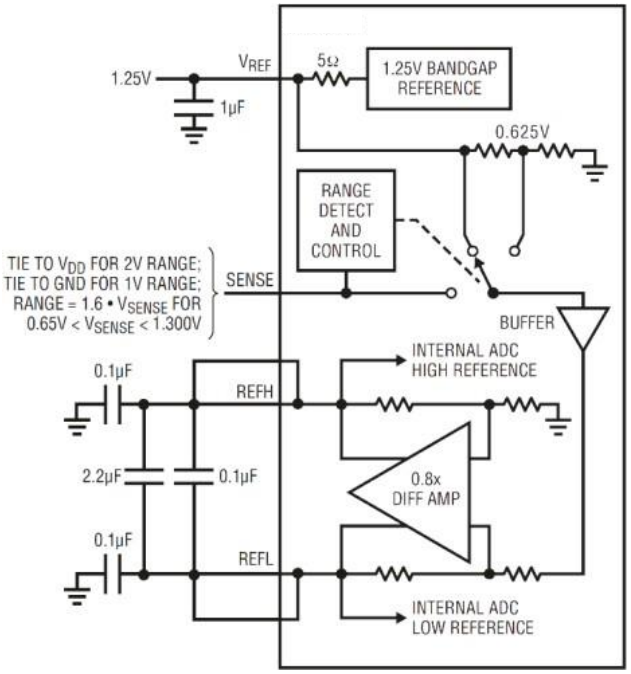


Figure 13. Reference Circuit

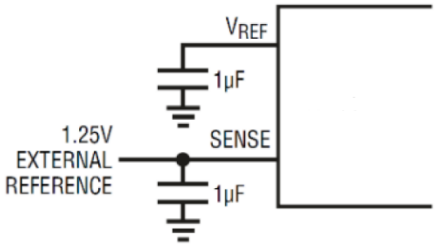


Figure 14. Using an External 1.25 V Reference

Encoding Clock Input

The signal quality of the encoding clock input significantly affects the noise performance of the ADC. The encoding input should be treated as an analog signal, and its PCB routing should not be adjacent to digital signal traces. The encoding input is in differential encoding mode (see Figure 15).

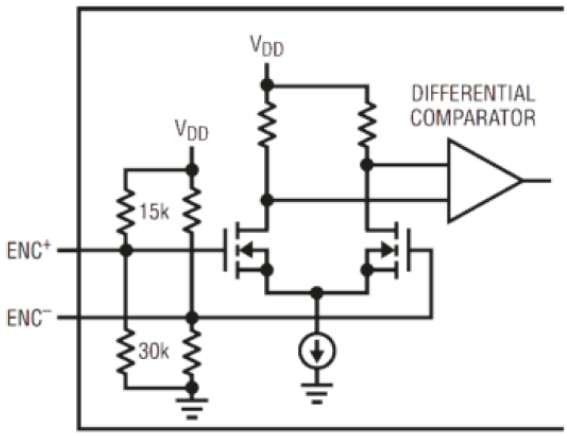


Figure 15. Equivalent Encoding Input Circuit for Differential Encoding Mode

For encoding inputs in the form of sine, PECL, or LVDS, differential encoding mode is recommended (see Figures 16 and 17). The pins for the encoding input are internally biased to 1.2 V through a 10k equivalent resistor. The externally applied encoding input signal can be higher than VDD (up to 3.6 V), while its common-mode voltage range should be from 1.1 V to 1.6 V. In differential encoding mode, ENC- should be at least 200 mV higher than ground potential to avoid false triggering of single-ended encoding mode. To reduce the impact of jitter on performance, ENC+ should have fast rise and fall times.

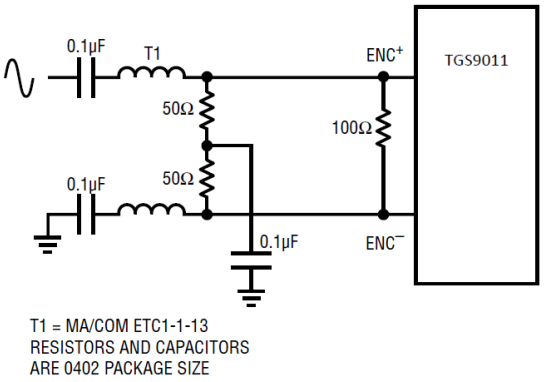


Figure 16. Sine Encoding Driver

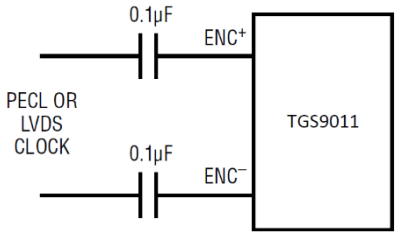


Figure 17. PECL or LVDS Encoding Driver

Clock PLL and Duty-Cycle Stabilizer

The encoding clock is multiplied internally in the chip via a phase-locked loop (PLL), which then generates serial digital output data using this multiplied clock. Each time the encoding signal changes frequency or is turned off, the PLL requires 25 µs to re-lock the frequency and phase with the input clock. The internal clock duty-cycle stabilizer circuit allows the duty cycle of the applied encoding signal to vary between 30% and 70%. In serial programming mode, while the duty-cycle stabilizer can be disabled, it is not recommended. In parallel programming mode, the duty-cycle stabilizer is always enabled.

Digital Output

The digital output of TGS9011 is serialized LVDS signals. Data is processed in 14-bit serialization (see timing diagram for details). Each ADC channel outputs two bits at a time via two LVDS serial ports A and B (dual-lane mode), and it can also be selected to output one bit via a single LVDS serial port under lower sampling rate conditions (single-lane mode). Both modes use a double data rate (DDR) format to double the output efficiency.
DDR output data should be latched by the master controller processor on the rising and falling edges of the data clock output (DCO). The data frame output (FR) can be used to determine the starting point of the data output for each conversion result.
The ADC's 125 MHz maximum sampling rate determines the maximum serial data output rate to be 875 Mbps, while the DCO reaches a maximum frequency of 437.5 MHz (see Table 11). The minimum sampling rate of the ADC is limited by the minimum output frequency of the internal phase-locked loop, which is 80 Msps in dual-lane mode and 40 Msps in single-lane mode.

Table 11. Maximum Sampling Rate in Serialized Mode

Mode	Maximum sampling rate f_S (MHz)	DCO Frequency	FR Frequency	Serial data rate
Dual-lane	125	$3.5 \bullet f_S$	$0.5 \bullet f_S$	$7 \bullet f_S$
Single-lane	62.5	$7 \bullet f_S$	f_S	$14 \bullet f_S$

By default, the digital output is at standard LVDS levels: that is, a 3.5 mA output current and a 1.25 V output common-mode voltage. Each pair of LVDS outputs requires an external 100 Ω differential termination resistor. The termination resistors should be placed as close as possible to the LVDS receivers.

Adjustable LVDS Output Current

The default value for the output driver current is 3.5 mA. In serial programming mode, this current can be adjusted via control register A2. The configurable current values are

1.75 mA, 2.1 mA, 2.5 mA, 3 mA, 3.5 mA, 4 mA, and 4.5 mA. In parallel programming mode, the SCK pin can select either 3.5mA or 1.75mA current values.

Optional Internal Termination for LVDS Driver

In most cases, an external 100 Ω termination resistor provides excellent LVDS signal integrity. Additionally, an internal 100 Ω termination resistor can be enabled via the mode serial programming control register A2. The internal termination helps absorb reflections caused by poor termination at the receiver end. When the internal termination is enabled, the output driver current must be doubled to maintain the same output voltage swing. In parallel programming mode, the SDO pin is responsible for enabling the internal termination. The internal termination should only be used in 1.75 mA, 2.1 mA, or 2.5 mA LVDS output current modes.

Data Format

Table 12 describes the relationship between the simulated input voltage and the digital data output bits. By default, the output data format is offset binary. The binary two's complement format can be selected by serial programming of the mode control register A1.

Table 12.

(AIN+-AIN-) (2 V Range)	D13-D0 (Offset Binary)	D13-D0 (Two's Complement)
>1.000000V +0.99878V +0.999756V	11 1111 1111 1111 11 1111 1111 1111 11 1111 1111 1110	01 1111 1111 1111 01 1111 1111 1111 01 1111 1111 1110
+0.000122V +0.000000V -0.000122V -0.000244V	10 0000 0000 0001 10 0000 0000 0000 01 1111 1111 1111 01 1111 1111 1110	00 0000 0000 0001 00 0000 0000 0000 11 1111 1111 1111 11 1111 1111 1110
-0.999878V -1.000000V <-1.000000V	00 0000 0000 000100 0000 0000 000000 0000 0000 0000	10 0000 0000 0001 10 0000 0000 0000 10 0000 0000 0000

Digital Output Random Function Generator

Interference from ADC digital output is sometimes unavoidable. Digital interference may arise from capacitive or inductive coupling, or through coupling via ground planes.
Even small coupling coefficients can introduce unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted outside the chip, such unwanted tones can be minimized in amplitude.
Digital output can be randomized by performing an "exclusive OR" logic operation between the LSB and all other data output bits. For decoding, the inverse operation is applied, i.e., performing an "exclusive OR" operation between the LSB and all other bits. The FR and DCO outputs are unaffected. The output random function generator is enabled by serial programming of the mode control register A1.

Digital Output Test Mode

To perform in-line testing of the digital interface to the ADC, a test mode can be used to force the ADC data output of all channels (D13-D0) to known values. This digital output test mode is enabled by serial programming of the mode control registers A3 and A4. When enabled, the priority of the test mode will be higher than all other formatting modes: binary two's complement and random function generator.

Output Disable

The digital output can be disabled by serial programming of the mode control register A2. The current drivers for all digital outputs (including DCO and FR) are disabled to save power or enable in-line testing. When disabled, the common mode of each output pair changes to high impedance, but the differential

impedance can remain low.

Sleep and Standby Modes

The ADC can be placed in sleep or standby mode to save power. In sleep mode, the entire chip is powered down, resulting in a power consumption of 1 mW. Sleep mode is enabled by the mode control register A1 (serial programming mode) or SDI (parallel programming mode). The time required to recover from sleep mode depends on the size of the bypass capacitor on VREF. For the recommended parameter values in Figure 13, the ADC will stabilize after 2 ms.
In standby mode, any combination of ADC channels can be powered down while the internal reference circuit and PLL remain operational, allowing for a faster wake-up speed than sleep mode. Recovery from standby mode requires at least 100 clock cycles. If the application requires very accurate DC stability, an additional 50 μs time should be provided to allow the on-chip reference to stabilize from slight temperature drift (caused by changes in power supply current when the ADC exits standby mode). In serial programming mode, standby mode is enabled by the mode register A1.

Device Programming Mode

The operating mode of the TGS9011 can be set using a parallel interface or a simple serial interface. The serial interface offers greater flexibility and can set all available modes. The parallel interface has more limitations and can only set certain more commonly used modes.
Parallel Programming Mode
If you need to use the parallel programming mode, you should connect PAR/SER to V_{DD}. The $\overline{CS}$, SCK, SDI, and SDO pins are binary logic inputs responsible for setting certain operating modes. These pins can be connected to VDD or ground, or driven by 1.8 V, 2.5 V, or 3.3 V CMOS logic circuits. When used as an input, SDO should be driven through a 1k series resistor. Table 13 lists the modes set using $\overline{CS}$, SCK, SDI, and SDO.

Table 13. Parallel programming mode control bits (PAR/$\overline{SER}$ = V_{DD})

Pins	Description
$\overline{CS}$	Dual-lane/ Single-lane selection bit 0 = Dual-lane, 14 bit serialized output mode 1 = Single-lane, 14 bit serialized output mode
SCK	**LVDS** current selection bit 0 = 3.5mA LVDS current mode 1 = 1.75 mA LVDS current mode
SDI	**Power-off control bit** 0 = Normal operation 1 = Sleep mode
SDO	Internal terminal resistor selection bit 0 = Internal termination resistor is disabled 1 = Internal termination resistor is enabled

Serial Programming Mode

If you want to use the serial programming mode, you should connect PAR/$\overline{SER}$ to ground. The $\overline{CS}$, SCK, SDI, and SDO pins become a serial interface used to set the ADC mode control register. Data and a 16-bit serial word are written to a register. Data can also be read back from a register to verify its contents. Serial data transmission starts when $\overline{CS}$ is pulled low. The data on the SDI pin is latched on the first 16 rising edges of SCK. After the first 16 rising edges
All rising edges on SCK are ignored. When $\overline{CS}$ is pulled high again, the serial data transmission ends.
16 the first bit of the input word is R/W bit. Next, 7 bits are the address bits of the register (A6:A0). Finally, 8 bits are the data bits of the register (D7:D0).
If the R/W bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/W bit is high, the data in the register set by the address bits (A6:A0) will be read back

on the SDO pin (see the "Timing Diagram" section). During the execution of a readback command, the register is not updated and the data on the SDI is ignored.
SDO pin is an open-drain output, pulled to ground potential with a 200 Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If the serial data is only written and not read back, the SDO pin can be left floating without a pull-up resistor. Table 14 shows the mapping of the mode control register.

Software Reset and Initialization

If serial programming is used, the mode control register should be programmed as soon as possible after the power is turned on and stabilized.

The first serial command must be a software reset, which will reset all register data bits to 0. To perform a software reset, the D7 bit in the reset register should be written as a logic “1 ”. After the reset

After the SPI write command is completed, the D7 bit will be automatically reset to 0.

After each software reset, the mode control register must be programmed according to the initialization values (Table 14) to allow the ADC to enter normal operating mode. For mode control after entering normal operation, refer to Table 14 and program only the required register bits accordingly.

Grounding and Bypassing

The TGS9011 requires a printed circuit board with a clean and complete ground plane. It is recommended to use a multilayer PCB with an internal ground plane laid out in the first layer of the PCB beneath the ADC chip. The layout of the printed circuit board should ensure that digital and analog signal lines are kept as separate as possible. In particular, care should be taken to avoid routing digital signal traces along the analog signal traces or beneath the ADC.

High-quality ceramic bypass capacitors should be used on the V_{DD}, OV_{DD}, V_{CM}, and V_{REF} pins. Bypass capacitors must be placed as close to the device pins as possible. The traces connecting the pins and bypass capacitors must be kept short and as wide as possible.

Analog inputs, encoded signals, and digital outputs should not be adjacent to each other. Ground fill and ground vias should be used as barriers to isolate these signals from each other.

Thermal Conductivity

The majority of the heat generated by the TGS9011 is transferred from the chip to the printed circuit board through the bottom of the package.

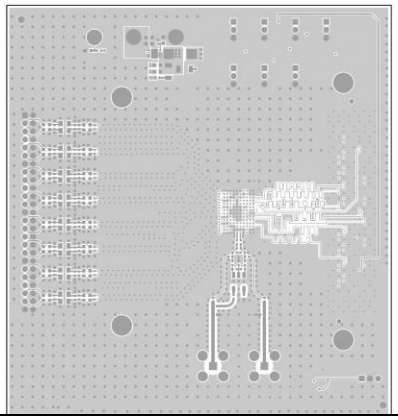
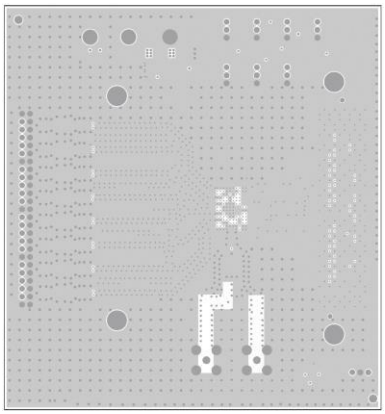
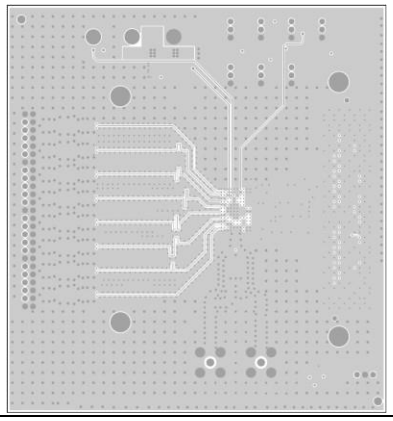
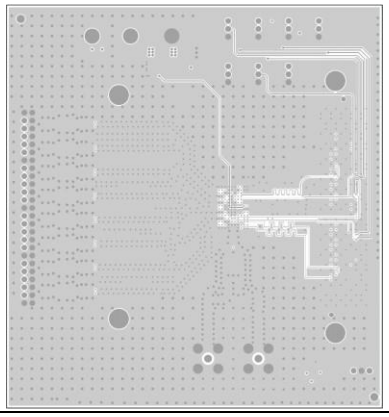
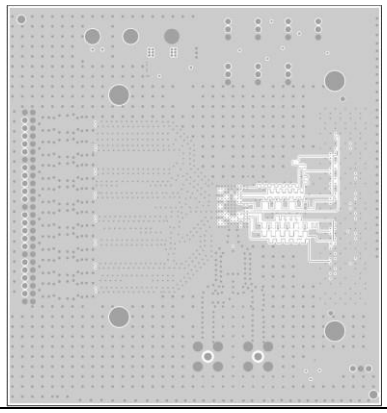
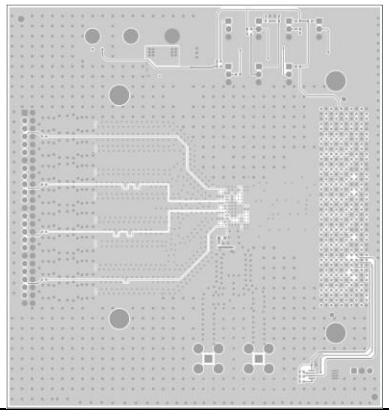
The ground pins should be connected to the internal ground plane of the PCB through multiple vias.

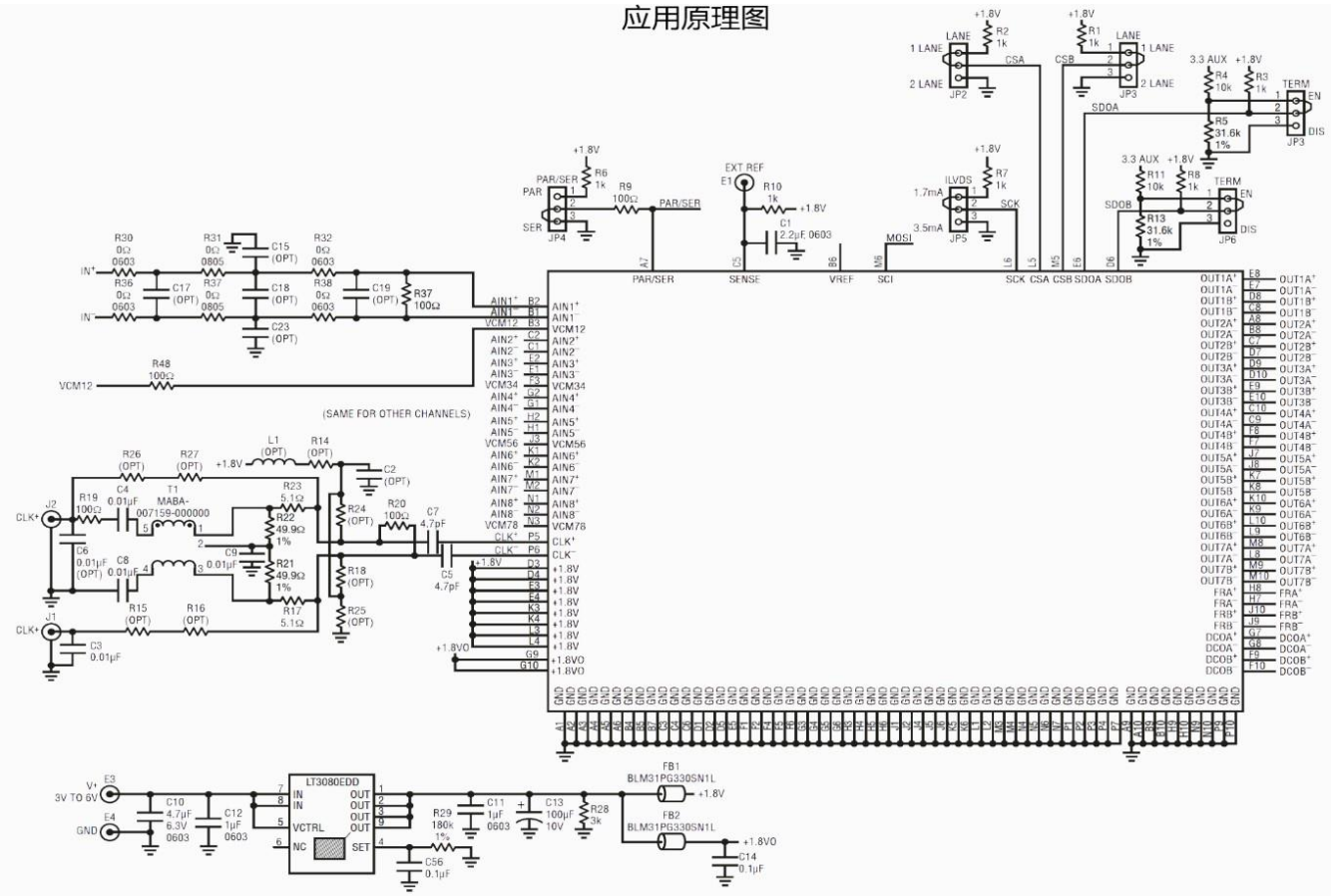
Register Table

Register Name	Address (HEX)	Data bits	Function	Default Value	Initial value (HEX)
A0	00	<7>	Reset Soft reset,1 Active	0	
		<6:0>	Unused, irrelevant bits	X	
A1	01	<7>	**DCSOFF** Clock duty-cycle stabilizer bit 0= Enable clock duty-cycle stabilizer 1= Disable clock duty-cycle stabilizer	0	80
		<6>	**RAND** Data output randomization mode control bit 0 = Disable output randomization mode 1 = Enable output randomization mode	0	
		<5>	**TWOSCOMP** Two's complement mode control bit 0 = Output binary format 1 = Output2's complement format	0	
		<4:0>	**SLEEP: NAP_4:NAP_3:NAP_2:NAP_1 Sleep/ Standby mode control bit** 00000 = **Normal operating mode** 0XXX1 = Channel1 is in standby mode 0XX1X = Channel2 is in standby mode 0X1XX = Channel3 is in standby mode 01XXX = Channel4 is in standby mode 1XXXX = Sleep mode. All channels stop working.	00000	
A2	02	<7:5>	**ILVDS2: ILVDS0LVDS** Output current control bit 000 = 3.5mA LVDS Output Driver Current 001 = 4.0mA LVDS Output Driver Current 010 = 4.5mA LVDS Output Driver Current 011 = Not used 100 = 1.75 mA LVDS Output Driver Current 101 = 2.0 mA LVDS Output Driver Current 110 =2.5 mA LVDS Output Driver Current 111 = 3.0 mA LVDS Output Driver Current	000	80
		<4>	**TERMON**LVDS Internal termination resistor gating bit 0 = Do not use chip internalLVDS termination resistor 1 = Use chip internalLVDS termination resistor	0	
		<3>	**OUTOFF** Output disable bit 0 = Normal digital output 1 = Turn off digital output	0	
		<2>	**OUTMODE** Digital output mode control bit 0= Dual-lane14 bit serial mode 1= Single-lane14 bit serial mode	0	
		<1:0>	X Not used	X	
A3	03	<7>	**OUTTEST** Digital output test mode control bit 0= Normal data output 1= Output test vector	0	
		<6>	X Unused, irrelevant bits.	X	
		<5:0>	**TP<13:8>** Test mode data bits (MSB) Used to set the highest bit of the test vector, bit13 (MSB) to data bit8.	0	
A4	04	<7:0>	**TP<7:0>** Test mode data bits (MSB) Used to set the highest bit of the test vector, bit7 to data bit0 (LSB).	0	
A5	05	<7:6>	Internal, not open. Keep 0000000.	0000000	
		<1>	Encoding clock receive module disable bit, can be used with standby mode 0 = Normal operation 1 = Disabled	0	

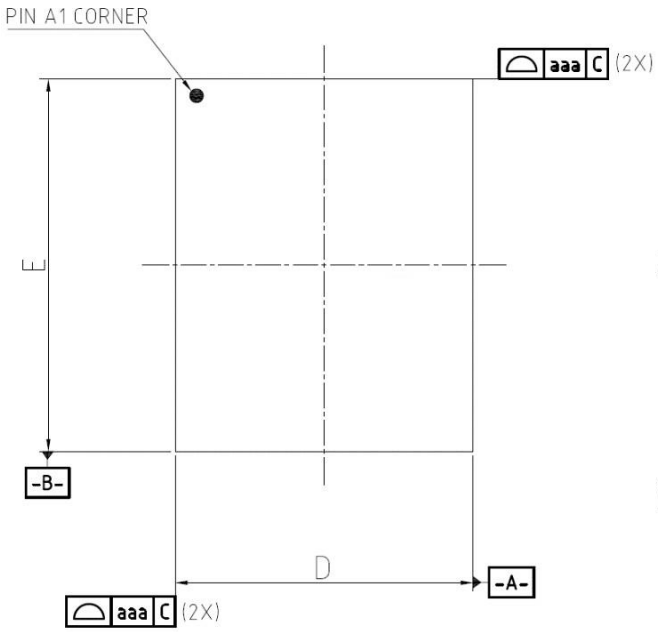
Table 14. Serial programming mode register mapping table (PAR/SER = GND)

Typical Applications

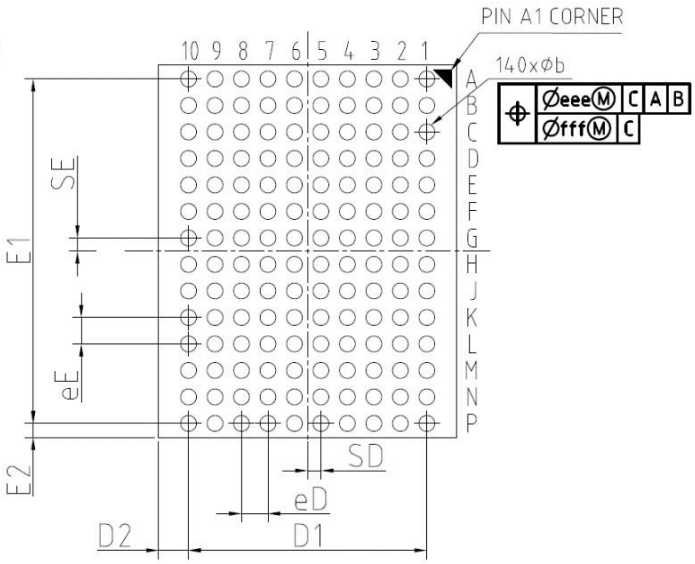
Top Surface	Inner Layer2	Inner Layer3
		
Inner Layer4	**Inner Layer5**	**Bottom Surface**
		



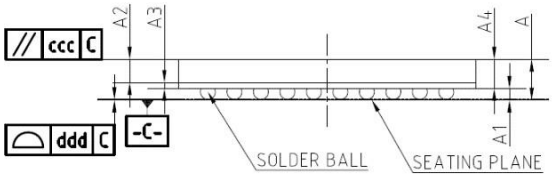
Package Description



Top View



Bottom View



Side View

ITEM.		SYM.	DIMENSION (mm)		
			MIN.	NOM.	MAX.
Body Size	X	D	8.90	9.00	9.10
	Y	E	11.15	11.25	11.35
Ball Pitch	X	eD	---	0.80TYP	---
	Y	eE	---	0.80TYP	---
Mold Thickness		A2	0.68	0.70	0.71
Substrate Thickness		A3	0.28	0.32	0.36
Substrate+Mold Thickness+Mold Gap		A4	0.96	1.02	1.07
Total Thickness		A	---	---	1.62
Ball Diameter			---	0.50	---
Ball Stand Off		A1	0.35	0.40	0.45
Ball Width		Øb	0.45	0.50	0.55
Package Edge Tolerance		aaa	---	0.15	---
Mold Flatness		ccc	---	0.10	---
Coplanarity		ddd	---	0.12	---
Ball offset(Package)		eee	---	0.15	---
Ball offset(Ball)		fff	---	0.08	---
Edge Ball Center to Center	X	D1	---	7.20TYP	---
	Y	E1	---	10.40TYP	---
Edge Ball Center to Package Edge	X	D2	0.80	0.90	1.00
	Y	E2	0.325	0.425	0.525
Ball Center to Body Center	X	SD	---	0.40TYP	---
	Y	SE	---	0.40TYP	---