TGS9009

50 MHz - 6 GHz Wideband RF Transceiver

Data sheet

Product Description

TGS9009 is a highly integrated, flexible and easy-to-use RF transceiver that provides dual-channel transmitters and dual-channel receivers, integrated frequency synthesizers and powerful digital signal processing units. The receiving path (Rx) consists of two independent direct conversion receivers with a bandwidth of up to 200 MHz and a high dynamic range. The feedback path (ORx) uses a feedback channel with a bandwidth of 450 MHz.

Channel receiver. The complete digital receiving channel includes automatic and manual attenuation control, DC offset correction (DCOC), quadrature error correction (QEC) and digital filtering, thus eliminating the need for these functions in the digital baseband part. The chip integrates fast automatic gain control (AGC) and also has flexible external gain control mode.

The receiving path (Rx) uses a continuous-time Σ-Δ ADC to directly digitize the signal. Compared with traditional intermediate frequency (IF) reception, direct conversion reception does not cause out-of-band image mixing or reduces aliasing, making the requirements for anti-aliasing filters lower and can reduce the requirements for RF filters.

The transmit channel (Tx) uses an innovative direct conversion modulator with a bandwidth of up to 450 MHz, achieving extremely high modulation accuracy and extremely low in-band and out-of-band noise. It supports time division duplexing (TDD) and frequency division duplexing (FDD) working modes; in conjunction with the feedback channel receiver (ORx), it implements the digital pre-distortion (DPD) function in the TDD scenario.

The chip integrates a full-featured phase-locked loop (PLL), including components such as a voltage-controlled oscillator (VCO) and a loop filter, to provide high-performance, low-power fractional-N RF frequency synthesis for the transmitter (Tx) and receiver (Rx) signal paths, while also generating the clock signals required by various functional units such as ADC and DAC converters, digital circuits and serial interfaces.

It integrates numerous auxiliary functions such as general-purpose analog-to-digital converters (ADCs), general-purpose digital-to-analog converters (DACs), and general-purpose input/output (GPIOs) interface signals for power amplifier (PA) and RF front-end control.

Supports high-speed JESD204B interface, with a channel rate of up to 12.288 Gbps.

TGS9009 can be powered directly by 1.3 V and 1.8 V externally and controlled by standard 4-wire SPI.

B20 package: 12 mm × 12 mm, 196-ball CSP_BGA.

Main features

- Integrated two-channel transmitter supports 50 MHz ~ 6 GHz adjustable
- Integrated two-channel receiver supports 50 MHz ~ 6 GHz adjustable
- Maximum bandwidth of transmitter: 450 MHz

- Maximum bandwidth of receiver: 200 MHz
- Maximum bandwidth of feedback channel: 450 MHz
- Integrated fractional N 9-frequency RF frequency synthesis
- Support frequency hopping
- Integrated automatic DC/LOL/IMR calibration algorithm
- Integrated automatic control algorithm of receiving path gain
- JESD204B interface
- Adopt 12mm×12mm, 196-ball CSP_BGA package.

Application

- 5G macro/micro/pico base stations
- Large-scale 9-layer antennas • Electronic warfare
- Phased array radar • Specialized communications • Satellite communications

Selection

- TGS9009, industrial grade, temperature range: -40°C ~ 85°C
- TGS9009K, wide temperature industrial grade, temperature range: -55°C ~ 125°C
- TGS9009N, general military grade, temperature range: -55°C ~ 125°C

Functional block diagram

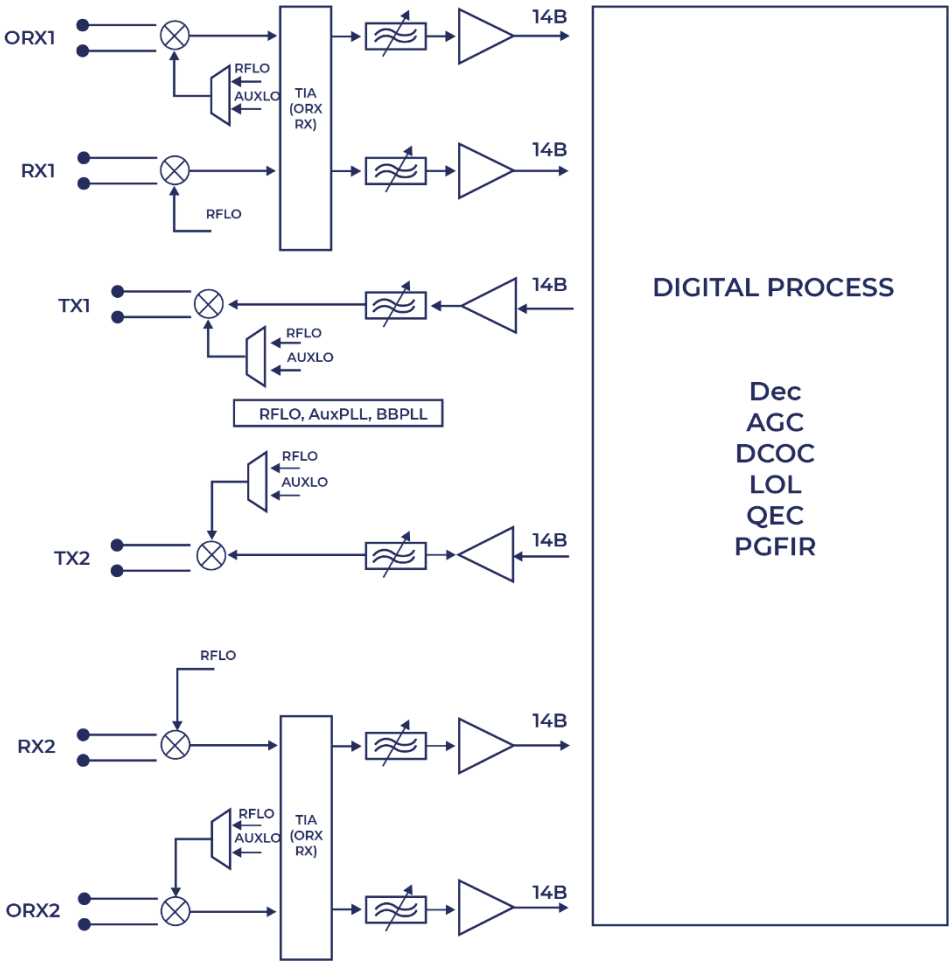


Figure 1. Functional block diagram

Parameter index

Table 1. Device performance parameters

Parameter	Test conditions	Unit	Min.	Typ.	Max.
Transmit channel Tx					
Carrier frequency		MHz	50		6000
Transmit signal bandwidth		MHz	100	450	456
Transmit large signal bandwidth		MHz	<100	200	400
Transmit power attenuation range		dB	0		32
Transmit power attenuation resolution		dB		0.5	
Adjacent channel leakage ratio ACLR@20MLTE/-12dBFs	50 MHz ~ 3 GHz	dB		-65	
	3 GHz ~ 6 GHz	dB		-62	
In-band noise floor	50 MHz ~ 3 GHz	dBm/Hz		-148	
	3 GHz ~ 6 GHz	dBm/Hz		-150	
Out-of-band noise floor	50 MHz ~ 3 GHz	dBm/Hz		-153	
	3 GHz ~ 6 GHz	dBm/Hz		-155	
TX1 TX2 Isolation	50 MHz ~ 3 GHz	dB		76	
	3 GHz ~ 6 GHz	dB		63	
In-band image rejection	|BW| < 100 MHz @ 50 MHz ~ 3 GHz	dB		68	
	|BW| < 100 MHz @ 3 GHz ~ 6 GHz	dB		60	
Out-of-band image rejection	200 MHz ~ 450 MHz	dB		43	
Maximum output power	50 MHz ~ 3 GHz	dBm		9	
	3 GHz ~ 6 GHz	dBm		7	
OIP3	50 MHz ~ 3 GHz	dBm		27	
	3 GHz ~ 6 GHz	dBm		23	
Carrier leakage	50 MHz ~ 3 GHz	dBFS		-78	
	3 GHz ~ 6 GHz	dBFS		-75	
EVM	50 MHz ~ 3 GHz	%		1	
	3 GHz ~ 6 GHz	%		1.2	
Feedback channel FBRx					
Carrier frequency		MHz	50		6000
Gain adjustment range		dB		32	
Gain adjustment step		dB		0.25	
Received signal bandwidth		MHz	200	200	450
Maximum input signal power		dBm			
IIP2		dBm		62	
IIP3		dBm		12	
IM3		dBc		-65	
Image suppression		dBc		-60	
Input impedance	Difference	ohm		100	
Receive channel Rx					
Carrier frequency		MHz	50		6000
Gain adjustment range		dB		32	
Gain adjustment step		dB		0.25	
Received signal bandwidth		MHz	100	200	225
Maximum input signal power		dBm		-13	-5

Noise figure		dB		13	
IIP2		dBm		62	
IP3		dBm		12	
IM3		dBc		-65	
Image suppression		dBc		-60	
Input impedance	Difference	Ohm		100	
Frequency Synthesizer					
Input frequency range		MHz	96	122.88	125
Local oscillator (LO) frequency adjustment step		Hz		2	2.3
Plotting Phase Noise 1900 MHz LO (PLL Loop BW 50 KHz)	At 100 kHz offset	dBc/Hz		-100	
	At 400 kHz offset	dBc/Hz		-118	
	At 10 MHz offset	dBc/Hz		-141	
Plotting Phase Noise 3800 MHz LO (PLL loop bandwidth 300 KHz)	At 100 kHz offset	dBc/Hz		-100	
	At 1 MHz offset	dBc/Hz		-120	
	At 10 MHz offset	dBc/Hz		-135	
Plotting Phase Noise 5900 MHz LO (PLL loop bandwidth 300 KHz)	At 100 kHz offset	dBc/Hz		-100	
	At 1 MHz offset	dBc/Hz		-118	
	At 10 MHz offset	dBc/Hz		-135	
Integrated phase noise 1900 MHz LO	PLL loop bandwidth 50 kHz	o_{rms}		0.22	
Integrated phase noise 3800 MHz LO	PLL loop bandwidth 300 KHz	o_{rms}		0.38	
Integrated phase noise 5900 MHz LO	PLL loop bandwidth 300 KHz	o_{rms}		0.57	
1.8 V/2.5 V digital interface (SPI, GPIO_x, TXx_ENABLE, RXx_ENABLE, $\overline{\text{RESET}}$)					
VDD_INTERFACE (VDD_I)	Interface voltage	V		1.8/2.5	
VIH	High level input voltage	V	VDD_ Ix0.8		VDD_I
VIL	Low level input voltage	V	0		VDD_Ix0.2
VOH	High level input voltage	V	VDD_ Ix0.8		
VOL	Low level input voltage	V			VDD_Ix0.2
3.3V digital interface (GPIO_3P3_x)					
VDDA_3P3	Interface voltage	V		3.3	
VIH	High level input voltage	V	VDDA_3 P3x0.8		VDDA_3P3
VIL	Low level input voltage	V	0		VDDA_3P3x 0.2
VOH	High level input voltage	V	VDDA_3 P3x0.8		
VOL	Low level input voltage	V			VDDA_3P3x 0.2
Analog interface (AUX ADC/DAC)					
Input level range		V	0.05		VDDA_3P3 – 0.05
Output level range		V	0.7		VDDA_3P3 – 0.3

Recommended working conditions

Table 2. Recommended Operating Conditions

Symbol	Describe	Minimum value	Typical value	Maximum value	Unit
Power supply					
VDDA1P3[1]	Analog 1.3V power supply	1.27	1.3	1.33	V
VDDD1P3_DIG	Digital 1.3V power supply	1.27	1.3	1.33	V
VDDA1P8_TX	Analog 1.8V transceiver supply	1.71	1.8	1.89	V
VDDA1P8_BB	Analog 1.8V baseband power supply	1.71	1.8	1.89	V
VDD_INTERFACE	Digital interface power supply	1.71	1.8/2.5	2.63	V
VDDA_3P3	Analog 3.3V power supply	3.14	3.3	3.47	V

[1] VDDA1P3 indicates all analog 1.3V supply voltage.

Device power-on sequence description: B20 requires a specific power-on sequence to avoid unexpected power-on current. The best power-on sequence is as follows: VDDD1P3_DIG and VDDA1P3 power supplies (VDDA1P3 includes all analog 1.3V power supplies) are powered on at the same time. If these two power supplies cannot be powered on at the same time, the VDDD1P3_DIG power supply must be powered on first. Then after the above 1.3 V power supplies are turned on, power on the VDDA_3P3, VDDA1P8_BB, VDDA1P8_TX, VDDA1P3_DES, and VDDA1P3_SER power supplies. There is no special order requirement for the VDD_INTERFACE power supply. The device power-off sequence is not strict. If possible, disconnect the VDDD1P3_DIG power supply last.

Extreme working conditions

Warning: The extreme operating voltage parameters are shown in Table 3. Exceeding these values may cause chip damage and reliability issues. Table 3. Extreme operating conditions (analog voltage reference VSSA, digital voltage reference VSSD)

Parameter	Scope
VDDA1P3[1]	−0.3 V to +1.4 V
VDDD1P3_DIG	−0.3 V to +1.4 V
VDD_INTERFACE	−0.3 V to +3.0 V
VDDA_3P3	−0.3 V to +3.9 V
VDDA1P8_TX, VDDA1P8_BB	−0.3 V to +2.0 V
1.8/2.5 digital interface input and output signals	−0.3 V to VDD_ INTERFACE + 0.3 V
JESD204B signal output	−0.3 V to VDDA1P3_SER
JESD204B signal input	−0.3 V to VDDA1P3_DES +0.3 V
Signal pin input current (excluding power pins)	±10 mA
Maximum input level of RF channel	23 dBm (peak)
Transmitter maximum voltage standing wave ratio (VSWR)	3:1
Maximum Junction Temperature (TJ)	110°C
Storage temperature	−65°C to +150°C

[1] VDDA1P3 indicates all analog 1.3V supply voltage.

Pin description

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSSA	ORX2_IN+	ORX2_IN–	VSSA	RX2_IN+	RX2_IN–	VSSA	VSSA	RX1_IN+	RX1_IN–	VSSA	ORX1_IN+	ORX1_IN–	VSSA
B	VDDA1P3_RX_RF	VSSA	VSSA	VSSA	VSSA	VSSA	RF_EXT_LO_I/O–	RF_EXT_LO_I/O+	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
C	GPIO_3P3_0	GPIO_3P3_3	VDDA1P3_RX_TX	VSSA	VDDA1P3_RF_VCO_LDO	VDDA1P3_RF_VCO_LDO	VDDA1P1_RF_VCO	VDDA1P3_RF_LO	VSSA	VDDA1P3_AUX_VCO_LDO	VSSA	VDDA_3P3	GPIO_3P3_9	RBIAS
D	GPIO_3P3_1	GPIO_3P3_4	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VDDA1P1_AUX_VCO	VSSA	VSSA	GPIO_3P3_8	GPIO_3P3_10
E	GPIO_3P3_2	GPIO_3P3_5	GPIO_3P3_6	VDDA1P8_BB	VDDA1P3_BB	VSSA	REF_CLK_IN+	REF_CLK_IN–	VSSA	ANA_TP	AUXADC_3	VDDA1P8_TX	GPIO_3P3_7	GPIO_3P3_11
F	VSSA	VSSA	AUXADC_0	AUXADC_1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	AUXADC_2	VSSA	VSSA	VSSA
G	VSSA	VSSA	VSSA	VSSA	VDDA1P3_CLOCK_SYNTH	VSSA	VDDA1P3_RF_SYNTH	VDDA1P3_AUX_SYNTH	RF_SYNTH_VTUNE	VSSA	VSSA	VSSA	VSSA	VSSA
H	TX2_OUT–	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	GPIO_12	GPIO_11	VSSA	TX1_OUT–
J	TX2_OUT+	VSSA	GRIO_18	$\overline{\text{RESET}}$	GP_INTERRUPT	NC_1	GPIO_2	GPIO_1	SDIO	SDO	GPIO_13	GPIO_10	VSSA	TX1_OUT+
K	VSSA	VSSA	SYSREF_IN+	SYSREF_IN–	GPIO_5	GPIO_4	GPIO_3	GPIO_0	SCLK	$\overline{\text{CS}}$	GPIO_14	GPIO_9	VSSA	VSSA
L	VSSA	VSSA	$\overline{\text{SYNCIN1}}$–	$\overline{\text{SYNCIN1}}$+	GPIO_6	GPIO_7	VSSD	VDDD1P3_DIG	VDDD1P3_DIG	VSSD	GPIO_15	GPIO_8	$\overline{\text{SYNCOUT1}}$–	$\overline{\text{SYNCOUT1}}$+
M	VDDA1P1_CLOCK_VCO	VSSA	$\overline{\text{SYNCIN0}}$–	$\overline{\text{SYNCIN0}}$+	RX1_ENABLE	TX1_ENABLE	RX2_ENABLE	TX2_ENABLE	VSSA	GPIO_17	GPIO_16	VDD_INTERFACE	$\overline{\text{SYNCOUT0}}$–	$\overline{\text{SYNCOUT0}}$+
N	VDDA1P3_CLOCK_VCO_LDO	VSSA	SERDOUT3–	SERDOUT3+	SERDOUT2–	SERDOUT2+	VSSA	VDDA1P3_SER	VDDA1P3_DES	SERDIN1–	SERDIN1+	SERDIN0–	SERDIN0+	VSSA
P	CLOCK_SYNTH_VTUNE	VSSA	VSSA	SERDOUT1–	SERDOUT1+	SERDOUT0–	SERDOUT0+	VDDA1P3_SER	VDDA1P3_DES	VSSA	SERDIN3–	SERDIN3+	SERDIN2–	SERDIN2+

Table 4. Pin I/0 Type Description

I/0	Description
Input	Input signal
Output	Output signal
Input/ output	Bidirectional input/output signal
Power	Power supply
Ground	Ground

Table 5. Pin arrangement and description

Pin location	Type	Name	Describe
A1, A4, A7, A8, A11, A14, B2 -B6, B9 -B14, C4, C9, C11, D3 - D9, D11, D12, E6, E9, F1, F2, F5 - F10, F12 - F14, G1 - G4, G6, G10 -G14, H2 - H10, H13, J2, J13, K1, K2, K13, K14, L1, L2, M2, M9, N2, N7, N14, P2, P3, P10	Ground	VSSA	Analog ground
A2, A3	Input	ORX2_IN+, ORX2_IN−	Feedback channel 2 differential input. Connect to ground when not used in design.
A5, A6	Input	RX2_IN+, RX2_IN−	Receive channel 2 differential input. Connect to ground when not used in design.
A9, A10	Input	RX1_IN+, RX1_IN−	Receive channel 1 differential input. Connect to ground when not used in design.
A12, A13	Input	ORX1_IN-, ORX1_IN+	Feedback channel 1 differential input. Connect to ground when not used in design.
B1	Power	VDDA1P3_RX_RF	Feedback channel receives power supply, 1.3 V.
B7, B8	Input/ output	RF_EXT_LO_I/O−, RF_EXT_LO_I/O+,	External local oscillator (LO) input or internal local oscillator (LO) output. When using an external local oscillator (LO), the input frequency must be twice the expected carrier. If not used in the design, leave it unconnected.
C1	Input/ output	GPIO_3P3_0	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_6 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
C2	Input/ output	GPIO_3P3_3	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_9 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
C13	Input/ output	GPIO_3P3_9	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_3 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
D1	Input/ output	GPIO_3P3_1	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_7 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
D2	Input/ output	GPIO_3P3_4	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_10 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.

D13	Input/ output	GPIO_3P3_8	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_2 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
D14	Input/ output	GPIO_3P3_10	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_4 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
E1	Input/ output	GPIO_3P3_2	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_8 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
E2	Input/ output	GPIO_3P3_5	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_11 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
E3	Input/ output	GPIO_3P3_6	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_0 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
E13	Input/ output	GPIO_3P3_7	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_1 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
E14	Input/ output	GPIO_3P3_11	3.3 V general-purpose input and output pin, which can be configured as AUXDAC_5 function. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
C3	Power	VDDA1P3_RX_TX	Receiver and transmitter baseband circuits, transimpedance amplifier (TIA), transmit transconductance (GM), baseband filter and AUDDAC power supply, 1.3 V.
C5, C6	Power	VDDA1P3_RF_VCO_LDO	RF VCO LDO power supply, 1.3 V. C5 and C6 pins are connected together. Use a separate power line to connect to the power plane.
C7	output	VDDA1P1_RF_VCO	RF_VCO 1.1 V output, cannot be powered externally. Place a 1μF decoupling capacitor on this pin.
C8	Power	VDDA1P3_RF_LO	RF synthesizer local oscillator (LO) power supply, this pin is sensitive to power supply noise.
C10	Power	VDDA1P3_AUX_VCO_LDO	AUX_VCO_LDO power supply, 1.3 V.
C12	Power	VDDA_3P3	General purpose output pin pull-up and AUXDAC power supply, 3.3 V.
C14	Input/ output	RBIAS	Bias resistor, use 14.3 kΩ 1% to ground. This pin generates internal current based on the external bias resistor.

D10	output	VDDA1P1_AUX_VCO	AUX_VCO 1.1 V output, cannot be powered externally. Place a 1 μF decoupling capacitor on this pin.
E4	Power	VDDA1P8_BB	ADC, DAC and AUXADC power supply, 1.8 V.
E5	Power	VDDA1P3_BB	ADC, DAC and AUXADC power supply, 1.3 V.
E7, E8	Input	REF_CLK_IN+, REF_CLK_IN−	Device differential clock input.
E10	Output	ANT_TP	Test pin, it is recommended to keep the test point.
E12	Power	VDDA1P8_TX	Transmit path 1.8 V power supply.
F3, F4, F11, E11	Input	AUXADC_0 to AUXADC_3	Auxiliary ADC input, when not used in the design, connect to ground through a resistor or directly to ground.
G5	Power	VDDA1P3_CLOCK_ SYNTH	Clock synthesizer power supply, 1.3 V. Use a separate power line to connect to the power plane.
G7	Power	VDDA1P3_RF_SYNTH	RF synthesizer power supply, 1.3 V. This pin is sensitive to power supply noise.
G8	Power	VDDA1P3_AUX_SYNTH	Auxiliary synthesizer supply, 1.3 V.
G9	Output	RF_SYNTH_VTUNE	The RF synthesizer adjusts the voltage output.
H11	Input/ output	GPIO_12	1.8 V to 2.5 V general-purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
H12	Input/ output	GPIO_11	1.8 V to 2.5 V general-purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
J11	Input/ output	GPIO_13	1.8 V to 2.5 V general-purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
J12	Input/ output	GPIO_10	1.8 V to 2.5 V general-purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
J3	Input/ output	GPIO_18	1.8 V to 2.5 V general purpose input/output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. Not used in the design When the output is low, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
J7	Input/ output	GPIO_2	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
J8	Input/ output	GPIO_1	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
K5	Input/ output	GPIO_5	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.

K6	Input/ output	GPIO_4	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
K7	Input/ output	GPIO_3	1.8 V to 2.5 V general-purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
K8	Input/ output	GPIO_0	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
K11	Input/ output	GPIO_14	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
K12	Input/ output	GPIO_9	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
L5	Input/ output	GPIO_6	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
L6	Input/ output	GPIO_7	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
L11	Input/ output	GPIO_15	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
L12	Input/ output	GPIO_8	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
M10	Input/ output	GPIO_17	1.8 V to 2.5 V general purpose input and output pin. Since this pin contains the input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
M11	Input/ output	GPIO_16	1.8 V to 2.5 V general-purpose input and output pin. Since this pin contains input function circuit, the input voltage needs to be controlled. When not used in the design, it needs to be grounded through a resistor or kept floating and configured in low-level output mode.
H14, J14	Output	TX1_OUT-, TX1_OUT+	Transmit channel 1 differential output. Leave it unconnected if not used in the design.
H1, J1	Output	TX2_OUT−, TX2_OUT+	Transmit channel 2 differential output. Leave it unconnected if not used in the design.
J4	Input	$\overline{\text{RESET}}$	Reset pin, low level is valid.

J5	Output	GP_INTERRUPT	General interrupt output pin, when not used in the design, keep it floating and unconnected.
J6	Input	NC_1	NC pin, keep it floating and unconnected.
J9	Input/ output	SDIO	Serial input in 4-wire SPI mode and serial input and output in 3-wire SPI mode.
J10	Output	SDO	Serial output in 4-wire SPI mode, leave it floating in 3-wire SPI mode.
K3, K4	Input	SYSREF_IN+, SYSREF_IN−	JESD204B system reference signals, LVDS differential input.
K9	Input	SCLK	SPI clock signal.
K10	Input	$\overline{CS}$	SPI chip select signal, low voltage is valid.
L3, L4	Input	$\overline{SYNCIN1}$ −, $\overline{SYNCIN1}$ +	JESD204B synchronization signal 1, paired RF input channel data, LVDS differential input, when not used in the design, grounded through a pull-down resistor or directly grounded.
L7, L10	Ground	VSSD	Digitally.
L8, L9	Power	VDDD1P3_DIG	Digital core power supply, 1.3V. L8 and L9 pins are connected together. Use wide power traces to connect to the power plane.
L13, L14	Output	$\overline{SYNCOUT1}$ -, $\overline{SYNCOUT1}$ +	JESD204B synchronization signal 1, paired RF output channel data, LVDS differential output, when not used in the design, keep it floating and unconnected.
M1	Output	VDDA1P1_CLOCK_VCO	CLOCK_VCO 1.1V output, cannot be powered externally. Place a 1μF decoupling capacitor on this pin.
M3, M4	Input	$\overline{SYNCIN0}$-, $\overline{SYNCIN0}$+	JESD204B synchronization signal 0, paired RF input channel data, LVDS differential input, when not used in the design, grounded through a pull-down resistor or directly grounded.
M5	Input	RX1_ENABLE	RF receiving channel 1 enable signal, high level is valid, when not used in the design, it is grounded through a pull-down resistor or directly grounded.
M6	Input	TX1_ENABLE	RF transmit channel 1 enable signal, high level is valid. When not used in the design, it is grounded through a pull-down resistor or directly grounded.
M7	Input	RX2_ENABLE	RF receiving channel 2 enable signal, high level is valid, when not used in the design, it is grounded through a pull-down resistor or directly grounded.
M8	Input	TX2_ENABLE	RF transmission channel 2 enable signal, high level is valid, when not used in the design, it is grounded through a pull-down resistor or directly grounded.
M12	Power	VDD_INTERFACE	Digital input and output interface power supply, 1.8V or 2.5 V.
M13, M14	Output	$\overline{SYNCOUT0}$-, $\overline{SYNCOUT0}$+	JESD204B synchronization signal 0, paired RF output channel data, LVDS differential output, when not used in the design, keep it floating and unconnected.
N1	Power	VDDA1P3_CLOCK_VCO_ LDO	1.3 V power supply, connected to the power plane using a separate power line.
N3, N4	Output	SERDOUT3−, SERDOUT3+	JESD204B signal, CML differential output 3, when not used in the design, leave it floating and unconnected.
N5, N6	Output	SERDOUT2−, SERDOUT2+	JESD204B signal, CML differential output 2. Leave it floating and unconnected if not used in the design.
N8, P8	Power	VDDA1P3_SER	JESD204B serializer supply, 1.3 V.
N9, P9	Power	VDDA1P3_DES	JESD204B deserializer supply, 1.3 V.
N10, N11	Input	SERDIN1−, SERDIN1+	JESD204B data signal, CML differential input 1, leave it floating when not used in the design.
N13, N12	Input	SERDIN0+, SERDIN0−	JESD204B data signal, CML differential input 0, when not used in the design, leave it floating and

			unconnected.
P1	Output	CLOCK_SYNTH_VTUNE	Clock synthesizer adjusts voltage output
P4, P5	Output	SERDOUT1−, SERDOUT1+	JESD204B data signal, CML differential output 1, if not used in the design, leave it floating and unconnected.
P6, P7	Output	SERDOUT0−, SERDOUT0+,	JESD204B data signal, CML differential output 0. If not used in the design, leave it floating and unconnected.
P11, P12	Input	SERDIN3−, SERDIN3+	JESD204B data signal, CML differential input 3, when not used in the design, leave it floating and unconnected.
P13, P14	Input	SERDIN2−, SERDIN2+	JESD204B data signal, CML differential input 2, leave it floating when not used in the design.

Power consumption information

Specification	BW	Working frequency point	Quiet power consumption (W)	Working (Full bandwidth) (w)
2Tx2Rx	TX400M/Rx200M	3G	3.8	5.07
2Tx1ORx	TX400M/ORx400M	3G	3.05	4.11
1Tx1ORx	TX400M/ORx400M	3G	2.47	3.1
1Tx1Rx	TX400M/Rx200M	3G	2.41	3.17
1Tx	TX400M	3G	2.27	2.61
1Rx	Rx200M	3G	1.78	2
1ORx	ORx400M	3G	2.05	2.24

SPI

The TGS9009 chip integrates an SPI slave controller. The master baseband controller (BBP) can control and configure TGS9009 related parameters and detect the chip operation status through the SPI interface. TGS9009 supports the standard 4-wire SPI bus mode.

The SPI bus consists of SCLK, $\overline{CS}$n, SDIO and SDO pin signals.

- SCLK: serial clock (master device output)
- SDIO: serial data input (master device output, slave device input)
- SDO: serial data output (master device input, slave device output)
- $\overline{CS}$n: chip select signal (master device output, low level is valid)

When the $\overline{CS}$n signal is input high, the SDO and SDIO pins transition to a high impedance state. The TGS9009 does not provide pull-up or pull-down resistors on these pins.

When SDO is inactive, it is in a high impedance state. If the master device always needs to provide a valid logic state on SDO, a pull-up/pull-down value needs to be added on the printed circuit board (PCB) 10 kΩ is recommended.

SPI Bus Protocol

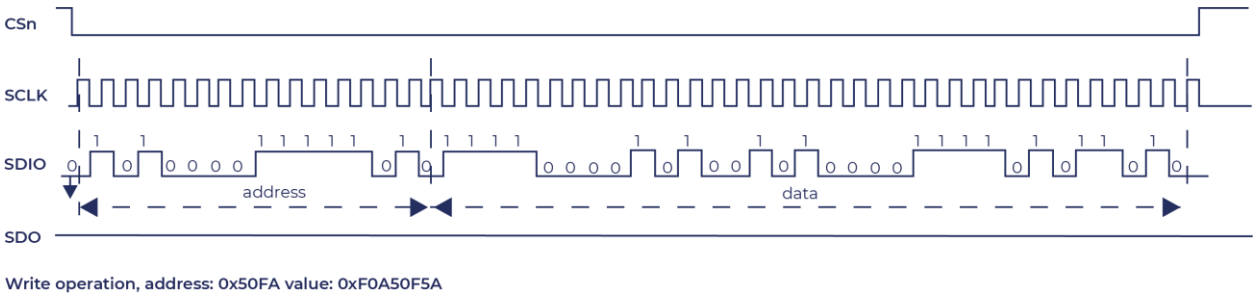


Figure 4. SPI write operation diagram

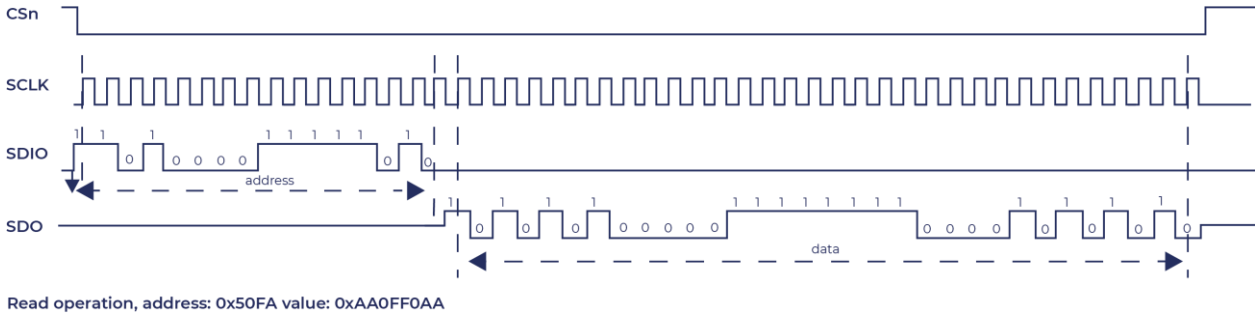


Figure 5. SPI read operation diagram

The SPI interface of TGS9009 supports the standard mode0 communication mode, that is, the master device needs to configure two parameters.

- Clock polarity (CPOL) = 0;
- Clock phase (CPHA) = 0;

SPI interface communication timing parameters

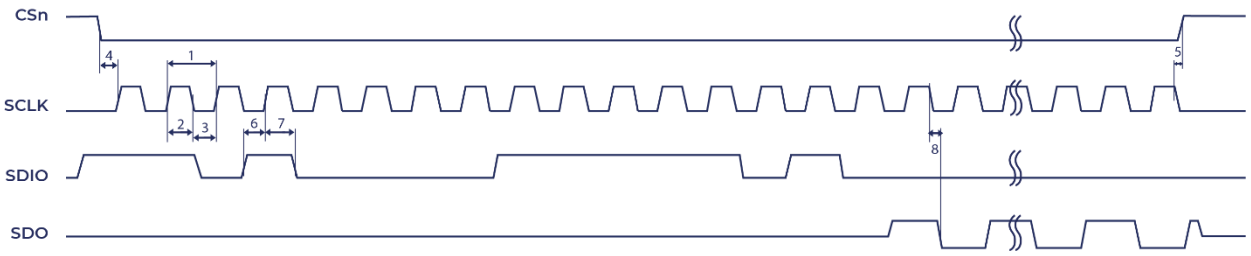


Figure 6. SPI read and write operation timing diagram

The following table describes the parameters in Figure 6.

Serial number	Parameter	Symbol	Minimum value	Typical value	Maximum value	Unit
1	SCLK Period	Tc	-	50	-	ns
2	SCLK High Pulse Duty Cycle	Thdc	40	-	60	%
3	SCLK Low Pulse Duty Cycle	Tldc	40	-	60	%
4	Setup time, $\overline{CS}$n falling edge to SCLK rising edge (start of the communication)	Tsu1	3	-	-	ns
5	Hold time, SCLK falling edge to $\overline{CS}$n rising edge (End of the communication)	Th1	1	-	-	ns
6	Setup time, SDIO valid before SCLK rising edge	Tsu2	3	-	-	ns
7	Hold time, SDIO valid after SCLK rising edge	Th2	1	-	-	ns
8	Delay time, SCLK falling edge to SDO valid	Td1	-	6	12	ns

Package information

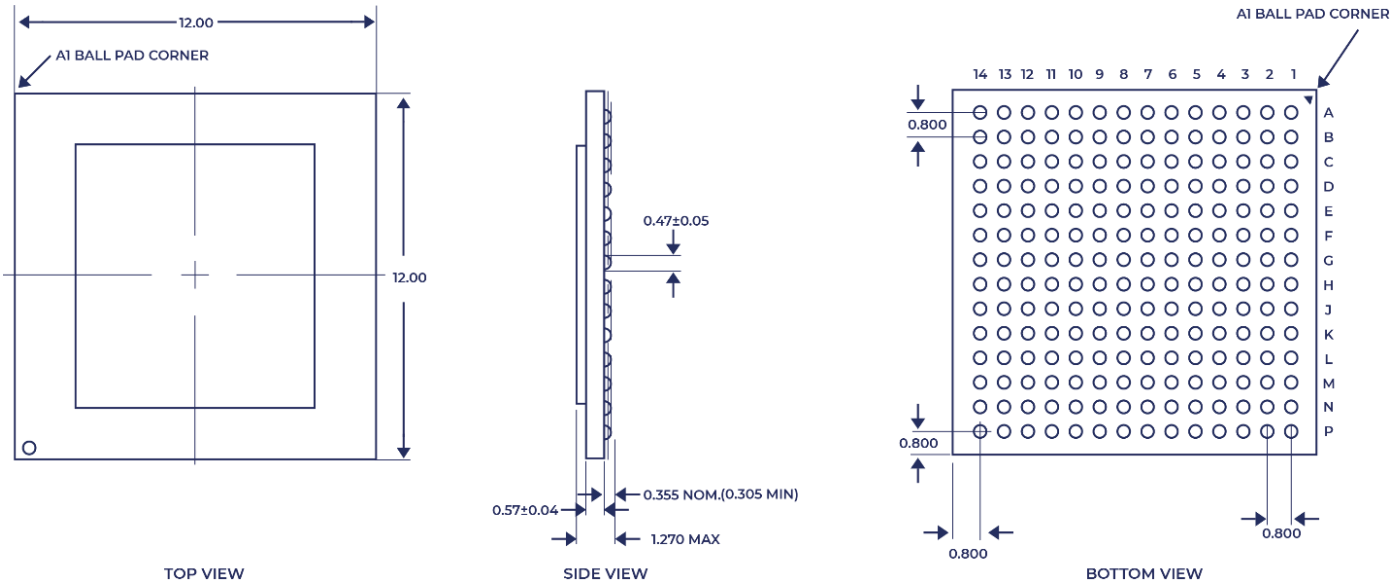


Figure 4. 196-pin CSP_BGA package (Chip Scale Package Ball Grid Array)

Notes:

1. All dimensions in the figure are in millimeters (mm)

2. This dimension is the maximum solder ball diameter tested after reflow soldering

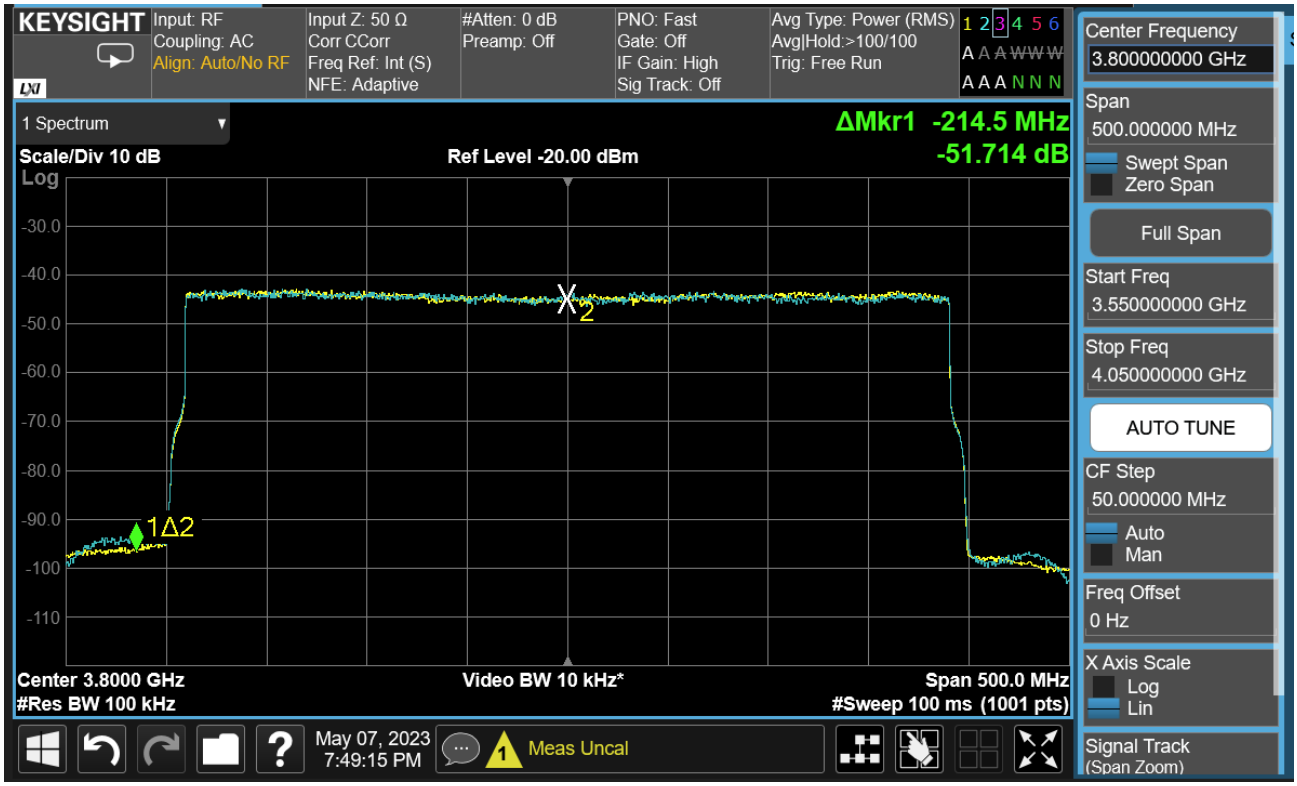
Typical test results

- **LO leakage**

Frequency GHz	1.8	2.6	3	3.5	4	4.5	5	5.5
Correction performance dBm	-66.84	-59.51	-68.1	-75.58	-67.49	-63.90	-77.27	-70.72

- **Flatness**

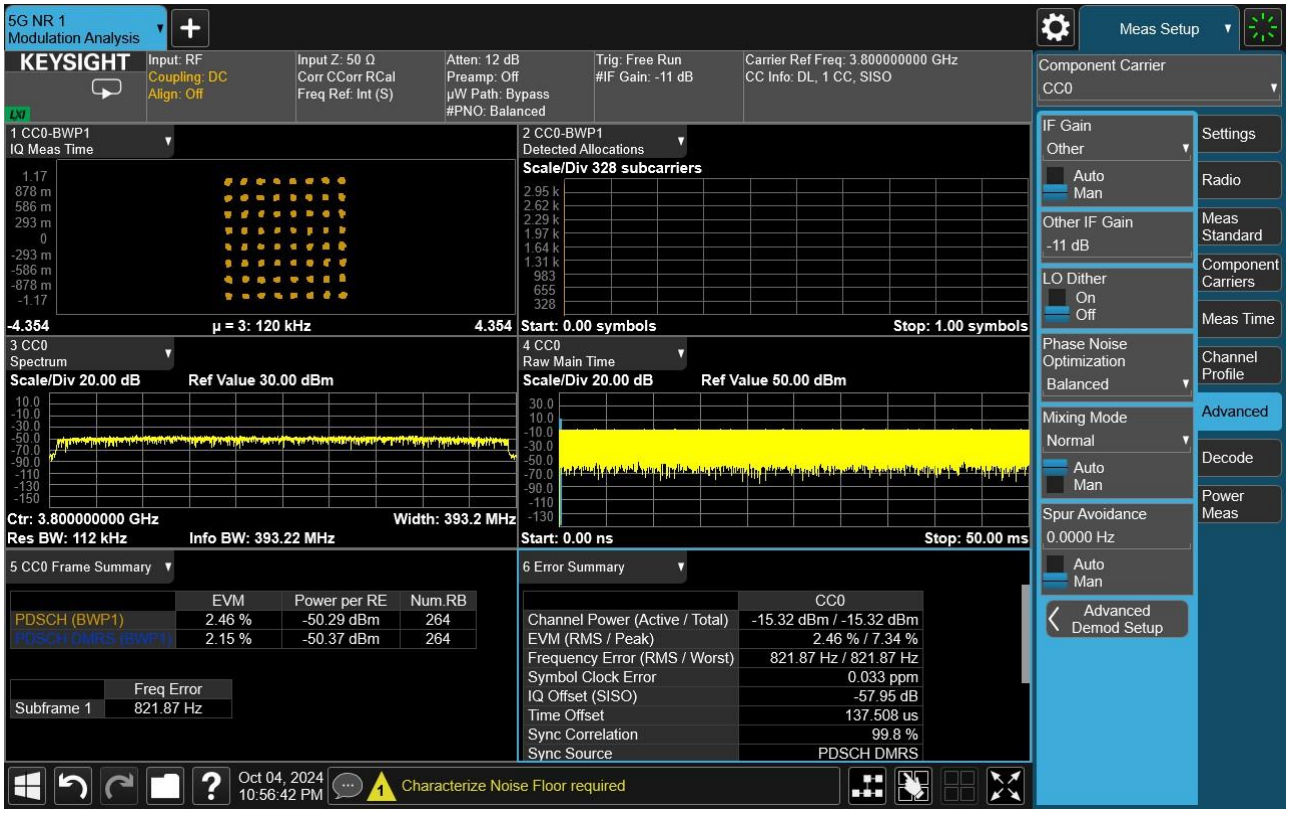
Test 3.8 G flatness, compared with foreign competitors (green is foreign competitors)



- **EVM**

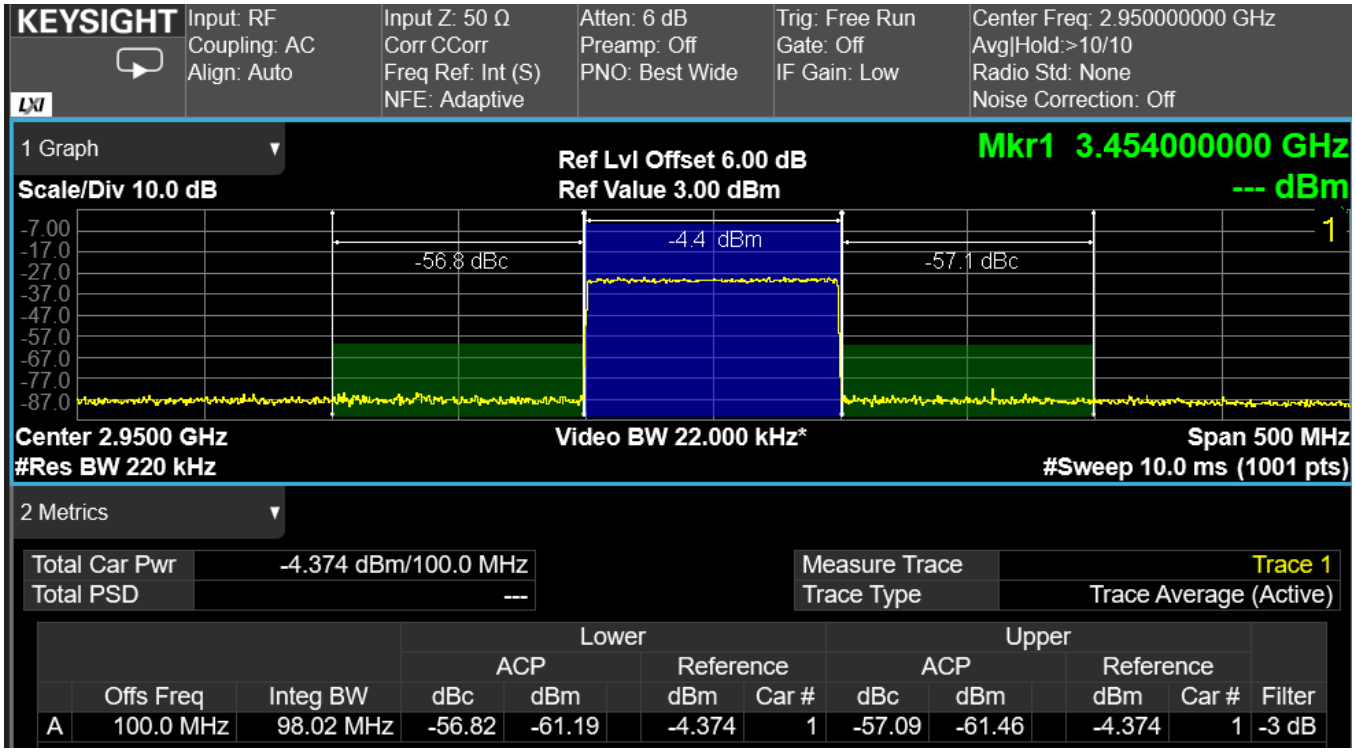
The EVM test of 5GNR100M@256QAM is as follows, 3.5 GHz frequency:

The EVM test of 400M@64QAM is as follows, 3.8 GHz frequency:

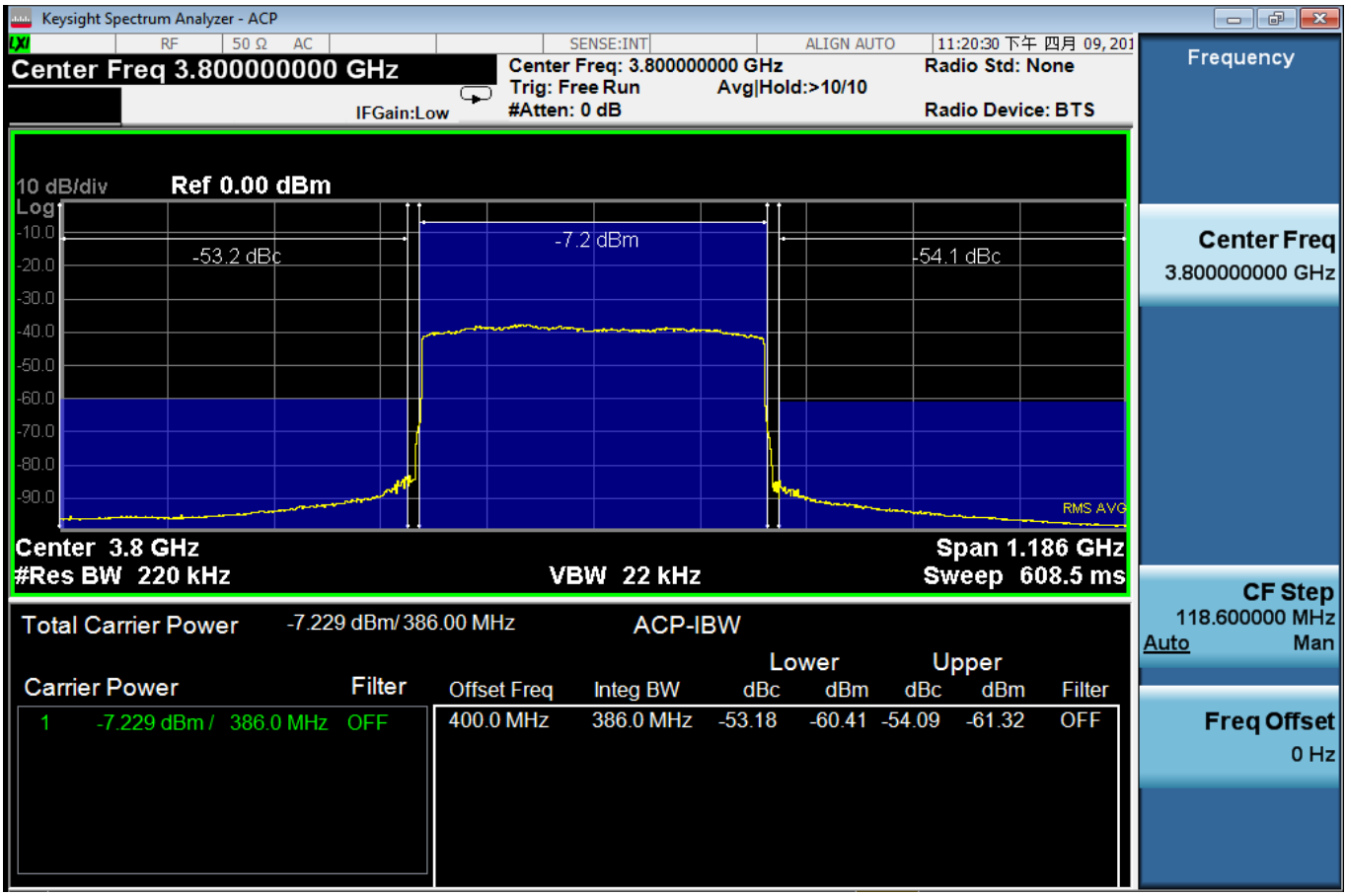


- **ACLR**

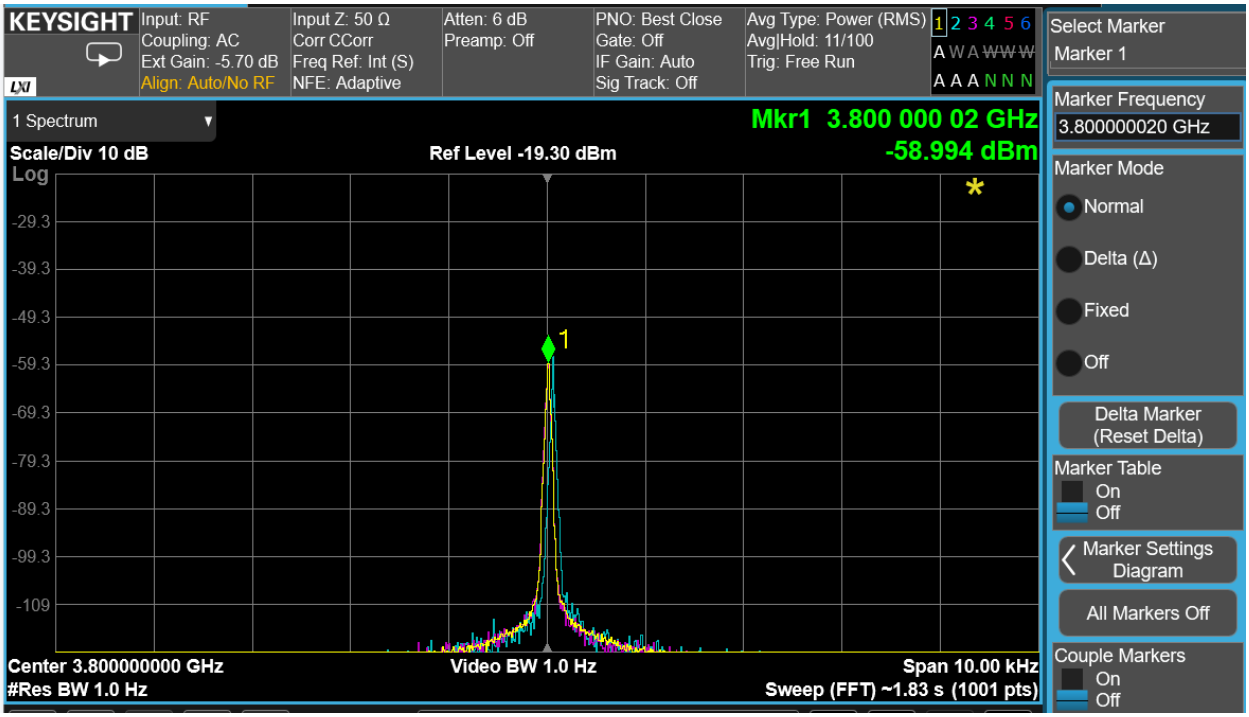
The ACLR@-12dBFs test of 5GNR100M@256QAM is as follows, 2.95 GHz frequency:



The ACLR@-12dBFs test of NR400M is as follows, 3.8 GHz frequency:

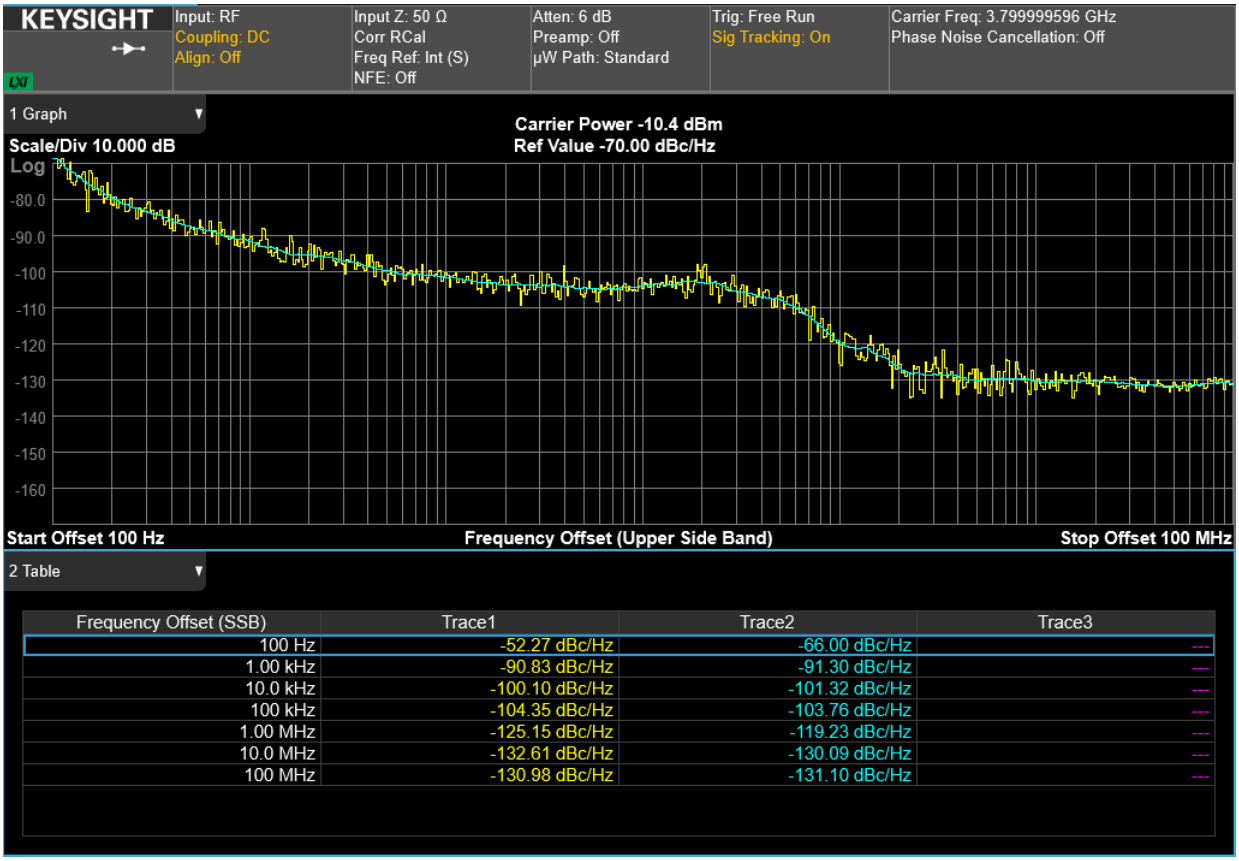


- **LO frequency difference**

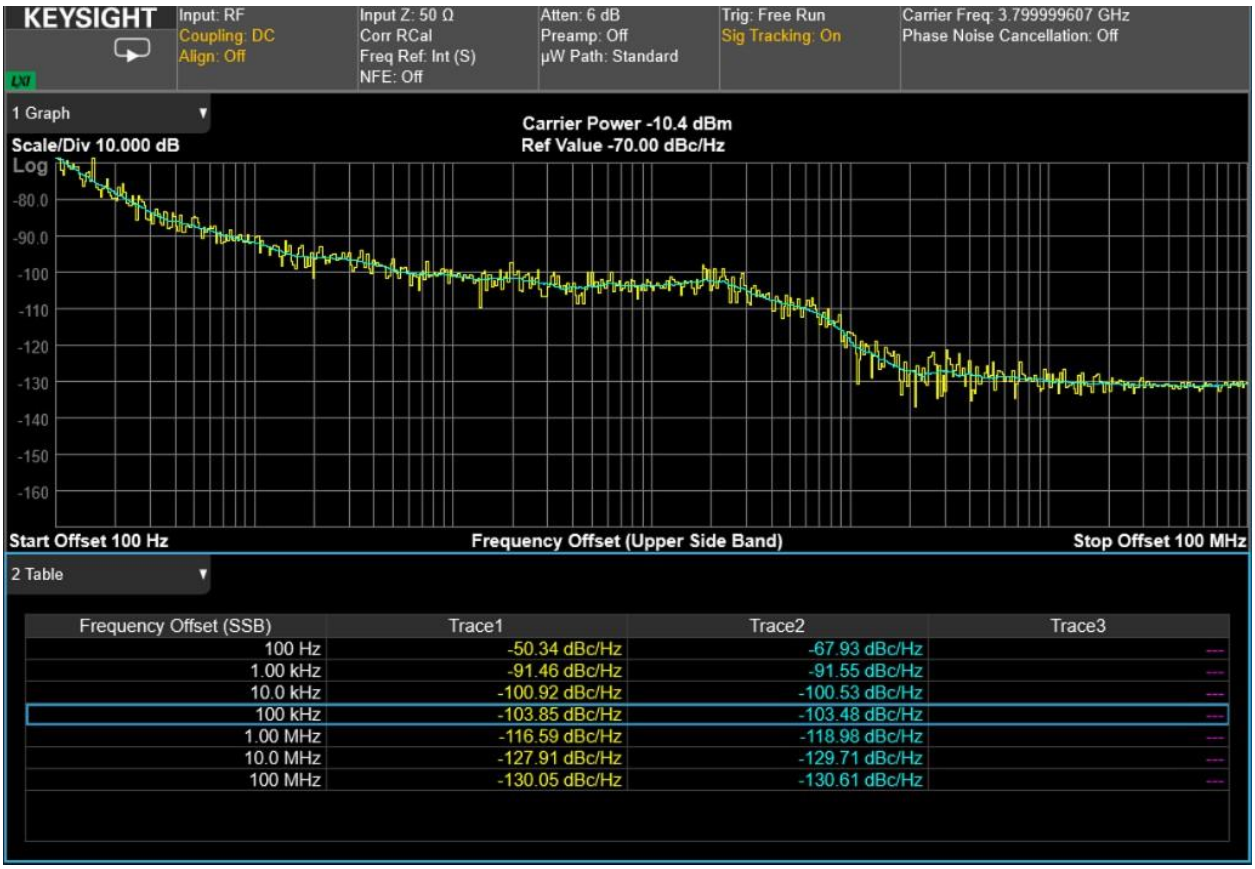


- **RFPLL and AuxPLL phase noise**

RFPLL operates at a frequency of 3.8 GHz, and the phase noise information is as follows:



AuxPLL operates at a frequency of 3.8 GHz, and the phase noise information is as follows:

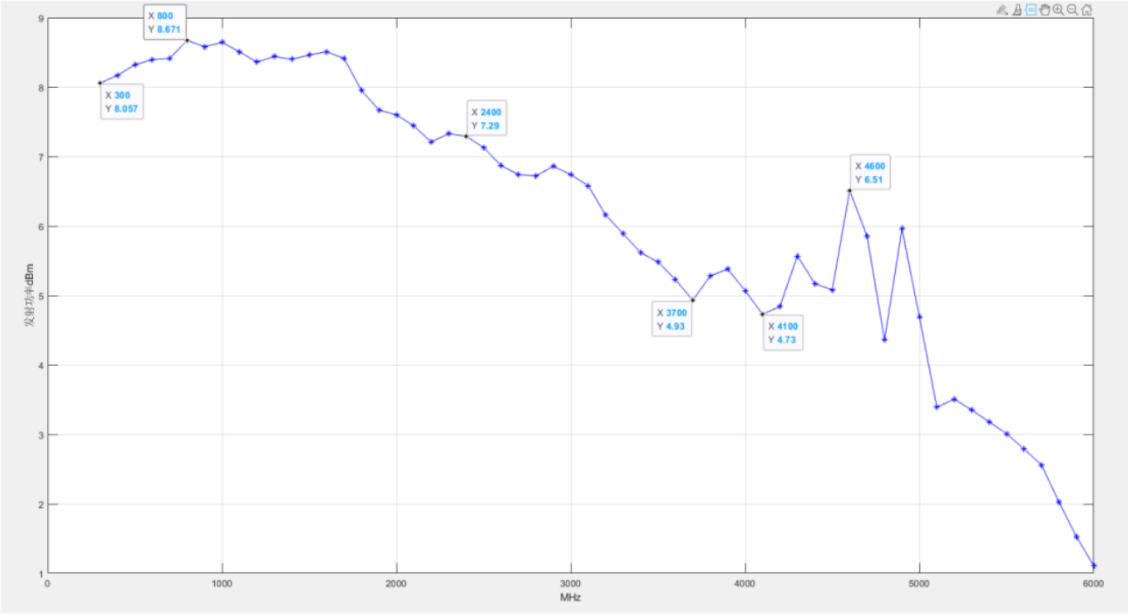


- **Transmit power test**

Test environment, spectrum analyzer keysight9020B, spectrum analyzer test RBW set to 100KHz, SPAN = 500M. Balun model is transmit broadband balun: TCM-83+.

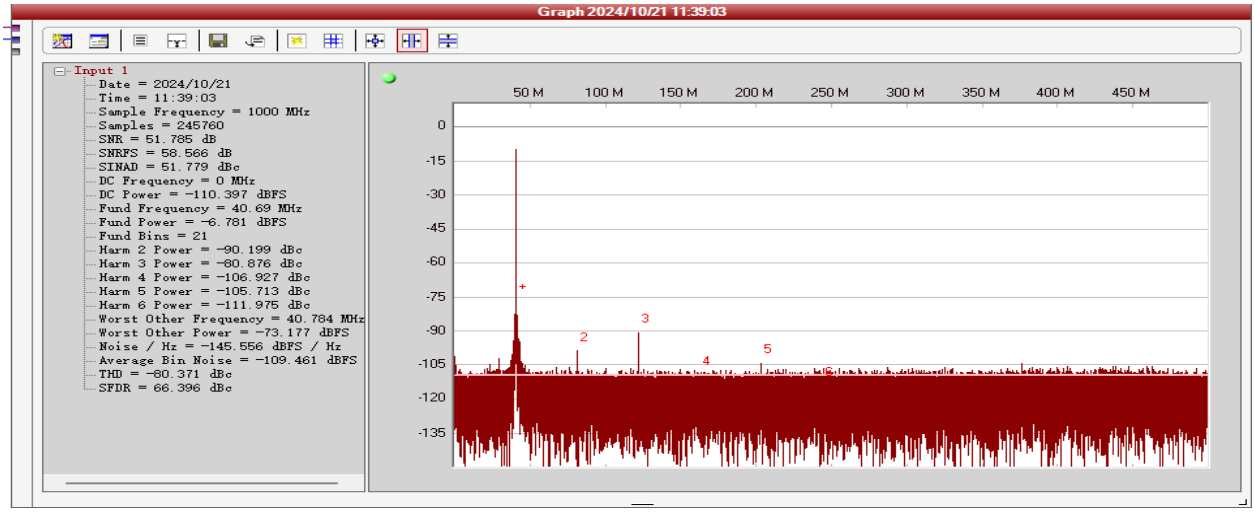
The signal source sends -10dBm single tone to the spectrum analyzer to test line loss.

Based on the above settings, the maker point test is conducted from 300M to 6G, and the transmission line loss compensation is tested every 250M interval. Every 100M interval, TX-ATT = 0dB, DDS full-scale single tone transmission test:



- **Typical receiving performance display**

Input -15dBm signal, frequency 3 GHz, after calibration:



Typical applications

Specification	Instructions for use
2Tx2Rx	1) 2Tx and 2Rx work at the same frequency; 2) 2Tx and 2Rx work at different frequencies;
2Tx2Rx+1ORx	TDD+DPD Typical Application
1TxRx+1TxRx	Each pair of TxRx has a different operating frequency
2Tx1ORx	1) 2Tx and 1ORx work at the same frequency; 2) 2Tx and 1ORx work at the same time at different frequencies; 3) The above bandwidth supports a maximum of 450M/200M transceiver @122.88 MHz; the minimum can be converted down based on the reference clock 122.88 MHz, such as 76M external reference, the bandwidth is about 126 MHz bandwidth;
1Tx1ORx	1) 1Tx and 1ORx work at the same frequency; 2) 1Tx and 1ORx work at the same time at different frequencies; 3) The above bandwidth supports a maximum of 450M/200M transceiver @122.88 MHz; the minimum can be converted down based on the reference clock 122.88 MHz, such as 76M external reference, the bandwidth is about 126 MHz bandwidth;
1Tx1Rx	1) 1Tx and 1Rx work at the same frequency; 2) 1Tx and 1Rx work at different frequencies;
1Tx	The bandwidth is typically 450M/200M/100M@122.88 MHz, and can also be converted down based on the reference clock 122.88 MHz, such as 76M external reference, and the bandwidth is approximately 64 MHz;
1Rx	Bandwidth: typical 200M/100M/100M@122.88 MHz;
1ORx	Bandwidth supports up to 450M/200M transceiver @122.88 MHz;

The chip supports the above specifications until February 1, 2025. On February 1, 2025, products with lower power consumption and other specifications other than those compatible with the above specifications will be launched to meet the requirements of multiple receiving channels, larger bandwidth multiple receiving channels, complex intermediate frequency reception, etc. Please stay tuned.