Tegsemi

TGS8435

32-channel discrete sensor

Data sheet

1. Product introduction

TGS8435 is a 32-channel discrete sensor with SPI interface, which can realize 32-channel discrete quantity to TTL level conversion, and supports functions such as mode selection, threshold configuration and data reading. It has four groups of 8 programmable discrete inputs, and the input mode can be selected between GND/Open or Supply/Open.

All discrete inputs are lightning protected and meet the requirements of AZ, BZ and ZZ standards in DO-160G Chapter 22 without adding external components.

Each discrete group has a VWETn pin that can apply a voltage higher than the logic supply to provide wetting current to the ground-side relay contacts. If the ground bias is small, there is no need to connect VWETn, and the wetting current is automatically provided from VLOGIC.

The interface to the digital subsystem uses CMOS logic inputs and outputs. The logic pins are 3.3 V compatible and can be connected directly to a variety of microcontrollers or FPGAs.

2. Main product features

- 4x8, 32 independent programmable discrete channels, GND/Open, Supply/Open configurable
- Programmable high/low threshold and hysteresis functions in 0.5 V steps from 2 V to 22 V
- Single voltage supply
- Output voltage noise: logic operating voltage range from 3.0 V to 3.6 V
- 20 MHz serial peripheral interface (SPI): supports high-speed data communication
- Built-in discrete input lightning protection, no external components required
- The lightning indirect effect protection capability of the discrete input port is DO-160G Chapter 22 Level Z
- Built-in self-test function
- Working range is -55℃ ~ 125℃

3. Application areas

- High reliability switch control
- Aviation
- Navigation parameters
- Electromechanical

4. Pin and Function Description

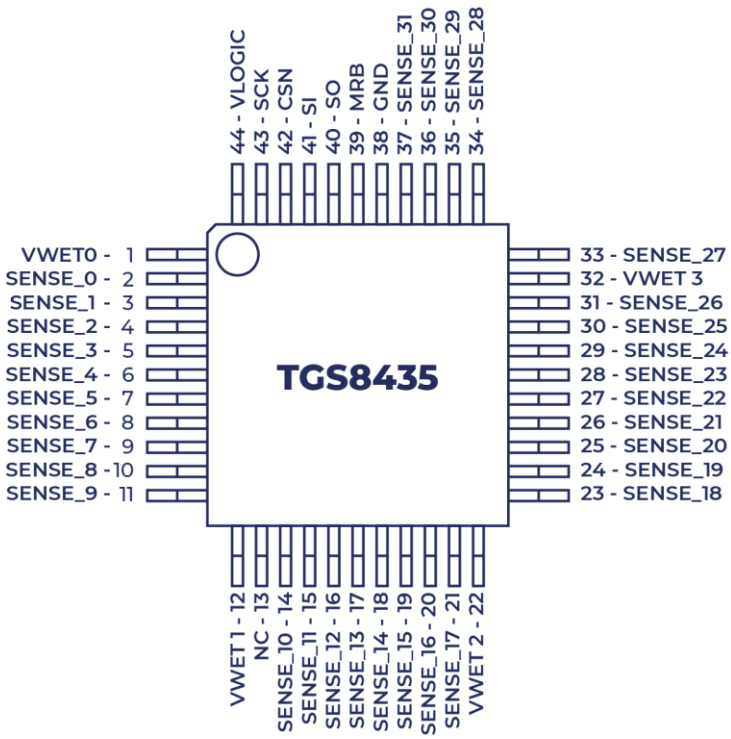


Figure 1. TGS8435 pin diagram

The chip terminal arrangement is specified in Table 2. The order of the terminals is as specified in Figure 1.

Table 2. Terminal symbols and function descriptions

Port number	Signal name	Type	Function
1	VWET0	Power supply	Optional input. In ground/on operating mode, it provides dry/wet current to the relay. Discrete input SENSE0 ~ SENSE7 group VWET0 port
2	SENSE0	Enter	Discrete input channel 0
3	SENSE1	Enter	Discrete input channel 1
4	SENSE2	Enter	Discrete input channel 2
5	SENSE3	Enter	Discrete input channel 3
6	SENSE4	Enter	Discrete input channel 4
7	SENSE5	Enter	Discrete input channel 5
8	SENSE6	Enter	Discrete input channel 6
9	SENSE7	Enter	Discrete input channel 7
10	SENSE8	Enter	Discrete input channel 8
11	SENSE9	Enter	Discrete input channel 9
12	VWET1	Power supply	Optional input. In ground/on operating mode, it provides dry/wet current to the relay. Discrete input SENSE8 ~ SENSE15 group VWET1 port
13	NC		-
14	SENSE10	Enter	Discrete input channel 10
15	SENSE11	Enter	Discrete input channel 11
16	SENSE12	Enter	Discrete input channel 12

17	SENSE13	Enter	Discrete input channel 13
18	SENSE14	Enter	Discrete input channel 14
19	SENSE15	Enter	Discrete input channel 15
20	SENSE16	Enter	Discrete input channel 16
21	SENSE17	Enter	Discrete input channel 17
22	VWET2	Power supply	Optional input. In ground/on operating mode, it provides dry/wet current to the relay. Discrete input SENSE16 ~ SENSE23 group VWET2 port
23	SENSE18	Enter	Discrete input channel 18
24	SENSE19	Enter	Discrete input channel 19
25	SENSE20	Enter	Discrete input channel 20
26	SENSE21	Enter	Discrete input channel 21
27	SENSE22	Enter	Discrete input channel 22
28	SENSE23	Enter	Discrete input channel 23
29	SENSE24	Enter	Discrete input channel 24
30	SENSE25	Enter	Discrete input channel 25
31	SENSE26	Enter	Discrete input channel 26
32	VWET3	Power supply	Optional input. In ground/on operating mode, it provides dry/wet current to the relay. Discrete input SENSE24 ~ SENSE32 group VWET3 port
33	SENSE27	Enter	Discrete input channel 27
34	SENSE28	Enter	Discrete input channel 28
35	SENSE29	Enter	Discrete input channel 29
36	SENSE30	Enter	Discrete input channel 30
37	SENSE31	Enter	Discrete input channel 31
38	GND	Land	Land
39	MRB	Output	Master reset, active low
40	SO	Output	SPI serial data output
41	SI	Enter	SPI serial data input
42	CSN	Enter	SPI chip select, active low level
43	SCK	Enter	SPI clock
44	VLOGIC	Power supply	Power supply (3.3 V)

5. Absolute Maximum Ratings

Supply voltage (VLOGIC): ~ +7 V

Supply voltage (VWETn): ~ +80 V

Discrete input port voltage (sense <0> ~ sense <31>): -80 V ~ +80 V

Storage temperature range: -65℃ ~ +150℃

Welding temperature (Th) (10s): 275℃

Junction temperature (Tj): 150℃

6. Recommended working conditions

Supply voltage (VLOGIC): V ~ 3.6 V

Supply voltage (VWETn): V ~ 36 V

Logic level input: V ~ 3.6 V

Discrete input port voltage (sense <0> ~ sense <31>): -4 V ~ +36 V

Work environment (T_A): -55℃ ~ +125℃

7. DC characteristics

Unless otherwise specified, the DC characteristics follow the provisions of Table 3. The test conditions are: T_A = -55℃ ~ +125℃, VLOGIC = 3.0 V and VLOGIC = 3.6 V.

Table 3. DC characteristics

Parameter	Symbol	Test conditions	Limit value		Unit
			Smallest	Maximum	
Logic input					
Input high level	V_{IH}	VLOGIC = 3.3 V	2.31	-	V
Input low level	V_{IL}	VLOGIC = 3.3 V	-	0.99	V
SI port input current	I_{SINK}	V_{IN} = VLOGIC, 30 kΩ pull-down resistor	-	125	uA
	I_{SOURCE}	V_{IN} = GND	-0.1	-	uA
MRB, CSN port Input current	I_{SINK}	V_{IN} = VLOGIC 30 kΩ pull-up resistor	-	0.1	uA
	I_{SOURCE}	V_{IN} = GND	-125	-	uA
Logic output					
Output high level	V_{OH}	I_{OUT} = -100 uA，VLOGIC = 3.3 V	2.97	-	V
Output low level	V_{OL}	I_{OUT} = 100 uA，VLOGIC = 3.3 V	-	0.33	V
Output high current	I_{OH}	V_{OUT} = VLOGIC - 0.4 V	1.6	-1	mA
Output low current	I_{OL}	V_{OUT} = 0.4 V	1.6	-	mA
Power supply					
VLOGIC port current	I_{DD}	All ports left open	-	16	mA
VWETn port current	I_{VWETn}	All input pins are 0 V, VWET = 28 V	-	35	mA
GND/OPEN mode					
Input port to VLOGIC impedance	R_{IN}	VLOGIC = 3.3 V	2.5	5	kΩ
Input port to VWET impedance	R_W	VLOGIC = 3.3 V	20	40	kΩ
Maximum high threshold	V_{THIMAX}	VTHI – VTLO ≥ 1 V	-	23.5	V
Minimum low threshold	V_{TLOMIN}	VTHI-VTLO ≥ 1 V	1.5	-	V
Input current	I_{IN0}	VIN = 0 V, VWET = OPEN	-1	-0.5	mA
GND/OPEN mode					
Input port impedance to ground	R_{IN}	VLOGIC = 3.3 V	25	45	kΩ
Maximum high threshold	V_{THIMAX}	V_{THI} - V_{TLO} ≥ 1 V		23.5	V
Minimum low threshold	V_{TLOMIN}	V_{THI} - V_{TLO} ≥ 1 V	1.5		V
Input current	I_{IN28}	V_{IN} = 28 V	0.6	1.2	mA

8. Timing specification characteristics

Unless otherwise specified, the timing specifications and characteristics follow the provisions of Table 4. The test conditions are: T_A = -55℃ ~ +125℃, VLOGIC = 3.0 V and VLOGIC = 3.6 V.

Table 4. Timing characteristics

Parameter	Symbol	Test conditions	Limit value		Unit
			Smallest	Maximum	
SCK clock cycle	Tcyc	-	50	-	ns
SCK rising edge to chip select valid time	t_{CHH}	-	5	-	ns
Chip select establishment to SCK rising edge time	t_{CES}	-	5	-	ns
SCK falling edge to chip select hold time	t_{CEH}	-	5	-	ns
Chip select time interval	t_{CPH}	-	55	-	ns
Setup time from SI input to SCK rising edge	t_{DS}	-	10	-	ns
SCK rising edge to SI data retention time	t_{DH}		10	-	ns
SCK rise time	t_{SCKR}	-	-	10	ns
SCK falling time	t_{SCKF}	-	-	10	ns
SCK high pulse width	t_{SCKH}	-	20	-	
SCK low pulse width	t_{SCKL}	-	20	-	
SCK falling edge to SO valid time	t_{DV}	-	-	20	ns
Chip select invalid to SO high impedance time	t_{CHZ}	-	-	20	ns
MRB pulse width	t_{MR}	-	100		ns
Sense response delay	-	-	-	1	μs
Threshold response delay	-	-	-	1	μs

9. SPI interface timing

The SPI interface access timing follows Figure 2 and Figure 3.

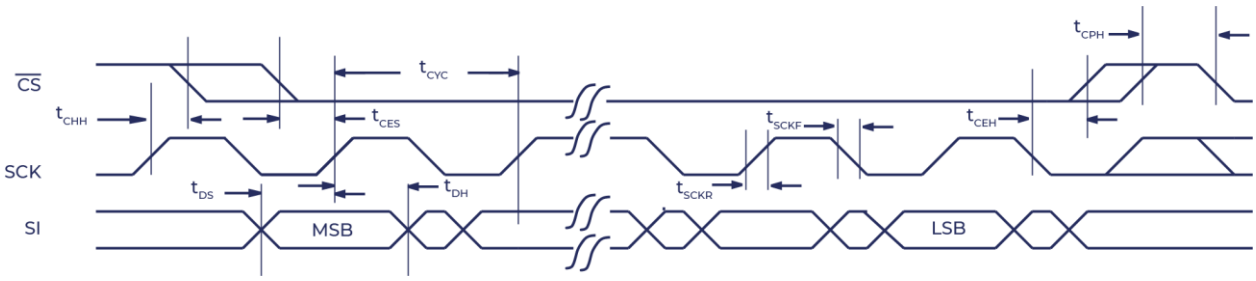


Figure 2. SPI interface timing diagram

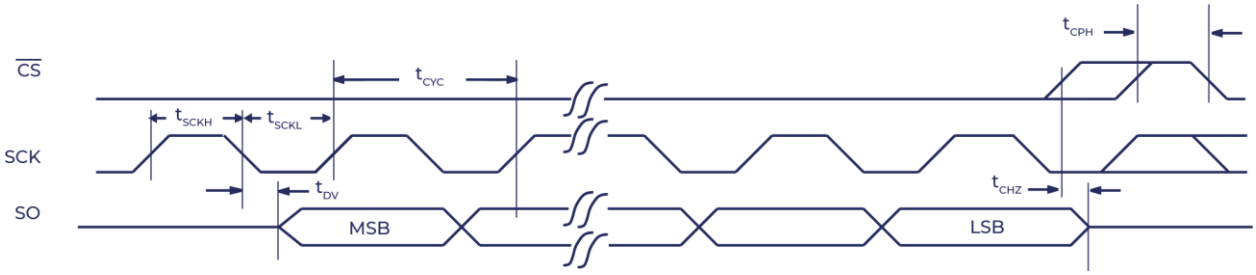


Figure 3. SPI interface timing diagram

10. Functional block diagram

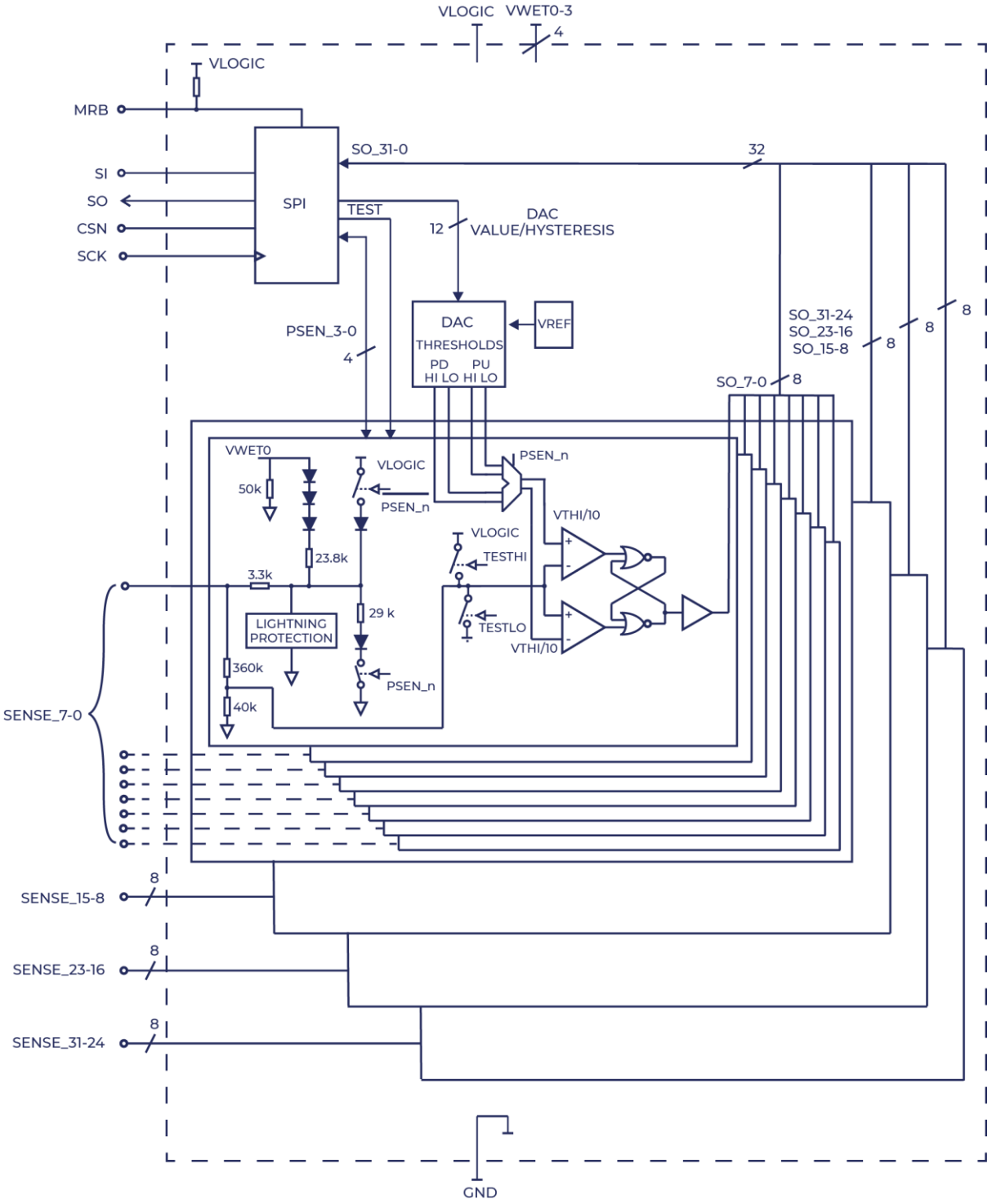


Figure 4. Chip functional block diagram

11. Function description

The TGS8435 discrete digital interface circuit provides 4 groups of 32 (4x8) discrete channels for conversion to TTL levels. The discrete processing mode of each group is SUPPLY/OPEN mode or GND/OPEN mode. The status of each group of discrete quantities can be configured through the SPI interface, or its status can be read.

Each group of discrete VWET pins can provide wetting current for the "GND" state of the discrete input port in GND/OPEN mode. By configuring the center threshold register and hysteresis register,

the chip can set the high/low threshold in GND/OPEN mode and the high/low threshold in SUPPLY/OPEN mode respectively. The threshold configuration range is 2 V to 22 V, and the step value is 0.5 V, see Table 5 and Table 6 for details.

The chip supports reading 1 or 4 sets of discrete conversion data at a time. Equipped with on-chip self-test function. The indirect lightning effect protection capability of the discrete input port reaches the AZ, BZ and ZZ levels in Chapter 22 "Lightning Induction Transient Sensitivity" of DO-160G, Waveform 3, Waveform 4, Waveform 5A and Waveform 5B (see below for details).

12.1 Initialization and reset

The chip can be reset in the following ways:

Built-in power-on reset. An internal power-on reset signal (POR) initializes all registers to default values.

MRB pin is reset. By applying a 100ns low-level pulse width signal to the MRB pin, a complete reset of the chip can be triggered.

SPI programming reset. By setting bit 1 of the control register (CTRL) to "1" through an SPI write operation, the chip can also be completely reset. The chip will not end the reset state until this bit is set to "0".

12.2 Configure working mode and threshold settings

Mode configuration

Users can complete chip configuration through the following steps:

1) Configure working modes for 4 groups of discrete inputs respectively;

2) Convert the desired VTHI and VTLO into center and hysteresis values as shown in the example below.

3) For GND/OPEN operating mode, VWETn must be set greater than VTHI/ 0.9 + 2.25 V.

Threshold settings

The chip has a built-in 6 bit DAC, and the VTHI and VTLO thresholds are set through the configuration register (GOCENHYS or SOCENHYS). DAC The step is 0.5 V / bit.

a) Select "VTHI" and "VTLO".

b) Hysteresis value = VTHI - VTLO.

c) Center value = (VTHI + VTLO) / 2 × 2 codes / V = VTHI + VTLO

d) Configure the registers.

Example:

a) GND/OPEN mode, VTHI = 10.5 V and VTLO = 4.5 V

b) Hysteresis value = VTHI – VTLO = 10.5 - 4.5 = 6 V = 0x06

c) Center value = VTHI + VTLO = 15 = 0x0F

d) Configure GOCENHYS register: 0x3A 0x06 0x0F

SENSE_n	PSEN_n	VWET_n	SO_n
Open circuit or $V_{SENSE\_n}>V_{THI}$	L(GND/OPEN)	**	L
$V_{SENSE\_n}<V_{TLO}$	L(GND/OPEN)	**	H
Open circuit or $V_{SENSE\_n}<V_{TLO}$	H(SUPPLY/OPEN)	OPEN	H
$V_{SENSE\_n}> V_{THI}$	H(SUPPLY/OPEN)	OPEN	L
Note: H = VLOGIC, L = GND, V_{THI} = ½ center value + ½ hysteresis value, V_{TLO} = ½ center value – ½ hysteresis value **For GND/OPEN mode, VWETn must be set greater than V_{THI} / 0.9 + 2.25 V			

Table 6. Configuration examples and allowed thresholds (-55°C to 125°C)

VLOGIC	VWET	PSENn	Operation mode	V_{THI}	V_{TLO}	High threshold maximum	Low threshold minimum
3.0 V - 3.6 V	7 V	L	GND/OPEN	4.0 V	2.0 V	V_{THI} + 0.5 V	V_{TLO} - 0.5 V
3.0 V - 3.6 V	28 V	L	GND/OPEN	22 V	2.0 V	V_{THI} + 1.25 V	V_{TLO} - 0.5 V
3.0 V - 3.6 V	OPEN	H	SUPPLY/OPEN	22 V	2.0 V	V_{THI} + 1.25 V	V_{TLO} - 0.5 V

NOTE: See Figure 5 Threshold Error Plot for the guaranteed error for set V_{THI} and V_{TLO}.

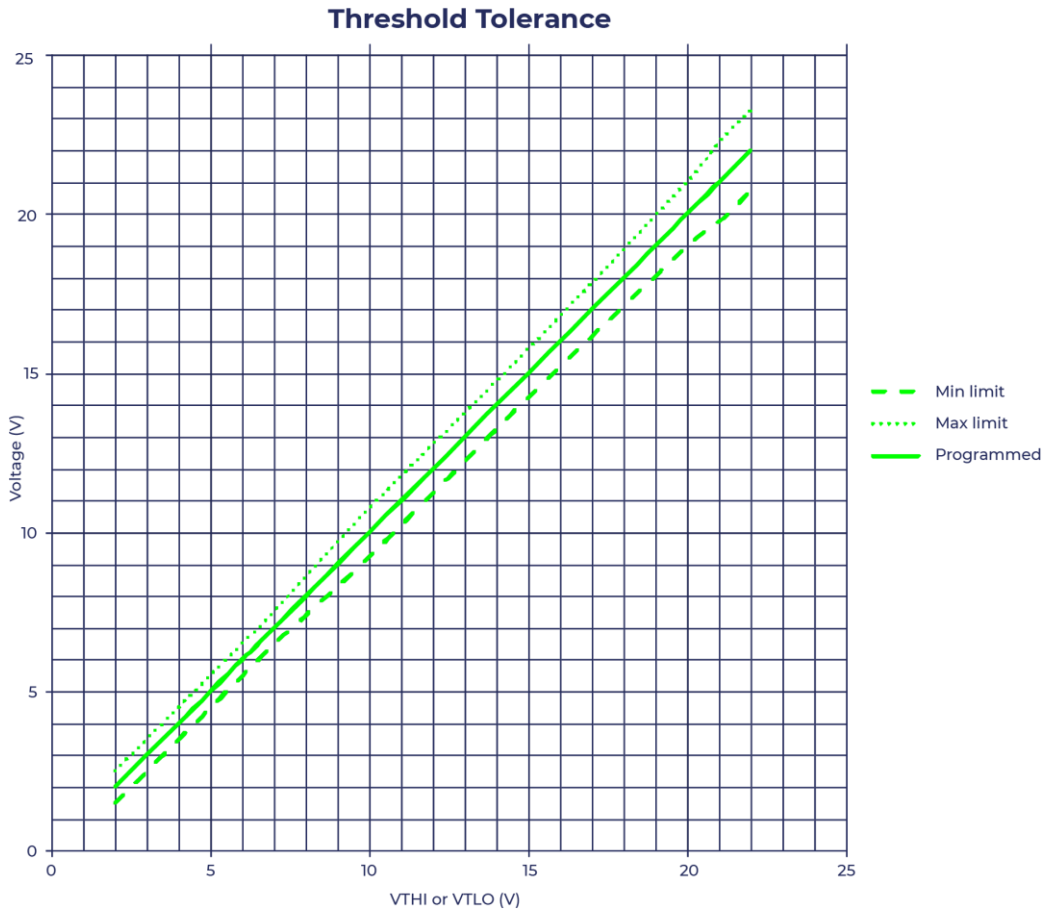


Figure 5. Threshold error graph

12.3 GND/OPEN mode

When the PSENn bit is set to 0, the configuration is in GND/OPEN mode. Referring to the chip architecture block diagram 4, the discrete input port is connected to the VLOGIC through a diode and a 3.3 kΩ pull-up resistor. This resistor can provide the wet current of the relay, and can also filter out noise when the port is in the OPEN state. The user sets the desired threshold voltage and then determines the open-circuit input voltage to set,VWETn. When SENSE_n is turned off, set the VWET voltage to be greater than (VTHI / 0.9 + 2.25 V). When the SENSE_n voltage is higher than the threshold voltage VTHI, the SO_n output is low.

12.4 SUPPLY/OPEN mode

When PSEN_n is set to 1, the group is configured in SUPPLY/OPEN mode. In addition to the 400 KΩ resistor connected to ground for the discrete input, a diode and 32 KΩ pull-down resistor are also connected in series at the switch. VWET_n must be disconnected when the user sets the desired threshold level. Threshold selection is handled in the same way as for the GND/OPEN case above.

12.5 Wetting current characteristics

The wetting current characteristics are shown in Figure 6.

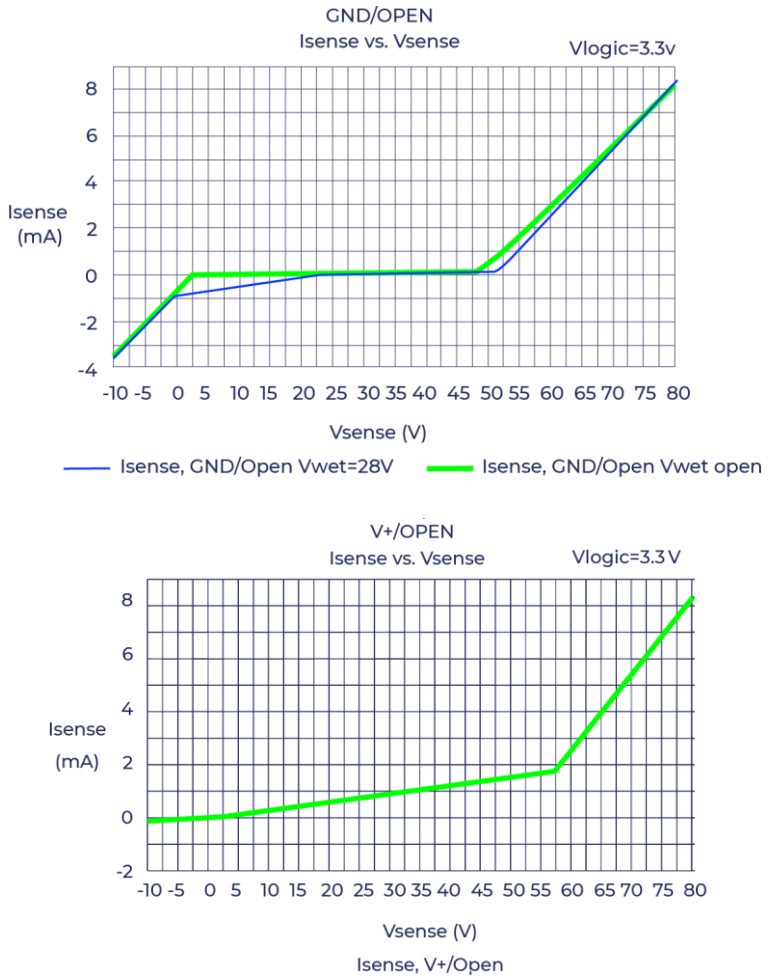


Figure 6. Input voltage and input current relationship diagram

12.6 Self-test mode

When the control register CTRL<0> is configured as "1", the chip enters self-test mode. In self-test mode, the input of each comparator is set to high level or low level, refer to Figure 5. Since a 360KΩ

resistor is connected in series between the self-test input signal and the discrete input pin, it will not interfere with the actual state of the input pin during self-test mode. By configuring the self-test mode register, four self-test modes can be selected, and the self-test results can be monitored by reading the data register through the SPI interface. Before entering self-test mode, the correct thresholds need to be configured to avoid errors.

12.7 SPI instructions

The SPI instructions supported by the chip are shown in Table 7.

Table 7. SPI command set

Opcode	Read/write	Number of bytes	Describe
0x02	W	1	Write control register
0x04	W	1	Write the discrete mode selection register PSE<3:0> to configure the discrete input mode
0x0A	W	2	Write GND/OPEN mode threshold center value and hysteresis value
0x0C	W	2	Write SUPPLY/OPEN mode threshold center value and hysteresis value
0x1E	W	1	Write self-test mode configuration register
0x82	R	1	Read control contactor
0x84	R	1	Read Discrete Mode Select Register
0xBA	R	2	Read GND/OPEN mode threshold center value and hysteresis value
0xBC	R	2	Read SUPPLY/OPEN mode threshold center value and hysteresis value
0x9E	R	1	Read self-test mode configuration register
0x90	R	1	Read Bank0, SOUT register, SO<7:0>, SENSE<7:0> input status
0x92	R	1	Read Bank1, SOUT register, SO<7:0>, SENSE<7:0> input status
0x94	R	1	Read Bank2, SOUT register, SO<7:0>, SENSE<7:0> input status
0x96	R	1	Read Bank3, SOUT register, SO<7:0>, SENSE<7:0> input status
0x98	R	4	Read the status of all Banks, SOUT registers, SO<31:0>, SENSE<31:0> inputs

12.8 SPI interface

The chip accesses internal registers through the SPI interface and programs to control/monitor the chip status. SPI instructions consist of opcodes and data bytes, as shown in Figure 5. The instructions start with the opcode and are 8 bits wide. When the most significant bit (MSB) is "0", it is a write operation, and when it is "1", it is a read operation. When CSN is low, the first eight rising edges of SCK sample the input SI opcode, and the MSB is the first sampled code.

The upward transition (rising edge) of CSN marks the completion of the serial transmission and SPI enters the next transmission preparation state. If CSN jumps to high level before clock SCK completes transmitting a complete byte, the incomplete byte input from SI is discarded. The chip operates in half-duplex mode. When actual serial data transmission is not performed, the SO output remains high impedance.

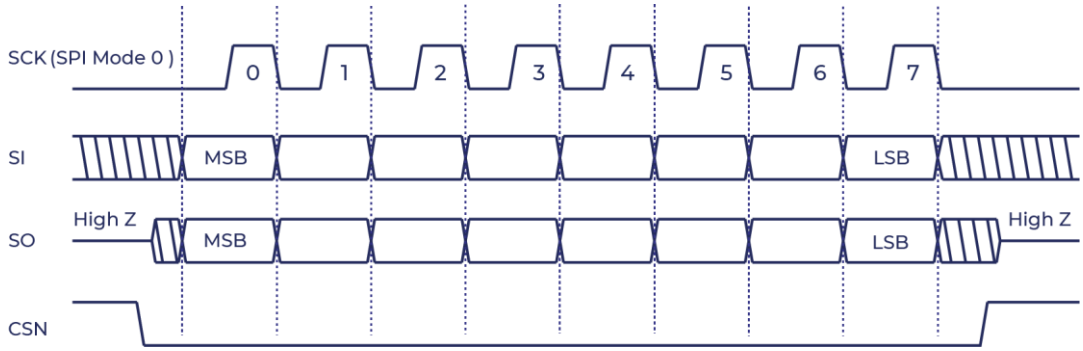


Figure 7. SPI opcode format

The write instruction samples SI data on the 8 rising edges of SCK after the instruction code and saves it to the data buffer. For multiple byte writes, this sequence is repeated until the write command is completed. After the read instruction ends in the SPI opcode, SO outputs the data value on the falling edge of the first SCK. As the falling edge of SCK changes, SO updates the data. For the read and write timing of single-byte, double-byte and four-byte register operations, as shown in Figure 8 to Figure 10, the instruction opcode is followed by the 8-bit data to be read or written. For register reads or writes, the CSN signal is pulled high after all data bytes have been transferred.

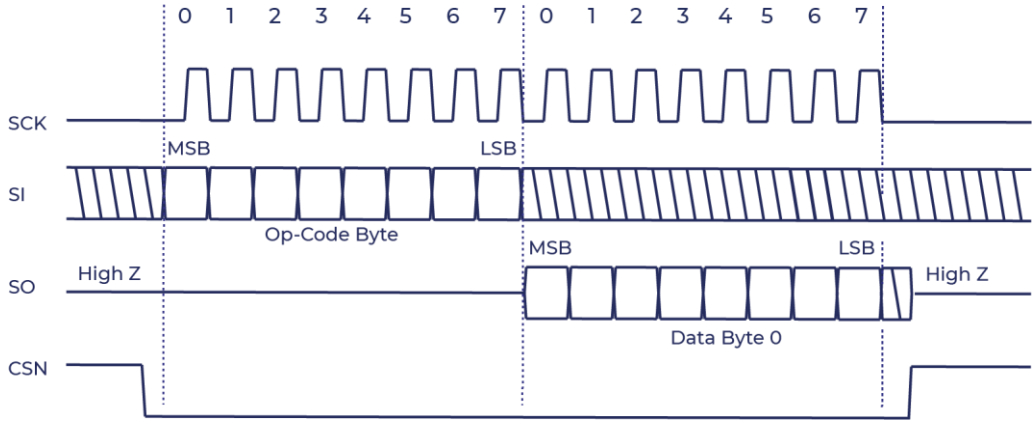


Figure 8. Single-byte register read operation example

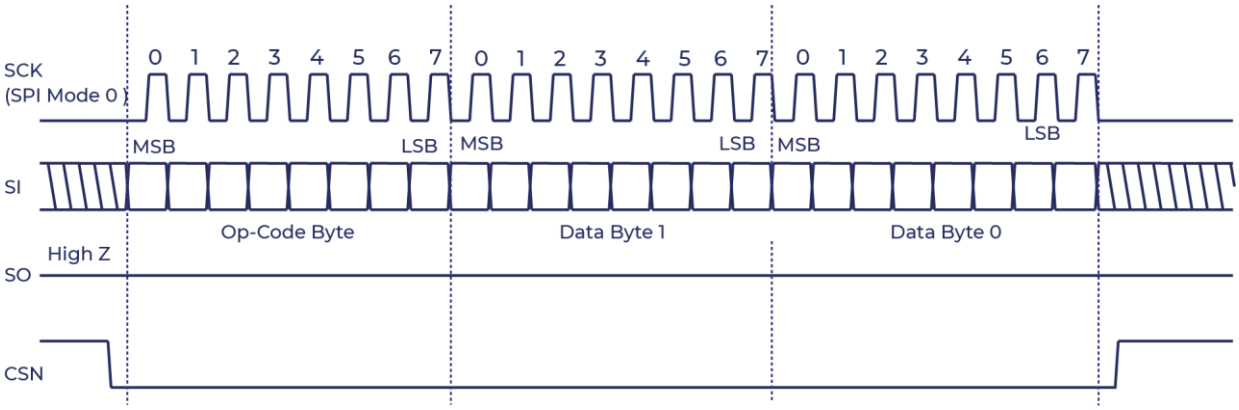


Figure 9. Example of double-byte register write operation

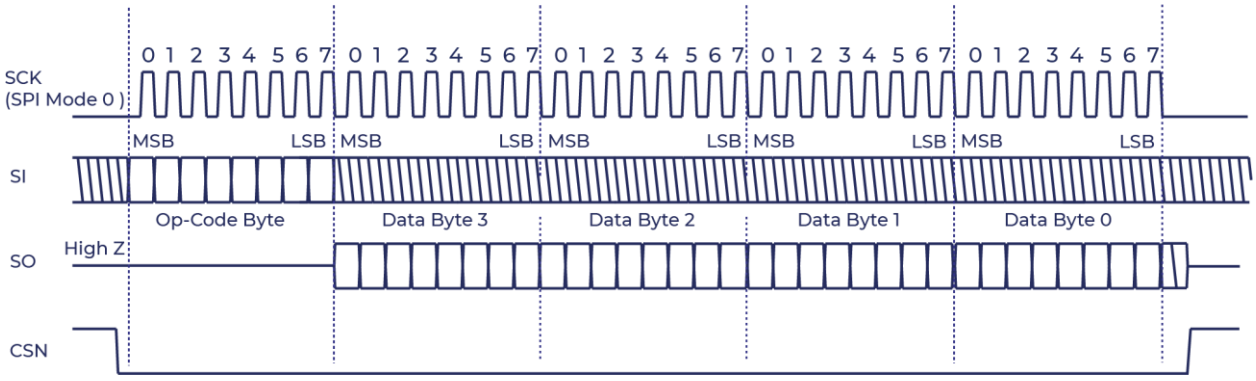


Figure 10. Example of four-byte register read operation

13. Register description

Control register: CTRL

Default value: 0x00

SPI read opcode: 0x82

SPI write opcode: 0x02

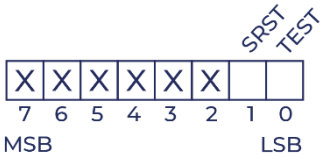


Table 8. Control register description

Bit field	Name	Read/write	Default value	Describe
7-2	-	R/W	0	Reserve
1	SRST	R/W	0	Soft reset. This bit is written to "1" and all other registers and the TEST bit of the control register are set to their default values. Write "0" to the SRST bit to exit the reset state.
0	TEST	R/W	0	Set this bit to "1" and the chip enters self-test mode. Sensor input configures register according to self-test mode The value determines the voltage comparator input.

Programmable Discrete Mode Register: PSEN<3:0>

Default value: 0x00

SPI read opcode: 0x84

SPI write opcode: 0x04

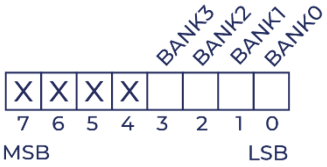


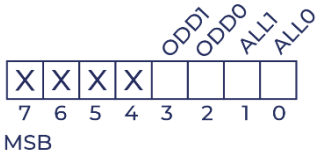
Table 9. Programmable discrete mode register description

Bit field	Name	Read/write	Default value	Describe
7-4	-	R/W	0	Reserve
3-0	BAN K3-0	R/W	0	BANK0 corresponds to SENSE<7:0> input BANK1 corresponds to SENSE<15:8> input BANK2 corresponds to SENSE<23:16> input BANK3 corresponds to SENSE<31:24> input When set to "0", this group of 8 inputs is configured as GND/OPEN mode. When set to "1", this group of 8 inputs is configured as SUPPLY/OPEN mode.

Self-test mode register: TMDATA

Default value: 0x00

SPI read opcode: 0x9E



SPI write opcode: 0x1E

Table 10. Self-test mode register description

Bit field	Name	Read/write	Default value	Describe
7-4	-	R/W	0	Reserve
3	ODD1	R/W	0	ODD1 is set to "1" and the odd input is set high.
2	ODD0	R/W	0	ODD0 is set to "1" and the odd input is set low.
1	ALL1	R/W	0	ALL1 is set to "1" and all inputs are set high.
0	ALL0	R/W	0	ALL0 is set to "1" and all inputs are set low.

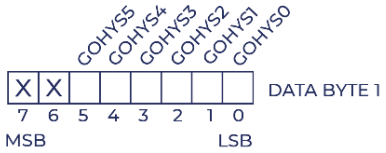
Note: Only one self-test mode can be selected to be valid. If multiple bits are set to "1", all inputs are set low.

GND/OPEN threshold center value and hysteresis value register: GOCENHYS

Default value: 0x00

SPI read opcode: 0xBA

SPI write opcode: 0x3A



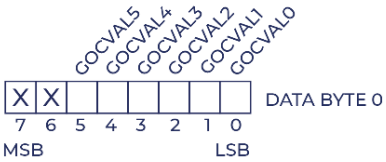


Table 11. GND/OPEN threshold center value and hysteresis value register description

Bit field	Name	Read/write	Default value	Describe
Data byte 1				
7-6	-	R/W	0	Reserve
5-0	GOHYS5- 0	R/W	0	GND/OPEN threshold hysteresis value. For all discrete inputs configured in GND/OPEN mode, the hysteresis value is set by these 6 bits. Hysteresis value = 1V * value of GOHYS<5:0>.
Data byte 0				
7-6	-	R/W	0	Reserve
5-0	GOCVAL 5-0	R/W	0	GND/OPEN threshold center value. For all discrete inputs configured in GND/OPEN mode, the threshold center value is set by these 6 bits. Threshold center value = 0.5V * value of GOCVAL<5:0>.

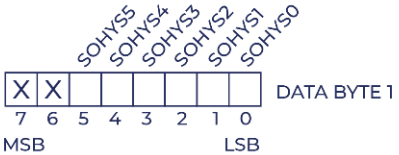
Note: The maximum value of VTHI is 22 V, and the minimum value of VTLO is 2 V. At the same time, VTHI - VTLO ≥ 1 V.

SUPPLY/OPEN threshold center value and hysteresis value register: SOCENHYS

Default value: 0x00

SPI read opcode: 0xBC

SPI write opcode: 0x3C



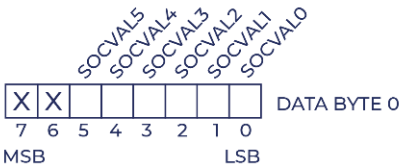


Table 12. SUPPLY/OPEN threshold center value and hysteresis value register description

Bit field	Name	Read/write	Default value	Describe
Data byte 1				
7-6	-	R/W	0	Reserve
5-0	SOHYS 5- 0	R/W	0	SUPPLY/OPEN threshold hysteresis value. For all discrete inputs configured in SUPPLY/OPEN mode, the hysteresis value is set by these 6 bits. Hysteresis value = 1V * value of SOHYS<5:0>.
Data byte 0				
7-6	-	R/W	0	Reserve
5-0	SOCV AL 5-0	R/W	0	GND/OPEN threshold center value. For all discrete inputs configured in SUPPLY/OPEN mode, the threshold center value is set by these 6 bits. Threshold center value = 0.5V * value of SOCVAL<5:0>.

Note: The maximum value of VTHI is 22 V, and the minimum value of VTLO is 2 V. At the same time, VTHI - VTLO ≥ 1V.

Output Status Register: SO<31:0>

The 32 registers can be accessed through the following 5 SPI commands.

For GND/OPEN input mode, if the discrete signal SENSE<n> is open circuit or >VTHI, then

SO<n> = "0".

If the discrete signal SENSE<n> level <VTLO, then SO<n> = "1".

For SUPPLY/OPEN input mode, if the discrete signal SENSE<n> is open circuit or <VTLO, then SO<n> = "1".

If the discrete signal SENSE<n> level>VTHI, then SO<n> = "0".

BANK0 output status register: SO<7:0>

Default value: 0x00

SPI read opcode: 0x90

SPI write opcode: None, read-only register

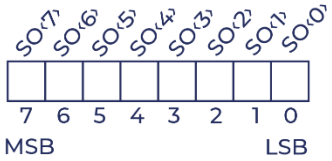


Table 13. BANK0 output status register description

Bit field	Name	Read/write	Default value	Describe
7-0	SO<7:0>	R	0	Discrete status output, SO<7:0> corresponds to SENSE<7:0> respectively.

BANK1 output status register: SO<15:8>

Default value: 0x00

SPI read opcode: 0x92

SPI write opcode: None, read-only register

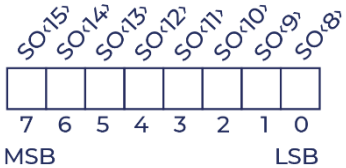


Table 14. BANK1 output status register description

Bit field	Name	Read/write	Default value	Describe
7-0	SO<15:8>	R	0	Discrete status output, SO<15:8> corresponds to SENSE<15:8> respectively.

BANK2 output status register: SO<23:16>

Default value: 0x00

SPI read opcode: 0x94

SPI write opcode: None, read-only register

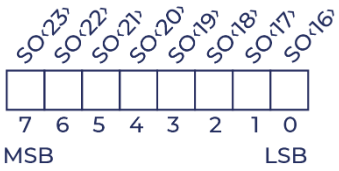


Table 15. BANK2 output status register description

Bit field	Name	Read/write	Default value	Describe
7-0	SO<23:16>	R	0	Discrete status output, SO<23:16> corresponds to SENSE<23:16> respectively.

BANK3 output status register: SO<31:24>

Default value: 0x00

SPI read opcode: 0x96

SPI write opcode: None, read-only register

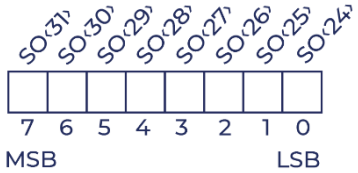


Table 16. BANK3 output status register description

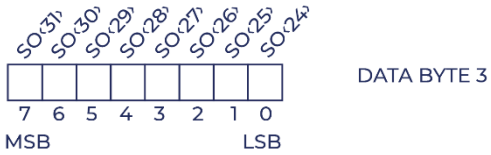
Bit field	Name	Read/write	Default value	Describe
7-0	SO<31:24>	R	0	Discrete status output, SO<31:24> corresponds to SENSE<31:24> respectively.

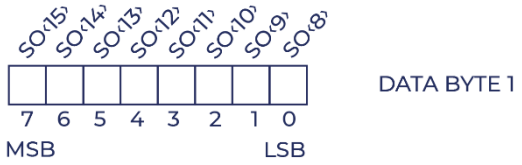
All output status registers: SO<31:0>

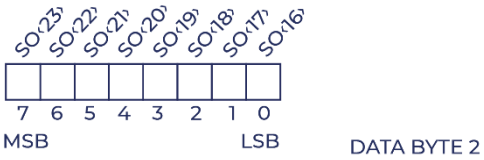
Default value: 0x00

SPI read opcode: 0xF8

SPI write opcode: None, read-only register







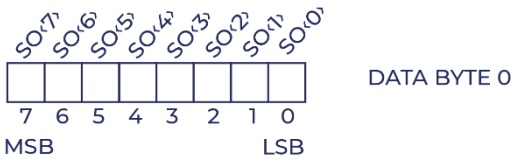


Table 17. Description of all output status registers

Bit field	Name	Read/write	Default value	Describe
31-0	SO<31:0>	R	0	Discrete status output, SO<31:0> corresponds to SENSE<31:0> respectively.

14. Lightning protection characteristics

The chip has a built-in lightning protection circuit in the discrete input port (SENSE0-SENSE31). When used, no external components are needed, and its lightning indirect effect protection capability can meet the AZ and BZ protection requirements specified in Chapter 22 of RTCA/DO-160G; In addition, in order to improve the robustness in composite aircraft structure applications, all inputs also meet the protection requirements of ZZ (waveform 3/3, 5B/5B). See Table 18 and Figure 11 for specific parameters and waveforms.

Table 18. Lightning protection characteristics

Level	WF (waveform)			
	3/3	4/1	5A/5A	5B/5B
	Voc(V)/Isc(A)	Voc(V)/Isc(A)	Voc(V)/Isc(A)	Voc(V)/Isc(A)
2	250/10	125/25	125/125	125/125
Z	500/20	300/60	300/300	300/300
3	600/24	300/60	300/300	300/300

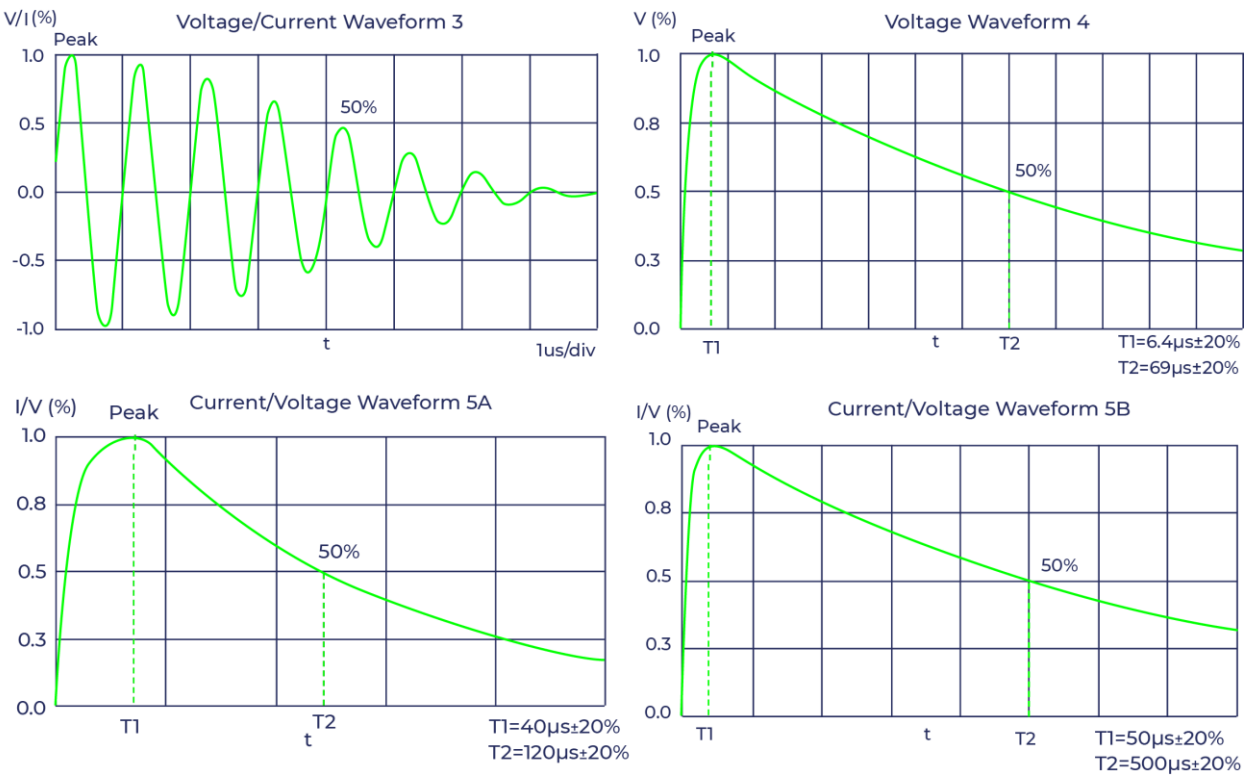


Figure 11. Lightning protection waveform

15. Level 3 lightning protection application plan

TGS8435 can achieve A3, B3 and Z3 protection requirements by connecting external resistors to discrete channels, as shown in Figure 12. R1 is external 0.25 W Anti-surge resistor, resistance value 470 Ω.

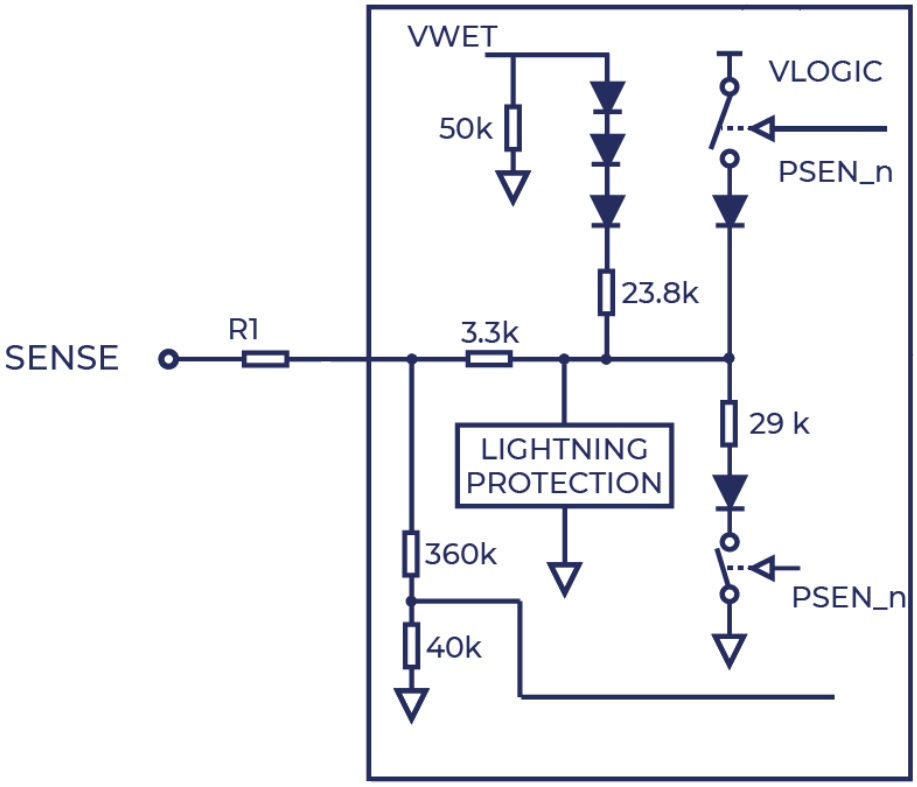


Figure 12. Assembly diagram of TGS8435 lightning protection (A3, B3 and Z3)

16. Cascade mode

TGS8435 supports cascading mode, and users can easily expand more channels through cascading. Figure 13 shows a processing solution that uses CSN signals to cascade three TGS8435s to expand to 96 discrete quantities.

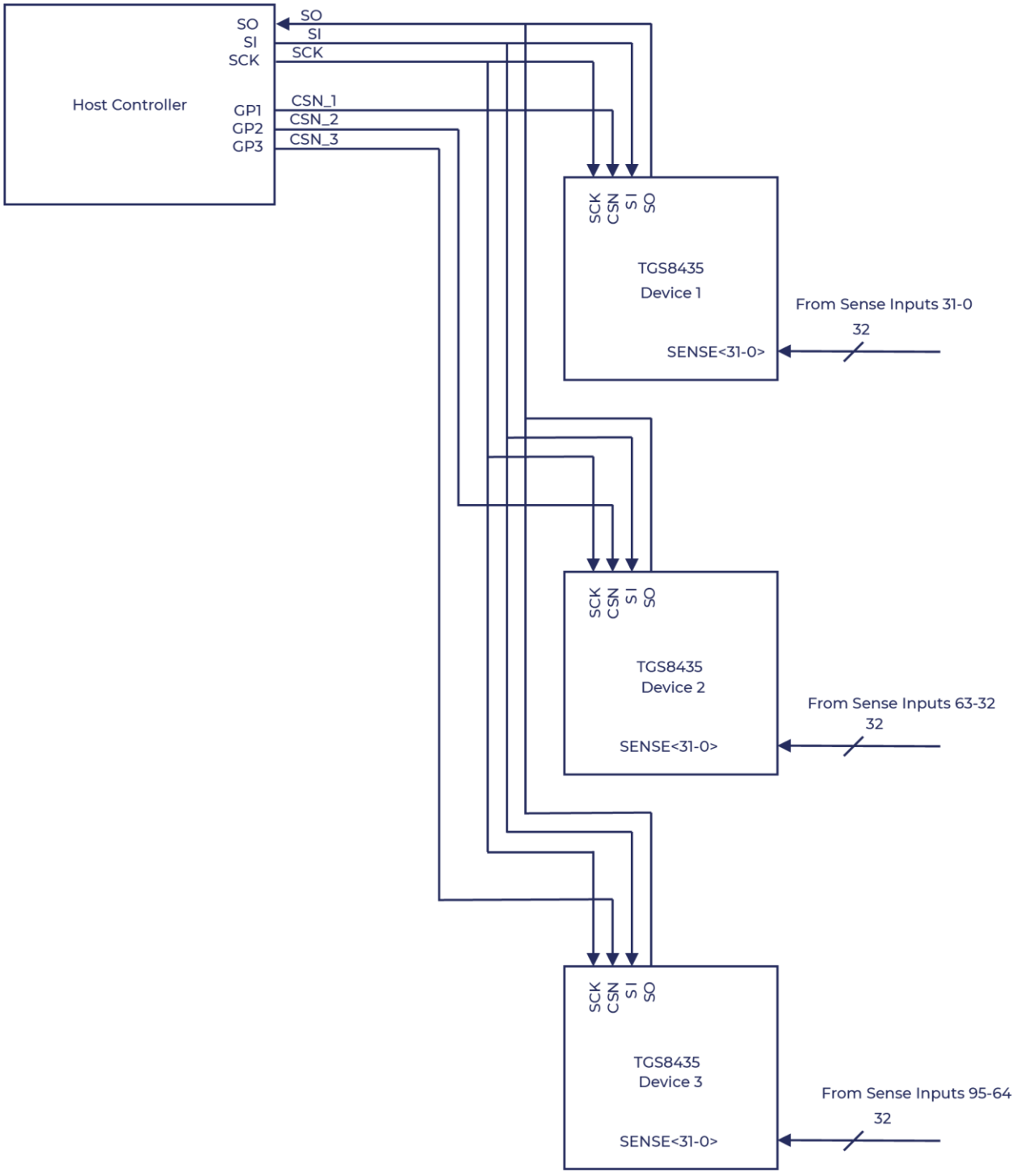


Figure 13. Schematic diagram of 96-channel discrete cascade expansion

17. Encapsulation

It is packaged in LQFP-44. The specific package dimensions are shown in Figure 14.

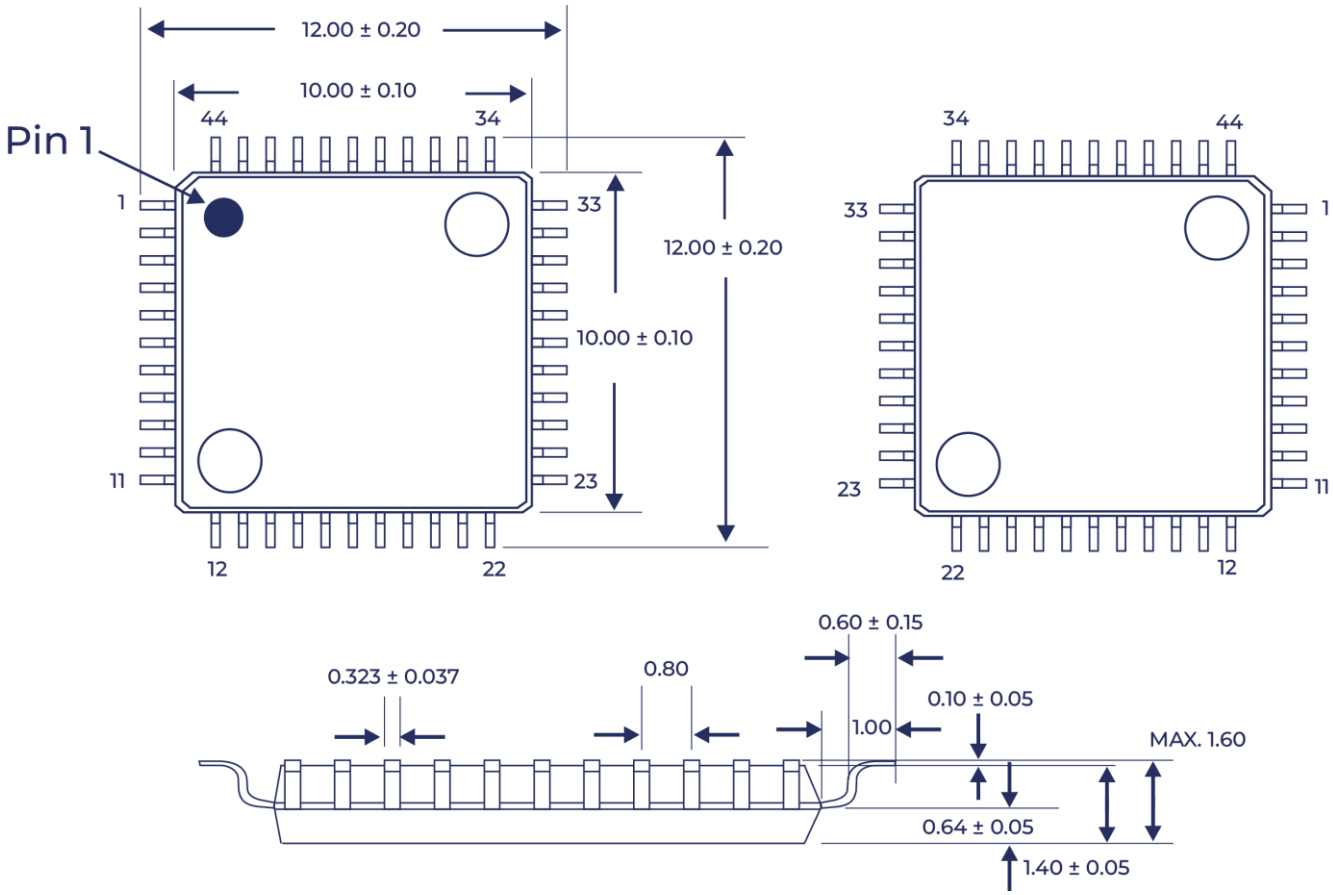


Figure 14. LQFP-44 package diagram

18. Ordering information

Model	Package
TGS8435-LQ	LQFP44