TGS32F103

Series MCU

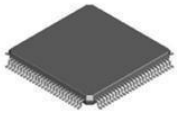
Data sheet

Function


QFN36 6 x 6 mm


LQFP48 7 x 7 mm


LQFP64 10 x 10 mm


LQFP100 14 x 14 mm

• Core: ARM32-bit Cortex™-M3 core

- Maximum operating frequency of 72MHz, up to 1.25DMips/MHz (Dhrystone2.1) when accessing the memory with 0 wait cycles
- Single cycle multiplication and hardware division

• **Memory**

- 64 KB or 128 KB program Flash
- 20 KB SRAM

• **Clock, reset and power management**

- 2.0 ~ 3.6 V power supply and I/O pins
- Power-on/power-off reset (POR/PDR), programmable voltage monitor (PVD)
- 4 ~ 16 MHz crystal oscillator
- Embedded factory-tuned 8 MHz high-speed RC oscillator
- Built-in 40 kHz low-speed RC oscillator
- PLL that generates the CPU clock
- 32 kHz RTC oscillator with calibration

• **Low power consumption**

- Sleep, shutdown and standby modes
- V_{BAT} powers the RTC and backup registers

• **12-bit ADCs, 1ps conversion time (up to 16 inputs channel)**

- Conversion range: 0 to 3.6 V
- Dual sampling and holding function
- Temperature sensor

• **DMA**：

- 7-channel DMA controller

- Supported peripherals: timers, ADC, SPI, I2C and USART

• **Up to 80 fast I/O ports**

- 26/37/51/80 I/O ports on the O side, all I/O ports can be mapped to 16 external interrupts; almost all ports can withstand 5 V signals.

• **Debug mode**

- Serial Single Wire Debug (SWD) and JTAG interface

• **7 timers**

- 3 16-bit timers, each with up to 4 channels for input capture/output compare/PWM or pulse counting and incremental encoder inputs

- 16-bit PWM advanced control timer with dead zone control and emergency brake for motor control

- 2 watchdog timers (independent and windowed)

- System time timer: 24-bit self-decreasing counter

• **Up to 9 communication interfaces**

- Up to 2 I2C interfaces (support SMBus/PMBus)

- Up to 3 USART interfaces (supports ISO7816 interface, LIN, IrDA interface and modem control)

- Up to 2 SPI interfaces (18Mbit/s)

- CAN interface (2.0B active)

- USB 2.0 full speed interface

• **CRC calculation unit, 96-bit unique chip identification code**

2. Description

The TGS32F103xB standard MCU series uses the high-performance ARM® Cortex™-M3 32-bit RISC core, operating at 72 MHz, built-in high-speed memory (up to 128K bytes of flash memory and 20K bytes of SRAM), and rich enhanced I/O ports and peripherals connected to both APB buses. It contains 2 12-bit ADCs, 3 general-purpose 16-bit timers and 1 PWM timer. In addition, it also contains standard and advanced communication interfaces: up to 2 I2C interfaces and SPI interfaces, 3 USART interfaces, 1 USB interface and 1 CAN interface.

The TGS32F103xB standard MCU series products have a power supply voltage of 2.0 V to 3.6 V, an operating temperature range of -45°C to +105°C, and a series of power-saving modes to meet the requirements of low-power applications.

The TGS32F103xB standard series products provide 4 different package forms from 36 to 100 pins; depending on the package form, the peripheral configurations in the device are different. A basic introduction to all peripherals in this family of products is given below.

These rich peripheral configurations enable the TGS32F103xB standard series microcontrollers to be used in a variety of applications:

• Motor drives and application control

• Medical and handheld devices

• PC gaming peripherals and GPS platforms

• Industrial applications: Programmable controllers (PLCs), frequency converters, printers and scanners

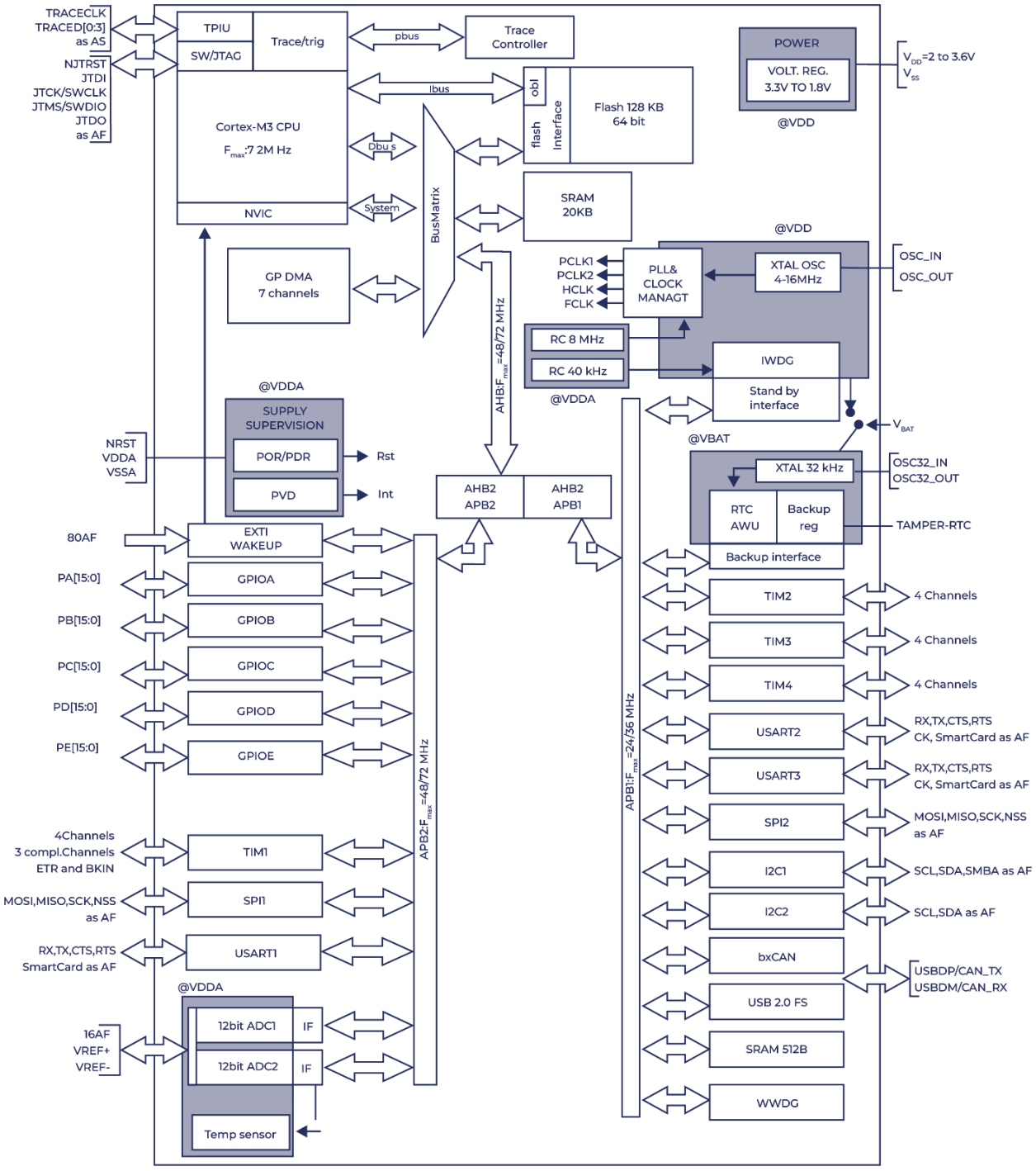
• Alarm systems, video intercoms and HVAC systems, etc.

2.1 Device comparison

TGS32F103xB product functions and peripheral configuration

Peripheral interface \ Product model		TGS32F103TB	TGS32F103CB	TGS32F103RB	TGS32F103VB
Flash Memory - K Bytes		128	128	128	128
SRAM - K Bytes		20	20	20	20
Timer	Universal	3	3	3	3
	Advanced control	1	1	1	1
Communication interface	**SPI**	1	2	2	2
	I2C	1	2	2	2
	USART	2	3	3	3
	USB	1	1	1	1
	CAN	1	1	1	1
GPIO port (number of channels)		26	37	51	80
12-bit synchronous ADC (number of channels)		2 10 channels	2 10 channels	2 16 channels	2 16 channels
CPU frequency		72 MHz			
Working voltage		2.0V ~3.6V			
Working temperature		Ambient temperature: -45°C ~ +105°C			
Encapsulation		QFN36	LQFP48	LQFP64	LQFP100

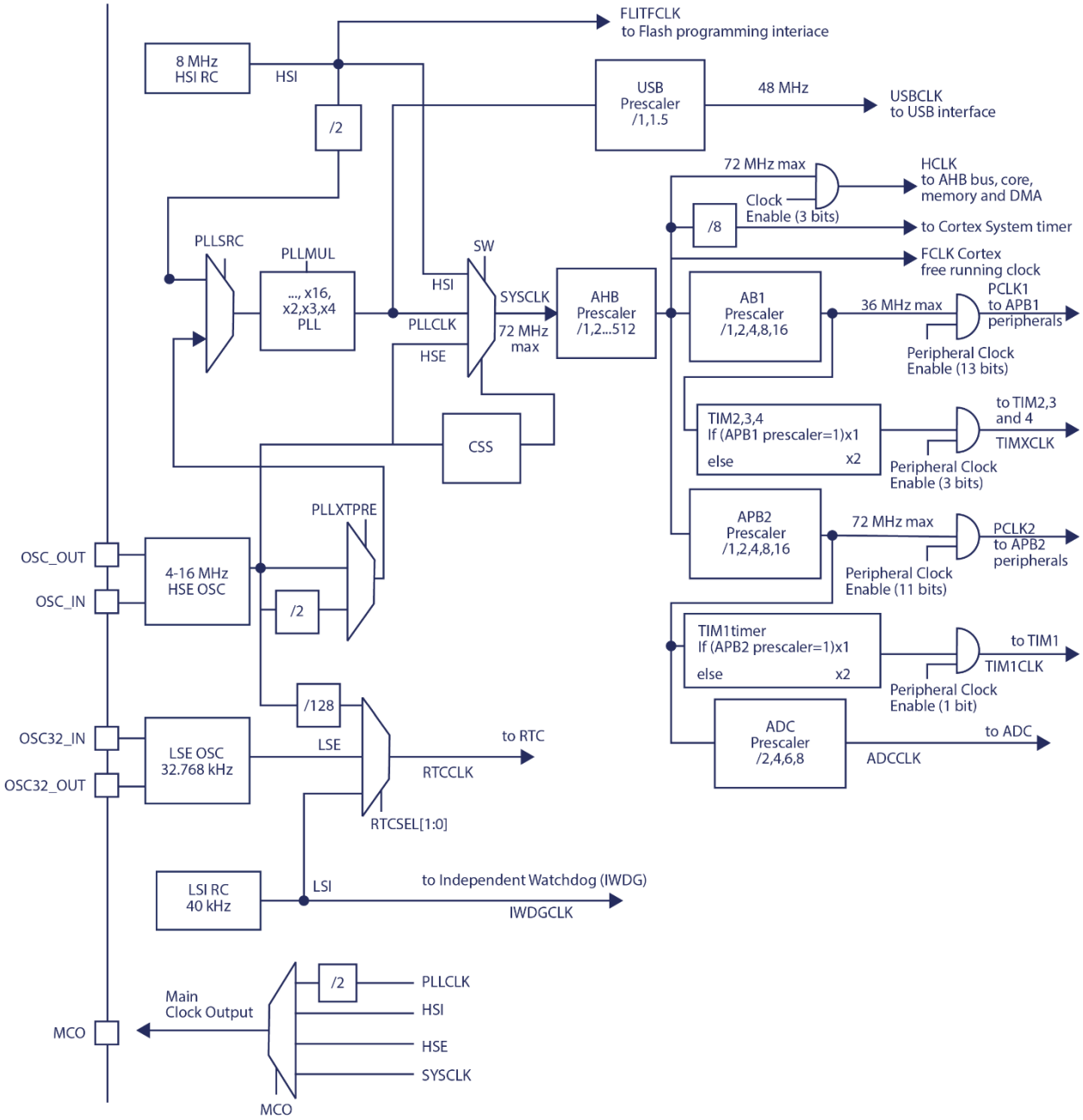
Figure 1. Functional block diagram



1. Operating temperature: -45°C to +105°C, junction temperature up to 150°C.

2. AF: I/O port that can be used as a peripheral function pin

Figure 2. Clock tree



Legend:

HSE = high-speed external clock signal
HSI = high-speed internal clock signal
LSI = low-speed internal clock signal
LSE = low-speed external clock signal

1. When HSI is used as the input of the PLL clock, the maximum system clock frequency can only reach 64MHz.

2. When using the USB function, HSE and PLL must be used at the same time, and the CPU frequency must be 48 MHz or 72 MHz.

3. When the ADC sampling time is required to be 1μs, APB2 must be set at 14 MHz, 28 MHz or 56 MHz.

2.2 Overview

2.2.1 ARM® Cortex™-M3 core with embedded flash memory and SRAM

ARM's Cortex™-M3 processor is the latest generation of embedded ARM processors. It provides a low-cost platform, reduced pin count and reduced system power consumption to implement MCU needs, while providing excellent computing performance and Advanced interrupt system response.

ARM's Cortex™-M3 is a 32-bit RISC processor that provides additional code efficiency, leveraging the high performance of ARM cores on the memory space typically found in 8- and 16-bit systems.

The TGS32F103xB standard series has a built-in ARM core, making it compatible with all ARM tools and software. Figure 1 is the functional block diagram of this series of products.

2.2.2 Built-in flash memory

128K bytes of built-in flash memory for program and data.

2.2.3 CRC (cyclic redundancy check) calculation unit

The CRC (Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In numerous applications, CRC-based techniques are used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting flash memory errors, a CRC calculation unit can be used to calculate the signature of the software in real time and compare it with the signature generated when the software is linked and generated.

2.2.4 Built-in SRAM

20K bytes of built-in SRAM, CPU can access (read/write) with 0 wait cycles.

2.2.5 Nested Vectored Interrupt Controller (NVIC)

The TGS32F103xB standard product has a built-in nested vectored interrupt controller that can handle up to 43 maskable interrupt channels.

(Excluding 16 Cortex™-M3 interrupt lines) and 16 priority levels.

• Tightly coupled NVIC enables low-latency interrupt response processing

• The interrupt vector entry address enters the kernel directly

• Tightly coupled NVIC interface

• Allow early handling of interrupts

• Handle late arriving higher priority interrupts

• Supports interrupt tail link function

• Automatically save processor state

• Automatic recovery on interrupt return without additional instruction overhead.

This module provides flexible interrupt management capabilities with minimal interrupt latency.

2.2.6 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 19 edge detectors for generating interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge or falling edge or both edges) and can be independently masked; a pending register maintains the status of all interrupt requests. EXTI can detect pulses whose width is less than the clock period of internal APB2. Up to 80 general-purpose I/O ports are connected to 16 external interrupt lines.

2.2.7 Clock and startup

The system clock is selected at startup. The internal 8 MHz RC oscillator is selected as the default CPU clock at reset. Subsequently, an external 4 ~ 16 MHz clock with failure monitoring can be selected; when the external clock failure is detected, it will Isolated, the system will automatically switch to the internal RC oscillator, and if interrupts are enabled, the software can receive corresponding interrupts. Likewise, complete interrupt management of the PLL clock can be implemented when required (e.g., when the external oscillator used during a period fails).

Multiple prescalers are used to configure the AHB frequency, high-speed APB (APB2) and low-speed APB (APB1) regions. AHB and high speed the maximum frequency of APB is 72 MHz and the maximum frequency of low speed APB is 36MHz. Refer to the clock driver block diagram shown in Figure 2.

2.2.8 Bootstrap mode

• At startup, one of three bootstrap modes can be selected via the bootstrap pin:

• Boot from program flash memory

• Boot from system memory

• Boot from internal SRAM

The bootloader is stored in the system memory and the flash memory can be reprogrammed through USART1.

2.2.9 Power supply solution

• V_{DD} = 2.0 ~ 3.6 V: The V_{DD} pin supplies power to the I/O pins and internal voltage regulator.

• V_{SSA}, V_{DDA}= 2.0 ~ 3.6 V: Provides power for the analog part of the ADC, reset module, RC oscillator and PLL. When using the ADC, V_{DDA} must not be less than 2.4 V. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.

• V_{BAT} = 1.8 ~ 3.6 V: When V_{DD} is turned off, power is supplied (via the internal power switch) to the RTC, external 32 kHz oscillator and backup registers.

See Figure 10 Power Supply Scheme for details on how to connect the power pins.

2.2.10 Power supply monitor

This product integrates a power-on reset (POR)/power-down reset (PDR) circuit. This circuit is always in working state to ensure that the system works when the power supply exceeds 2 V; when V_{DD} is lower than the set threshold ($V_{POR/PDR}$), the device is placed in the reset state without using an external reset circuit. There is also a programmable voltage monitor (PVD) in the device, which monitors the V_{DD} /V_{DDA} power supply and compares it with the threshold V_{PVD}. When V_{DD} is lower than or higher than the threshold V_{PVD}, an interrupt is generated. The interrupt handler can issue a warning message or set the microcontroller goes into safe mode. The PVD function needs to be enabled through a program. Refer to Table 8 for $V_{POR/PDR}$ and V_{PVD} values.

2.2.11 Voltage regulator

The voltage regulator has three operating modes: main mode (MR), low power mode (LPR) and shutdown mode

• Master mode (MR) for normal running operation

• Low power mode (LPR) for CPU shutdown mode

• Shutdown mode is used in the standby mode of the CPU: the output of the voltage regulator is in a high-impedance state, the power supply to the core circuit is cut off, and the voltage regulator is in a

zero-consumption state (but the contents of the register and SRAM will be lost)

The regulator is always active after reset and shuts down in standby mode with a high-impedance output.

2.2.12 Low power mode

The TGS32F103xB standard product supports three low-power modes to achieve the best balance between low power consumption, short startup time and multiple wake-up events.

Sleep mode

In sleep mode, only the MCU is stopped, all peripherals are active and can wake up the MCU when an interrupt/event occurs.

Shutdown mode

Stop mode can achieve the lowest power consumption without losing SRAM and register contents. In shutdown mode, the power supply to all internal 1.5 V parts is stopped, the PLL, HSI's RC oscillator and HSE crystal oscillator are turned off, and the voltage regulator can be placed in normal mode or low power mode.

The microcontroller can be woken up from Stop mode by any signal configured as EXTI. The EXTI signal can be 16 external one of the I/O ports, PVD output, RTC alarm clock or USB wake-up signal.

Standby mode

The lowest power consumption can be achieved in standby mode. The internal voltage regulator is turned off, so the power supply to all internal 1.5 V parts is cut off; the PLL, HSI RC oscillator and HSE crystal oscillator are also turned off; after entering standby mode, the contents of SRAM and registers will disappear, but the contents of the backup register are still retained and the standby circuit is still working.

The conditions for exiting from standby mode are: an external reset signal on NRST, an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm.

Note: When entering shutdown or standby mode, RTC, IWDG and their corresponding clocks will not be stopped.

2.2.13 DMA

Flexible 7-way general-purpose DMA manages memory-to-memory, device-to-memory, and memory-to-device data transfers;

The DMA controller supports ring buffer management, which avoids interrupts when the controller transfer reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software; the length of the transfer, the source address and destination address of the transfer can be set individually through software.

DMA can be used with the main peripherals: SPI, I2C, USART as well as general-purpose, high-level control timers TIMx and ADC.

2.2.14 RTC (real-time clock) and backup register

The RTC and backup registers are powered through a switch that selects VDD when VDD is valid, otherwise powered by the VBAT pin. The backup registers (10 16-bit registers) can be used to save 20 bytes of user application data when VDD is turned off. The RTC and backup registers are not reset by system or power reset sources, nor are they reset when waking from standby mode.

The real-time clock has a set of continuously running counters, can provide a calendar clock function

through appropriate software, and also has alarm interrupt and stage interrupt functions. The driving clock of the RTC can be a 32.768kHz oscillator using an external crystal, an internal low-power RC oscillator, or a high-speed external clock divided by 128. The internal low-power RC oscillator has a typical frequency of 40kHz. To compensate for natural crystal deviations, the RTC's clock can be calibrated by outputting a 512Hz signal. The RTC has a 32-bit programmable counter that allows long-term measurements using the compare register. There is a 20-bit prescaler for the time base clock which will produce a one second long time base by default when the clock is 32.768kHz.

2.2.15 Timers and watchdogs

The TGS32F103xB standard series includes 1 advanced control timer, 3 general-purpose timers, 2 watchdog timers and 1 system timer.

The following table compares the functionality of advanced control timers, normal timers, and basic timers:

Table 1. Timer function comparison

Timer	Counter resolution	Counter type	Prescaler coefficient	Generate DMA request	Capture/compare channels	Complementary output
TIM1	16 bit	Count up/down count	Any number between 1~65536 integer	Can	4	Have
TIM2 TIM3 TIM4	16 bit	Count up/count down	Any integer between 1~65536	Can	4	No

Advanced control timer (TIM1)

The Advanced Control Timer (TIM1) can be viewed as a three-phase PWM generator assigned to 6 channels, with complementary PWM outputs with dead-band insertion, or as a complete general-purpose timer. 4 independent channels can be used for:

• Input capture

• Output comparison

• Generate PWM (edge or center aligned mode)

• Single pulse output

When configured as a 16-bit standard timer, it has the same functionality as the TIMx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0~100%).

In debug mode, the counters can be frozen and the PWM outputs disabled, thereby turning off the switches controlled by these outputs. Many functions are the same as the standard TIM timer and the internal structure is the same, so the advanced control timer can operate in conjunction with the TIM timer through the timer link function to provide synchronization or event link functions.

General purpose timer (TIMx)

The TGS32F103xB standard product has built-in up to 3 standard timers (TIM2, TIM3 and TIM4) that can run synchronously. Each timer has a 16-bit auto-loading up/down counter, a 16-bit prescaler and 4 independent channels, each channel can be used for input capture, output compare, PWM and single pulse mode Outputs, providing up to 12 input capture, output compare, or PWM channels in the largest package configuration.

They can also work with advanced control timers via the timer linking feature, providing synchronization or event linking capabilities. In debug mode, the counter can be frozen. Any standard timer can be used to generate the PWM output. Each timer has an independent DMA

request mechanism.

These timers are also capable of processing the signals of incremental encoders, as well as the digital outputs of 1 to 3 Hall sensors.

Independent watchdog

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler, which is clocked by an internal independent 40 kHz RC oscillator; because this RC oscillator is independent of the main clock, it can run in shutdown mode and standby mode. It can be used as a watchdog to reset the entire system when a problem occurs, or as a free timer to provide timeout management for applications. The watchdog can be configured to be software or hardware enabled through the option byte. In debug mode, counters can be frozen.

Window watchdog

The window watchdog contains a 7-bit down counter that can be configured as a free-running counter. When used as a watchdog, the entire system can be reset if a problem occurs. It is driven by the main clock and has an early warning interrupt function; in debug mode, the counter can be frozen.

System time base timer

This timer can be used exclusively in real-time operating systems, or it can be used as a standard down counter. It has the following characteristics:

• 24-bit down counter

• Auto-reload feature

• Can generate a maskable system interrupt when the counter reaches 0

• Programmable clock source

2.2.16 I2C bus

Up to 2 I2C bus interfaces, capable of working in multi-master mode or slave mode, supporting standard mode and fast mode.

The I2C interface supports 7-bit or 10-bit addressing, and the 7-bit slave mode supports dual slave address addressing. Built-in hardware CRC generator/checker. The interface operates using DMA and supports the SMBus bus version 2.0/PMBus bus.

2.2.17 Universal Synchronous/Asynchronous Receiver-Transmitter (USART)

The communication rate of the USART1 interface can reach 4.5 Mb/s, and the communication rate of other interfaces can reach 2.25 Mb/s. The USART interface has hardware CTS and RTS signal management, supports IrDA SIR ENDEC transmission codec, is compatible with ISO7816 smart cards and provides LIN master/slave functionality. All USART interfaces can use DMA operations.

2.2.18 Serial Peripheral Interface (SPI)

Up to 2 SPI interfaces, configurable in slave or master mode, with communication rates up to 18 Mb/s in full and half duplex. The 3-bit prescaler generates 8 master mode frequencies, configurable into 8-bit or 16-bit data frame format. Hardware CRC generation/checking supports basic SD card and MMC modes.

All SPI interfaces can use DMA operations.

2.2.19 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active) with bit rates up to 1 Mb/s. It can receive and send standard frames with an 11-bit identifier, or extended frames with a 29-

bit identifier. Features 3 send mailboxes and 2 receive FIFOs, 3 levels of 14 adjustable filters.

2.2.20 Universal Serial Bus (USB)

The TGS32F103xB standard series products embed a device controller compatible with full-speed USB and comply with the full-speed USB device (12 Mb/s) standard, endpoints are software configurable with standby/wake capabilities. The USB-specific 48 MHz clock is generated directly by the internal main PLL (the clock source must be an HSE crystal oscillator).

2.2.21 General input and output interface (GPIO)

Each GPIO pin can be configured by software as an output (push-pull or open-drain), input (pull-up or pull-down or floating), or a multiplexed peripheral function port. Most GPIO pins are shared with multiplexed digital or analog peripherals. In addition to having analog input capabilities, all GPIO pins allow large currents to pass through them.

If desired, the peripheral function of an I/O pin can be locked by a specific operation to avoid accidental writes to the I/O registers. The I/O pins on APB2 can toggle up to 18 MHz.

2.2.22 ADC (analog/digital converter)

The TGS32F103xB standard product embeds two 12-bit analog/digital converters (ADCs). Each ADC shares up to 16 external channels and can achieve single conversion or scan mode conversion. In scan mode, conversions are automatically performed on a selected set of analog input pins.

Other logic functions on the ADC interface include:

• Synchronized sample and hold

• Interleaved sample and hold

• Single sampling

The ADC can operate using DMA.

The analog watchdog can monitor one, multiple or all selected channels very accurately. When the monitored signal exceeds the preset threshold, the analog watchdog will generate an interrupt.

Events generated by the standard timer (TIMx) and the advanced control timer (TIM1) can be internally cascaded to the start trigger and injection trigger of the ADC respectively, and the application can synchronize the AD conversion with the clock.

2.2.23 Temperature sensor

The temperature sensor generates a voltage that changes linearly with temperature, with a conversion range of 2 V < VDDA < 3.6 V. The temperature sensor is internally connected to the input channel of ADC1_IN16, which converts the sensor output to a digital value.

2.2.24 Serial single-wire JTAG debug port (SWJ-DP)

Embedded ARM's SWJ-DP interface, which is an interface that combines JTAG and serial single-wire debugging, can realize the connection of the serial single-wire debugging interface or the JTAG interface. The TMS and TCK signals of JTAG share pins with SWDIO and SWCLK respectively. A special signal sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3. Pin definition

Figure 3. TGS32F103xB LQFP100 pin distribution

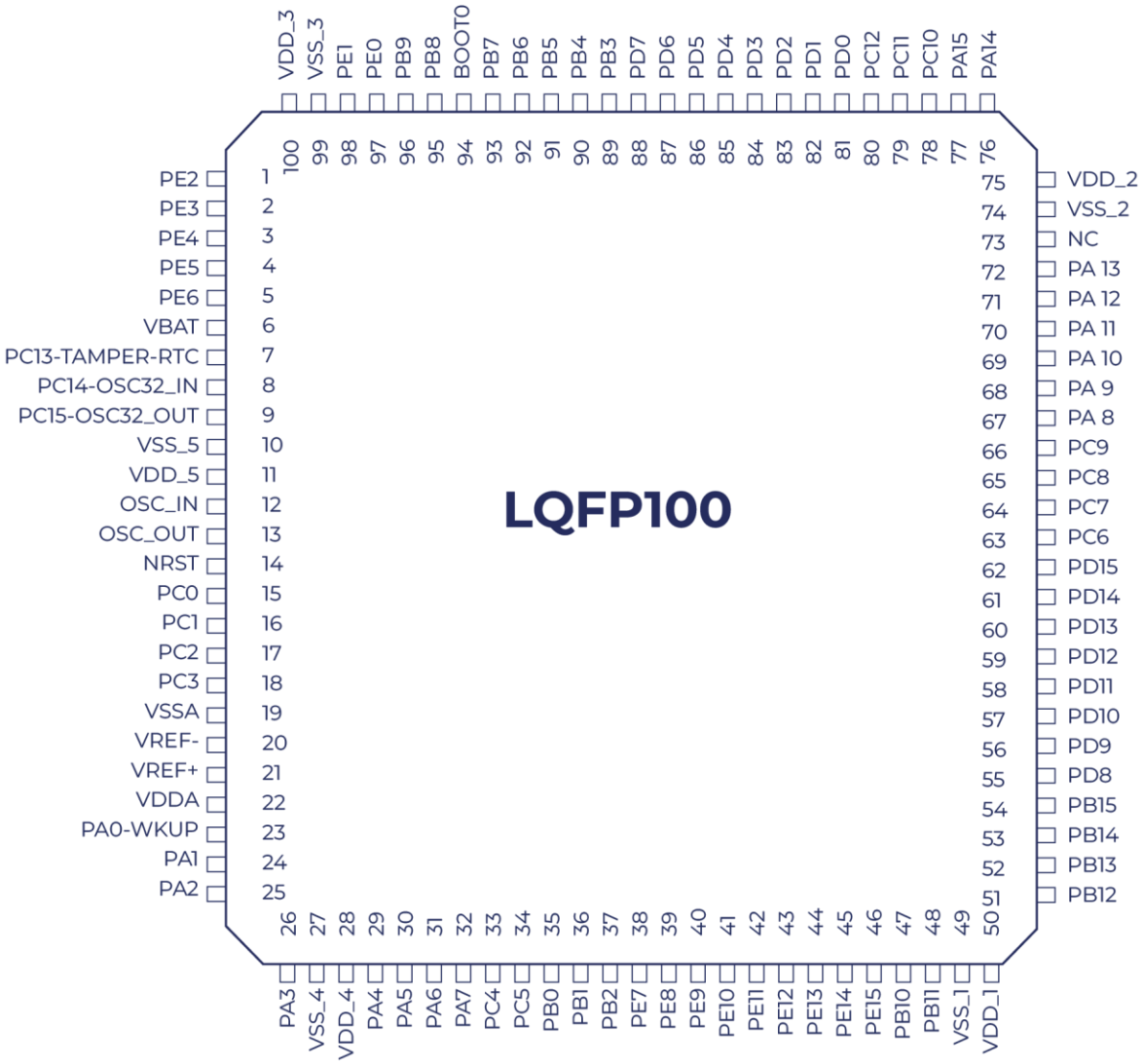


Figure 4. TGS32F103xB LQFP64 pin distribution

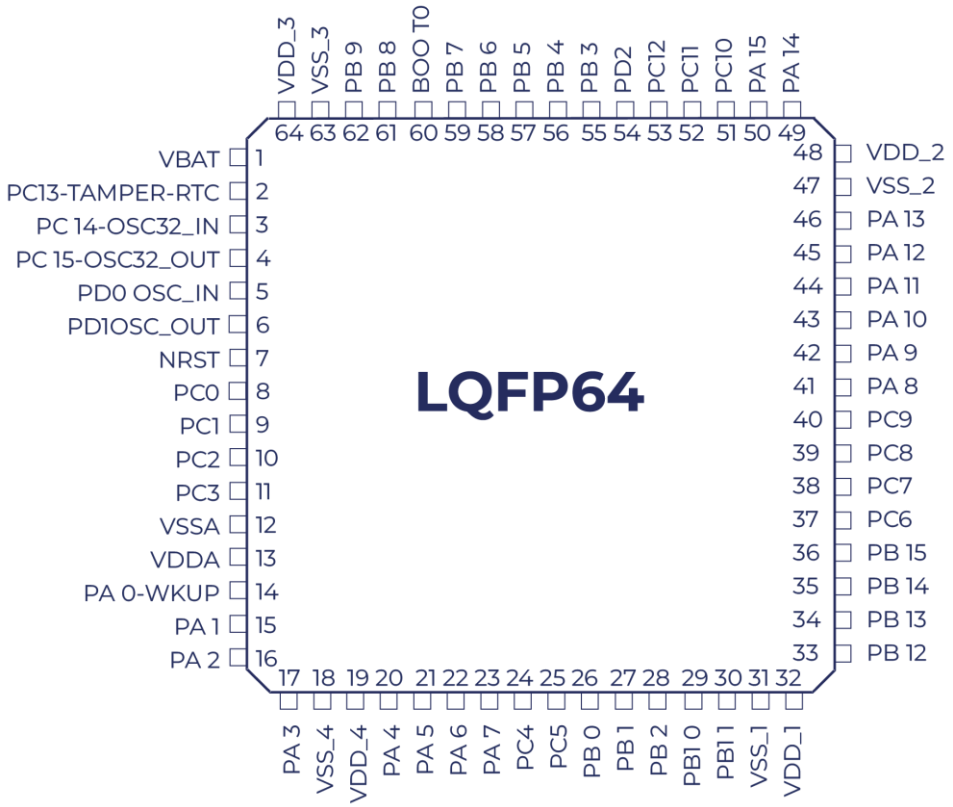


Figure 5. TGS32F103xB LQFP48 pin distribution

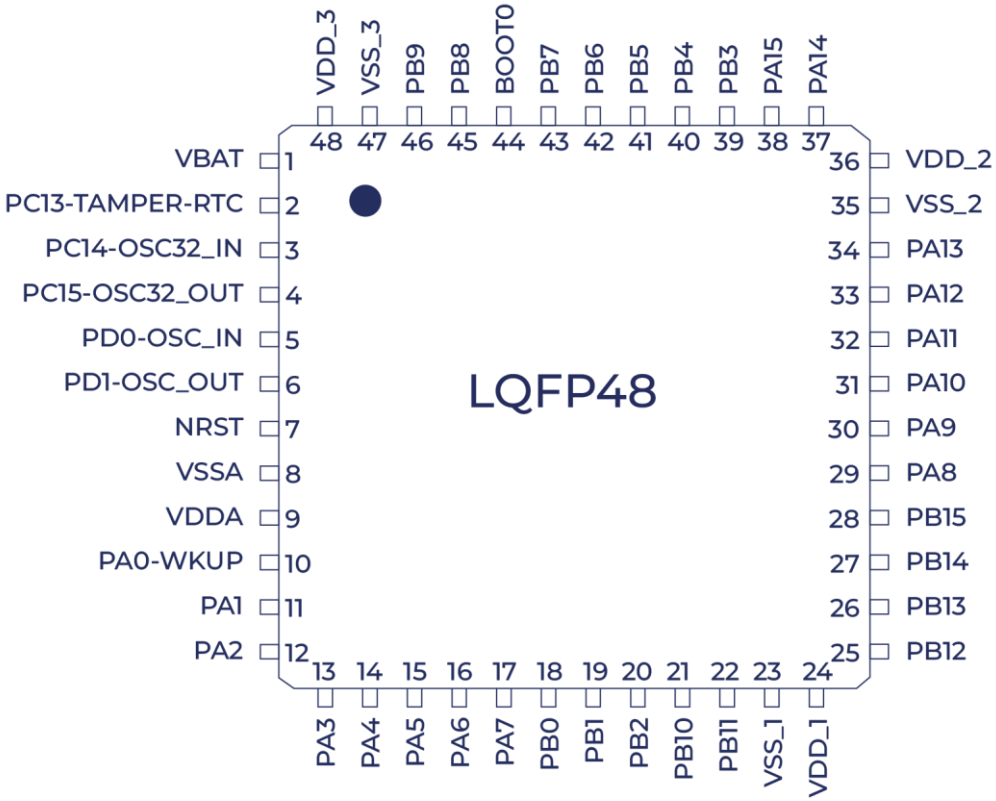


Figure 6. TGS32F103xB QFN36 pin distribution

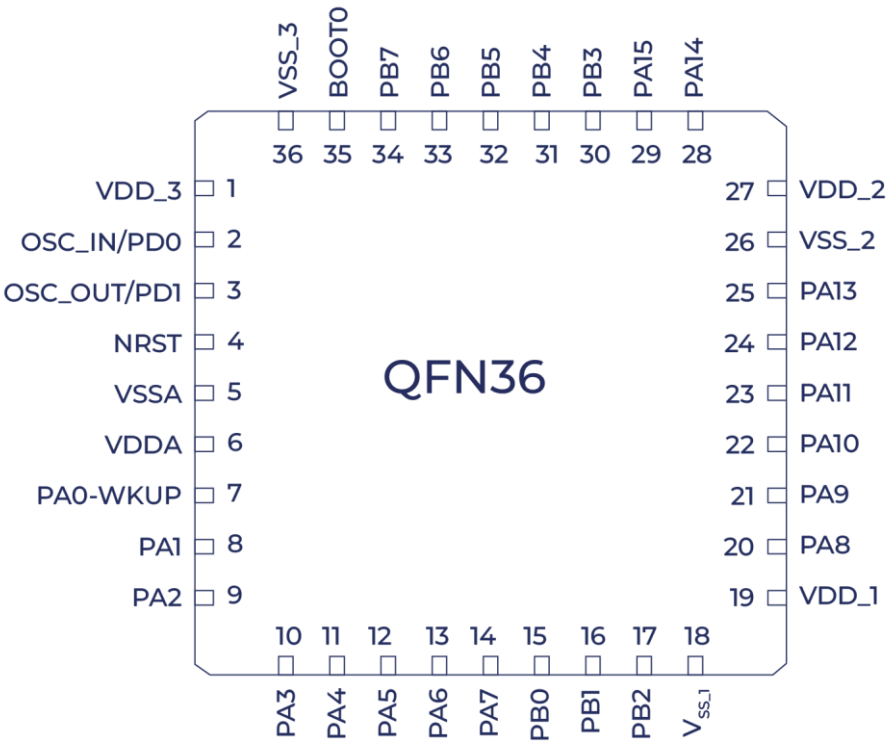


Table 2. TGS32F103XBxx pins definition

Foot position				Pin name	Type(1)	IO level(2)	Main function(3) (after reset)	Optional reuse function	
LQFP48	LQFP64	LQFP100	QFPN36					Default reuse function	Redefine function
-	-	1	-	PE2	I/O	FT	PE2	TRACECK	
-	-	2	-	PE3	I/O	FT	PE3	TRACED0	
-	-	3	-	PE4	I/O	FT	PE4	TRACED1	
-	-	4	-	PE5	I/O	FT	PE5	TRACED2	
-	-	5	-	PE6	I/O	FT	PE6	TRACED3	
1	1	6	-	VBAT	S		VBAT		
2	2	7	-	PC13-TAMPER- RTC	I/O		PC13	TAMPER-RTC	
3	3	8	-	PC14- OSC32_IN	I/O		PC14	OSC32_IN	
4	4	9	-	PC15-OSC32_OUT (5)	I/O		PC15	OSC32_OUT	
-	-	10	-	VSS_5	S		VSS_5		
-	-	11	-	VDD_5	S		VDD_5		
5	5	12	2	OSC_IN	I		OSC_IN		PD0(7)
6	6	13	3	OSC_OUT	O		OSC_OUT		PD1(7)
7	7	14	4	NRST	I/O		NRST		
-	8	15	-	PC0	I/O		PC0	ADC12_IN10	
-	9	16	-	PC1	I/O		PC1	ADC12_IN11	
-	10	17	-	PC2	I/O		PC2	ADC12_IN12	
-	11	18	-	PC3	I/O		PC3	ADC12_IN13	
8	12	19	5	VSSA	S		VSSA		
-	-	20	-	VREF-	S		VREF-		
-	-	21	-	VREF+	S		VREF+		
9	13	22	6	VDDA	S		VDDA		

10	14	23	7	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS /ADC12_IN0/TIM2_CH1_ETR	
11	15	24	8	PA1	I/O		PA1	USART2_RTS /ADC12_IN1/TIM2_CH2	
12	16	25	9	PA2	I/O		PA2	USART2_TX /ADC12_IN2/TIM2_CH3	
13	17	26	10	PA3	I/O		PA3	USART2_RX /ADC12_IN3/TIM2_CH4	
-	18	27	-	VSS_4	S		VSS_4		
-	19	28	-	VDD_4	S		VDD_4		
14	20	29	11	PA4	I/O		PA4	SPI1_NSS /USART2_CK /ADC12_IN4	
15	21	30	12	PA5	I/O		PA5	SPI1_SCK /ADC12_IN5	
16	22	31	13	PA6	I/O		PA6	SPI1_MISO /ADC12_IN6/TIM3_CH1	TIM1_BKIN
17	23	32	14	PA7	I/O		PA7	SPI1_MOSI /ADC12_IN7/TIM3_CH2	TIM1_CH1N
-	24	33		PC4	I/O		PC4	ADC12_IN14	
-	25	34		PC5	I/O		PC5	ADC12_IN15	
18	26	35	15	PB0	I/O		PB0	ADC12_IN8/TIM3_CH3	TIM1_CH2N

Foot position				Pin name	Type(1)	IO level(2)	Main function(3) (after reset)	Optional reuse function	
LQFP48	LQFP64	LQFP100	QFPN36					Default reuse function	Redefine function
19	27	36	16	PB1	I/O		PB1	ADC12_IN9/TIM3_CH4	TIM1_CH3N
20	28	37	17	PB2	I/O	FT	PB2/BOOT1		
-	-	38	-	PE7	I/O	FT	PE7		TIM1_ETR
-	-	39	-	PE8	I/O	FT	PE8		TIM1_CH1N
-	-	40	-	PE9	I/O	FT	PE9		TIM1_CH1
-	-	41	-	PE10	I/O	FT	PE10		TIM1_CH2N
-	-	42	-	PE11	I/O	FT	PE11		TIM1_CH2
-	-	43	-	PE12	I/O	FT	PE12		TIM1_CH3N
-	-	44	-	PE13	I/O	FT	PE13		TIM1_CH3
-	-	45	-	PE14	I/O	FT	PE14		TIM1_CH4
-	-	46	-	PE15	I/O	FT	PE15		TIM1_BKIN
21	29	47	-	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
22	30	48	-	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
23	31	49	18	V_{SS_1}	S		V_{SS_1}		
24	32	50	19	V_{DD_1}	S		V_{DD_1}		
25	33	51	-	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBAI/USART3_CK /TIM1_BKIN	
26	34	52	-	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS /TIM1_CH1N	
27	35	53	-	PB14	I/O	FT	PB14	SPI2_MISO/USART3_RTS TIM1_CH2N	

28	36	54	-	PB15	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N	
-	-	55	-	PD8	I/O	FT	PD8		USART3_TX
-	-	56	-	PD9	I/O	FT	PD9		USART3_RX
-	-	57	-	PD10	I/O	FT	PD10		USART3_CK
-	-	58	-	PD11	I/O	FT	PD11		USART3_CTS
-	-	59	-	PD12	I/O	FT	PD12		TIM4_CH1 /USART3_RTS
-	-	60	-	PD13	I/O	FT	PD13		TIM4_CH2
-	-	61	-	PD14	I/O	FT	PD14		TIM4_CH3
-	-	62	-	PD15	I/O	FT	PD15		TIM4_CH4
-	37	63	-	PC6	I/O	FT	PC6		TIM3_CH1
	38	64	-	PC7	I/O	FT	PC7		TIM3_CH2
	39	65	-	PC8	I/O	FT	PC8		TIM3_CH3
-	40	66	-	PC9	I/O	FT	PC9		TIM3_CH4
29	41	67	20	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1 /MCO	
30	42	68	21	PA9	I/O	FT	PA9	USART1_TX /TIM1_CH2	
31	43	69	22	PA10	I/O	FT	PA10	USART1_RX /TIM1_CH3	
32	44	70	23	PA11	I/O	FT	PA11	USART1_CTS/CANRX /USBDM/TIM1_CH4	
33	45	71	24	PA12	I/O	FT	PA12	USART1_RTS/ CANTX/USBDPTIM 1_ETR	
34	46	72	25	PA13	I/O	FT	JTMS/SWDIO		PA13
-	-	73	-	Not connected					
35	47	74	26	V_{SS_2}	S		V_{SS_2}		
36	48	75	27	V_{DD_2}	S		V_{DD_2}		
37	49	76	28	PA14	I/O	FT	JTCK/SWCLK		PA14
38	50	77	29	PA15	I/O	FT	JTDI		TIM2_CH1_ETR/ PA15 /SPI1_NSS

Foot position				Pin name	Type(1)	IO level(2)	Main function(3) (after reset)	Optional reuse function	
LQFP48	LQFP64	LQFP100	QFPN36					Default reuse function	Redefine function
-	51	78		PC10	I/O	FT	PC10		USART3_TX
-	52	79		PC11	I/O	FT	PC11		USART3_RX
-	53	80		PC12	I/O	FT	PC12		USART3_CK
-	-	81	2	PD0	I/O	FT	PD0		CANRX
-	-	82	3	PD1	I/O	FT	PD1		CANTX
	54	83	-	PD2	I/O	FT	PD2	TIM3_ETR	
-	-	84	-	PD3	I/O	FT	PD3		USART2_CTS
-	-	85	-	PD4	I/O	FT	PD4		USART2_RTS
-	-	86	-	PD5	I/O	FT	PD5		USART2_TX
-	-	87	-	PD6	I/O	FT	PD6		USART2_RX
-	-	88	-	PD7	I/O	FT	PD7		USART2_CK
39	55	89	30	PB3	I/O	FT	JTDO		TIM2_CH2 /PB3TRACESWOSP I1_SCK
40	56	90	31	PB4	I/O	FT	JNTRST		TIM3_CH1/PB4/SPI 1_MISO
41	57	91	32	PB5	I/O		PB5	I2C1_SMBAl	TIM3_CH2 /SPI1_MOSI
42	58	92	33	PB6	I/O	FT	PB6	I2C1_SCL /TIM4_CH1	USART1_TX
43	59	93	34	PB7	I/O	FT	PB7	I2C1_SDA /TIM4_CH2	USART1_RX
44	60	94	35	BOOT0	I		BOOT0		
45	61	95	-	PB8	I/O	FT	PB8	TIM4_CH3	I2C1_SCL /CANRX
46	62	96	-	PB9	I/O	FT	PB9	TIM4_CH4	I2C1_SDA/CANTX
-	-	97	-	PE0	I/O	FT	PE0	TIM4_ETR	

-	-	98	-	PE1	I/O	FT	PE1		
47	63	99	36	V_{SS_3}	S		V_{SS_3}		
48	64	100	1	V_{DD}_3	S		V_{DD}_3		

1. I = input, O = output, S = power supply

2. FT: 5 V voltage tolerance

3. PC13, PC14 and PC15 pins are powered by the power switch, and this power switch can only sink limited current (3 mA). Therefore, these three pins have the following limitations when used as output pins: only one pin can be used as an output at the same time. When used as an output pin, it can only work in 2 MHz mode, the maximum driving load is 30 pF, and it cannot be used as a current source (Such as driving LED).

4. These pins are in the main function state when the backup area is powered on for the first time. Even if reset later, the status of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these IO ports, please refer to the relevant chapters of the battery backup area and BKP register in the TGS32F103xB reference manual.

5. This type of alternate function can be configured by software to other pins (if the corresponding package model has this pin). For details, please refer to the alternate function I/O chapter and debugging settings chapter of the TGS32F103xB reference manual.

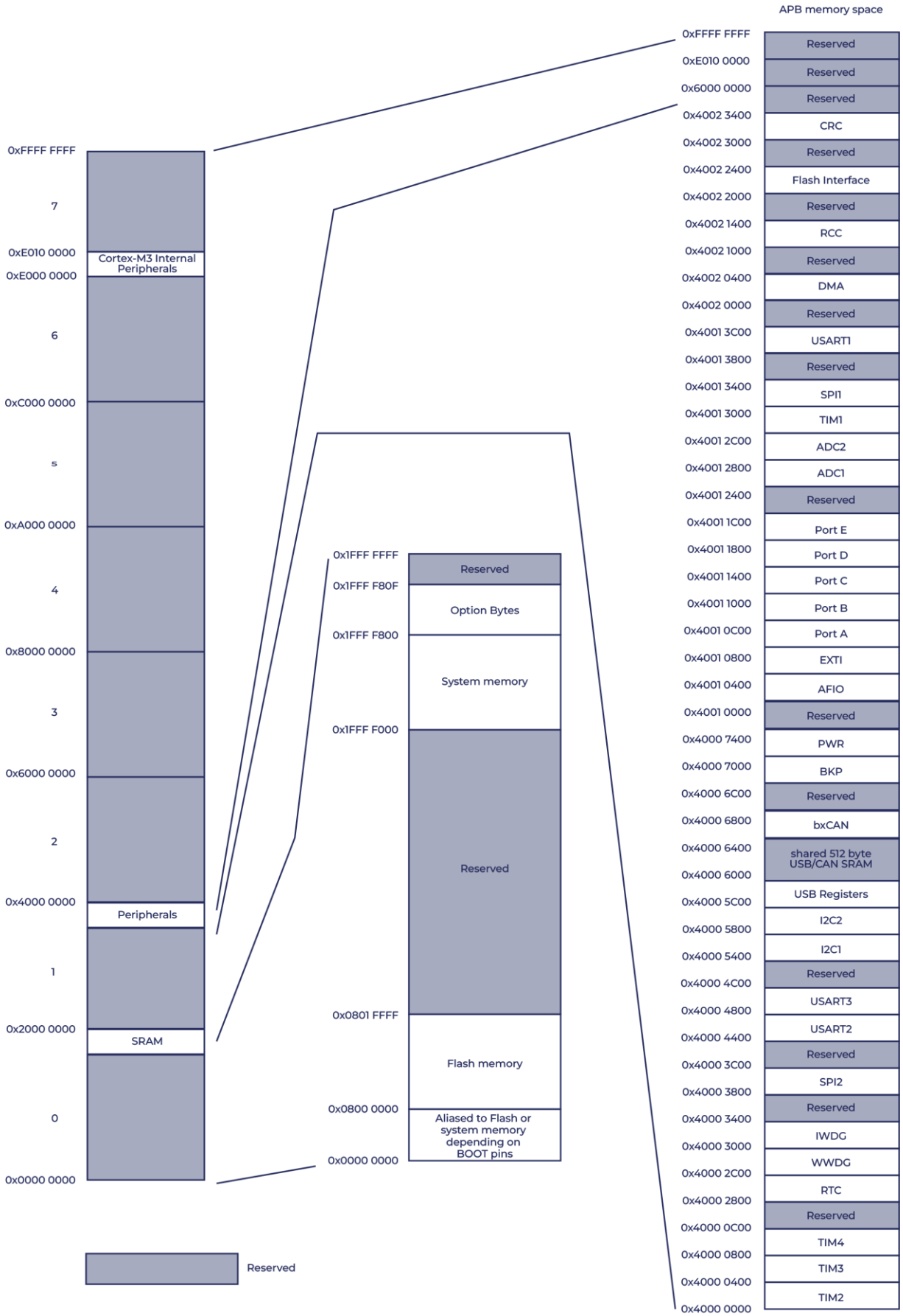
6. Pins 2 and 3 of the QFN36 package, and pins 5 and 6 of the LQFP48 and LQFP64 packages are configured as OSC_IN and OSC_OUT function pins by default after the chip is reset. Software can reset these two pins to the PD0 and PD1 functions. But for the LQFP100 package, since PD0 and PD1 are inherent function pins, there is no need to reimage settings by software. For more details, please refer to the Alternate Function I/O Chapter and Debug Settings Chapter of the TGS32F103xB Reference Manual. In output mode, PD0 and PD1 can only be configured in 50MHz output mode.

7. ADC12_INx (x represents an integer between 0 and 15) appears in the pin name label in the table, indicating that this pin can be ADC1_INx or ADC2_INx. For example: ADC12_IN9 means that this pin can be configured as ADC1_IN9 or ADC2_IN9.

8. Pin PA0 in the table corresponds to TIM2_CH1_ETR in the multiplex function, which means that the function can be configured as TIM2_TI1 or TIM2_ETR. Similarly, the name TIM2_CH1_ETR of the remapping multiplexing function corresponding to PA15 has the same meaning.

4. Memory image

Figure 7. Memory MAP diagram



5. Electrical Characteristics

5.1 Test conditions

Unless otherwise stated, all voltages are referenced to VSS.

5.1.1 Minimum and maximum values

Unless otherwise stated, all minimum and maximum values will be based on worst-case testing performed on 100% of the product on the production line at an ambient temperature of T_A = 25°C and T_A = T_{Amax} (T_{Amax} matches the selected temperature range). Guaranteed under ambient temperature, supply voltage and clock frequency conditions.

In the notes below each table, it is stated that the data is obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line; on the basis of comprehensive evaluation, the minimum and maximum values are obtained after passing sample testing. It is obtained by taking the average value and adding or subtracting three times the standard distribution (average ±3∑).

5.1.2 Typical values

Unless otherwise stated, typical data is based on T_A = 25°C and V_{DD} = 3.3 V (2V ≤ V_{DD} ≤ 3.3V voltage range). These data are for design guidance only and have not been tested.

Typical ADC accuracy values are obtained by sampling a standard batch and testing over all temperature ranges. 95% of the products have an error less than or equal to the given value (average ±2 Σ).

5.1.3 Typical curve

Unless otherwise stated, typical curves are for design guidance only and have not been tested.

5.1.4 Load capacitance

The load conditions when measuring pin parameters are shown in Figure 8.

5.1.5 Pin input voltage

How the input voltage on the pin is measured is shown in Figure 9.

Figure 8 Pin load conditions

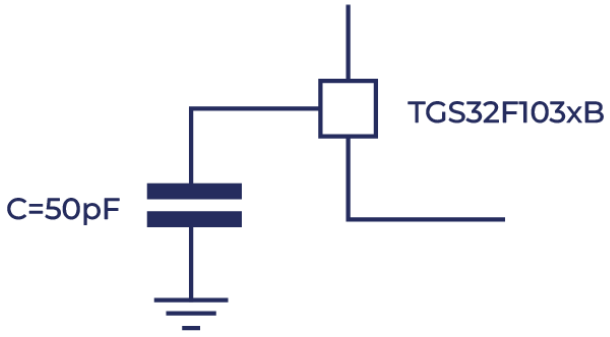
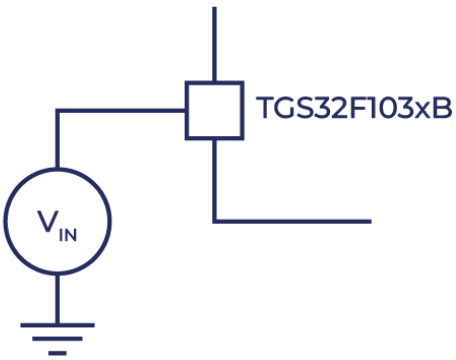
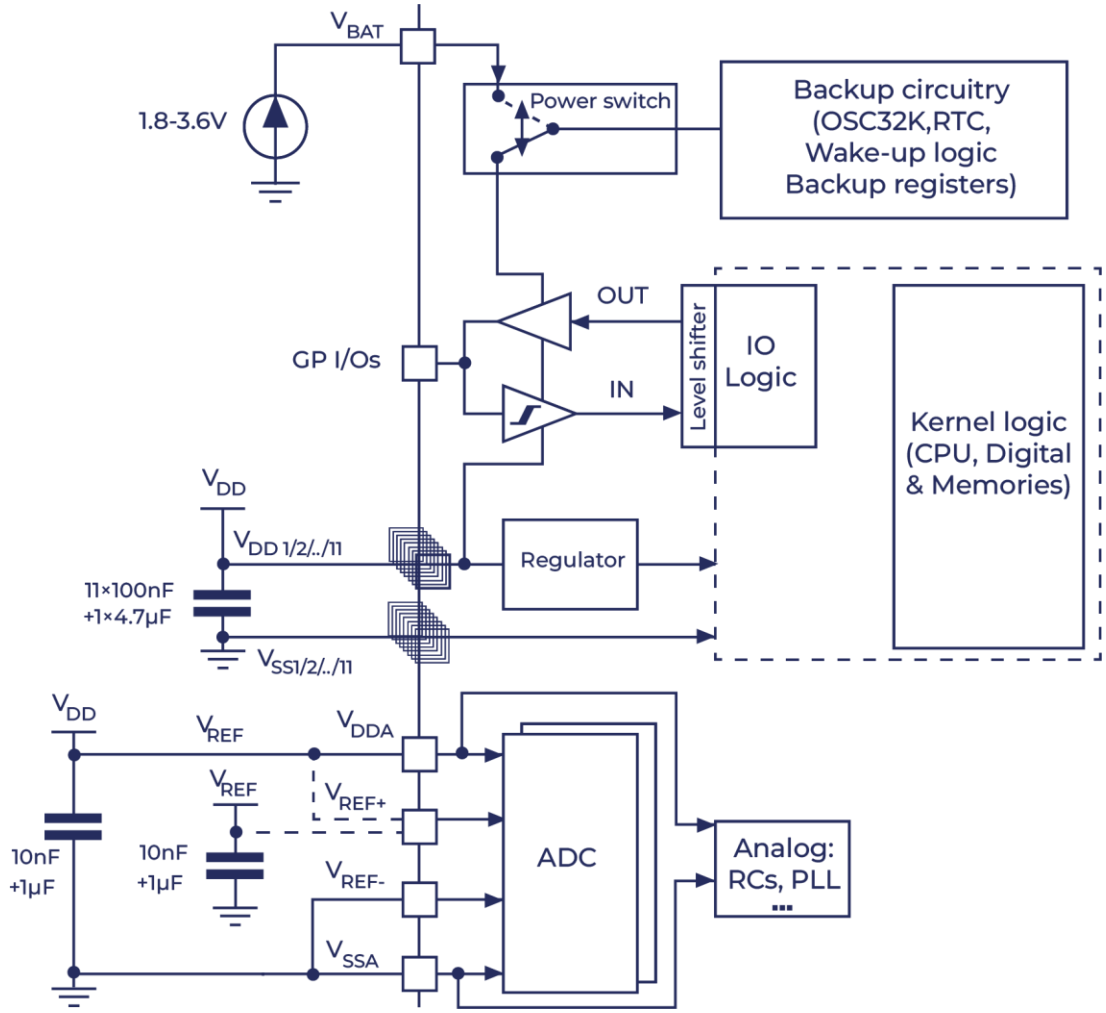


Figure 9 Pin input voltage



5.1.6 Power supply solution

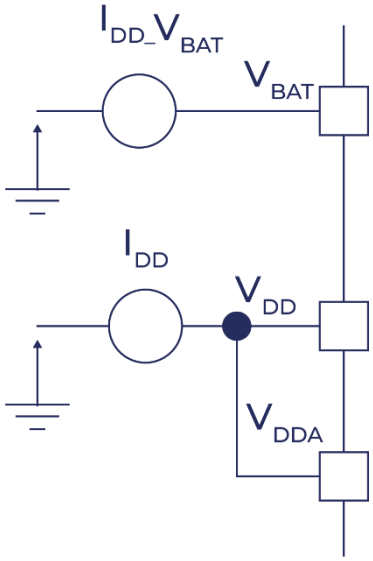
Figure 10. Power supply scheme



Note: The 4.7uf capacitor in the above picture must be connected to V_{DD3}.

5.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



5.2 Absolute Maximum Ratings

Loads applied to the device in excess of those given in the absolute maximum ratings tables (Table 3, Table 4, Table 5) may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device is correct under this condition. Long-term operation of the device under maximum conditions will affect the reliability of the device.

Table 3. Voltage characteristics

Symbol	Describe	Minimum value	Maximum value	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})(1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pins(2)	V_{SS} -0.3	V_{DD} +4.0	
	Input voltage on other pins(2)	V_{SS} -0.3	4.0	
$\|\Delta V_{DDx}\|$	The voltage difference between different supply pins	-	50	mV
$\|V_{SSx} - V_{SS}\|$	The voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD electrostatic discharge voltage (human body model)	See Section 5.3.11		

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to an external power supply system within the allowed range.

2. $I_{INJ(PIN)}$ must not exceed its limit (see Table 4), that is, ensure that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it must also be ensured that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When $V_{IN} > V_{INmax}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.

Table 4. Current Characteristics

Symbol	Describe	Maximum value	Unit
I_{VDD}	Total current through the V_{DD}/V_{DDA} power lines (supply current)(1)	150	mA
I_{VSS}	Total current through V_{SS} ground (outgoing current)(1)	150	
I_{IO}	Output sink current on any I/O and control pins	25	
	Output current on any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2)	5V Tolerant Pin Injection Current	-5/+0	
	Injection current from other pins(4)	±5	
$\sum I_{INJ(PIN)}$	Total injected current on all I/O and control pins(4)	±25	

1. All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within the allowed range.

2. $I_{INJ(PIN)}$ must not exceed its limit, that is, ensure that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it must also be ensured that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.

3. Reverse injection of current can interfere with the analog performance of the device. See Section 5.3.17.

4. When several I/O ports have injection currents at the same time, the maximum value of $\Sigma I_{INJ(PIN)}$ is the sum of the immediate absolute values of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum value of $\Sigma I_{INJ(PIN)}$ on the device's 4 I/O ports.

Table 5. Temperature characteristics

Symbol	Describe	Numerical value	Unit
T_{STG}	Storage temperature range	-65~+150	°C
T_J	Maximum junction temperature	150	°C

5.3 Working conditions

5.3.1 General working conditions

Table 6. General operating conditions

Symbol	Parameter	Condition		Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-		0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-		0	36	
f_{PCLK2}	Internal APB2 clock frequency	-		0	72	
V_{DD}	Standard working voltage	-		2	3.6	V
V_{DDA}(1)	Analog section operating voltage (ADC not used)	Must be the same as V_{DD}(2)		2	3.6	
	Analog part operating voltage (using ADC)			2.4	3.6	
V_{BAT}	Backup part of the working voltage	-		1.8	3.6	
V_{IN}	I/O input voltage	Standard I/O		-0.3	V_{DD}+0.3	
		FT I/O	2V < V_{DD} < 3.6V	-0.3	5.5	
			V_{DD} = 2V	-0.3	5.2	
		BOOT0		0	5.5	
P_D	Power dissipation	LQFP100		-	434	mW
		LQFP64		-	444	
		LQFP48		-	363	
		QFN36		-	1000	
T_A	Ambient temperature	Maximum power dissipation		-45	105	°C
		Low power dissipation(4)		-45	105	
T_J	Junction temperature range	Temperature label		-60	150	

1. When using the ADC, see Table 43.

2. It is recommended to use the same power supply to power V_{DD} and V_{DDA}, and a maximum of 300mV difference between V_{DD} and V_{DDA} is allowed during power-up and normal operation.

3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see Section 1).

4. Under lower power dissipation conditions, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see Section 1).

5.3.2 Operating conditions when powering on and off

The parameters given in the table below are tested under general working conditions.

Table 7. Operating conditions during power-on and power-down

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
t_{VDD}	V_{DD} rising rate	-	0	∞	µs/V
	V_{DD} falling rate		20	∞	

5.3.3 Embedded reset and power control module features

The parameters given in the table below are based on testing at the ambient temperatures and V_{DD} supply voltage listed in Table 6.

Table 8. Embedded Reset and Power Control Module Features

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]= 101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]= 101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]= 110 (rising edge)	2.66	2.78	2.90	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.80	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3.00	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.90	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-off reset threshold	falling edge	1 8(1)	1.88	1.96	V
		rising edge	1.84	1.92	2.0	V
$V_{PVDhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$(2)	Reset duration	-	1	2.5	4.5	ms

1. Product characteristics are guaranteed by design to the minimum value $V_{POR/PDR}$.

2. Guaranteed by design, not tested in production.

5.3.4 Built-in reference voltage

The parameters given in the table below are based on testing at the ambient temperatures and V_{DD} supply voltage listed in Table 6.

Table 9. Built-in reference voltage

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
		-45°C < T_A< +105°C	1.16	1.20	1.26	V
$T_{S\_vrefint}$(1)	When reading the internal reference voltage, the ADC's Sampling time	-	-	5.1	(2) 17.1	μs

1. Product characteristics are guaranteed by design to the minimum value $V_{POR/PDR}$.

2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

Current consumption is a comprehensive indicator of multiple parameters and factors, including operating voltage, ambient temperature, load on I/O pins, product software configuration, operating frequency, I/O pin toggle rate, program memory The location and code executed, etc.

The current consumption measurement method is explained in Figure 11.

All run-mode current consumption measurements given in this section are obtained while executing a simplified set of code.

Dhrystone 2.1 code equivalent results.

Maximum current consumption

The microcontroller is under the following conditions:

• All I/O pins are in input mode and connected to a quiescent level - V_{DD} or V_{SS} (no load).

• All peripherals are turned off unless otherwise noted.

• The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycles when 0~24 MHz, 0 wait cycles when 24 ~ 48 MHz 1 waiting period, 2 waiting periods when exceeding 48MHz).

• Instruction prefetch function is turned on (tip: this parameter must be set before setting the clock and bus frequency division).

• When peripheral is enabled: $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$.

The parameters given in Table 10, Table 11 and Table 12 are based on testing at the ambient temperature and V_{DD} supply voltage listed in Table 5.

Table 10. Maximum current consumption in run mode, data processing code running from internal flash memory

Symbol	Parameter	Condition	f_{HCLK}	Max(1)		Unit
				T_A= 85°C	T_A= 105°C	
IDD	Supply current in run mode	External clock, enables all peripherals(2)	72MHz	21.5	26.88	mA
			48MHz	14.3	17.88	
			32MHz	10.1	12.63	
			24MHz	8.6	10.75	
			16MHz	5.5	6.88	
			8MHz	3.0	3.75	
		External clock, turn off all peripherals(2)	72MHz	13.4	16.75	
			48MHz	11.2	14.00	
			32MHz	6.6	8.25	
			24MHz	5.1	6.38	
			16MHz	3.4	4.25	
			8MHz	2.0	2.50	

1. Derived from comprehensive evaluation and not tested in production.

2. The external clock is 8MHz, and the PLL is enabled when f_{HCLK}>8MHz.

Table 11. Maximum Current Consumption in Run Mode, Data Processing Code Running from Internal RAM

Symbol	Parameter	Condition	f_{HCLK}	Max(1)		Unit
				T_A= 85°C	T_A= 105°C	
I_{DD}	Supply current in run mode	External clock, enables all peripherals(2)	72MHz	16.9	21.13	mA
			48MHz	12.6	15.75	
			32MHz	8.0	10	
			24MHz	6.0	7.5	
			16MHz	4.2	5.25	
			8MHz	2.6	3.25	
		External clock, turn off all peripherals(2)	72MHz	7.5	9.38	
			48MHz	5.9	7.38	
			32MHz	4.0	5.00	
			24MHz	3.5	4.38	
			16MHz	2.8	3.50	
			8MHz	1.7	2.13	

1. Based on comprehensive evaluation, V_{DDmax} is used in production

2. The external clock is 8MHz, and the PLL is enabled when f_{HCLK}>8MHz.

Table 12. Maximum current consumption in sleep mode, code running in Flash or RAM

Symbol	Parameter	Condition	f_{HCLK}	Max(1)		Unit
				T_A= 85°C	T_A= 105° C	
I_{DD}	Supply current in sleep mode	External clock, enable all peripherals(2)	72MHz	17.1	21.38	mA
			48MHz	11.2	14.00	
			32MHz	8.2	10.25	
			24MHz	6.9	8.63	
			16MHz	4.2	5.25	
			8MHz	2.6	3.25	
		External clock, turn off all peripherals(2)	72MHz	6.8	8.50	
			48MHz	3.5	4.38	
			32MHz	3.1	3.88	
			24MHz	2.7	3.38	
			16MHz	1.9	2.38	
			8MHz	1.2	1.50	

1. Based on comprehensive evaluation, tested in production with V_{DDmax} and peripherals enabled at f_{HCLK} max.

2. The external clock is 8MHz, and the PLL is enabled when f_{HCLK} > 8 MHz.

Table 13. Typical and maximum current consumption in shutdown and standby modes

Symbol	Parameter	Condition	Typical value		Maximum value		Unit
			V_{DD}/V_{BAT} = 2.4V	V_{DD}/V_{BAT} = 3.3V	T_A = 85°C	T_A = 105°C	
I_{DD}	Supply current in shutdown mode	Regulator is in run mode, low speed and high speed internal RC Oscillator and high-speed oscillator are off (no independent watchdog)	22.7	23.4	300	385	μA
		The regulator is in low power mode, low speed and high speed internal RC oscillator and high-speed oscillator are off (no independent watchdog)	9.1	10.3	260	340	
	Supply current in standby mode	The low speed internal RC oscillator and independent watchdog are on On state	2.4	3.4	-	-	
		The low-speed internal RC oscillator is on and viewed independently Door dog is off	2.3	3.3	-	-	
		The low-speed internal RC oscillator and independent watchdog are turned off status, the low-speed oscillator and RTC are off	1.5	2.0	4	6	
I_{DD_VBAT}	Backup area supply current	Low speed oscillator and RTC are on	1.1	1.4	1.9(2)	3.2	

1. Typical values are measured at T_A = 25°C.

2. Derived from comprehensive evaluation and not tested in production.

Typical current consumption

The MCU is under the following conditions:

• All I/O pins are in input mode and connected to a quiescent level - V_{DD} or V_{SS} (no load).

• All peripherals are turned off unless otherwise noted.

• The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycles when 0 ~ 24 MHz, 1 wait cycle when 24 ~ 48 MHz, and 2 wait cycles when it exceeds 48 MHz).

• Ambient temperature and V_{DD} supply voltage conditions are listed in Table 6.

• Instruction prefetch function is turned on (tip: this parameter must be set before setting the clock and bus frequency division). When turning on peripherals:

• $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$.

Table 14. Typical current consumption in Run mode, data processing code running from internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Typical value(1)		Unit
				Enable all peripherals (2)	Turn off all peripherals	
I_{DD}	Supply current in run mode	External clock(3)	72MHz	20.9	11.9	mA
			48MHz	14.2	8.3	
			24MHz	7.8	4.6	
			8MHz	3.2	2.1	

1. Typical values are measured at T_A = 25°C and V_{DD} = 3.3 V.

2. Each ADC in the analog section adds an additional 0.8 mA current consumption. In the application environment, this part of the current will only increase when the ADC is turned on (the ADON bit of the ADC_CR2 register is set).

3. The external clock is 8MHz, and the PLL is enabled when f_{HCLK} > 8 MHz.

Table 15. Typical current consumption in run mode, data processing code running from internal RAM

Symbol	Parameter	Condition	f_{HCLK}	Typical value(1)		Unit
				Enable all peripherals (2)	Turn off all peripherals	
IDD	Supply current in run mode	External clock(3)	72MHz	17.8	8.6	mA
			48MHz	13.0	7.6	
			24MHz	7.2	4.3	
			8MHz	3.4	2.4	

1. Typical values are measured at T_A = 25°C and V_{DD} = 3.3 V.

2. Each ADC in the analog section adds an additional 0.8mA current consumption. In the application environment, this part of the current will only increase when the ADC is turned on (the ADON bit of the ADC_CR2 register is set).

3. The external clock is 8MHz, and the PLL is enabled when f_{HCLK} > 8 MHz.

Table 16. Typical current consumption in sleep mode with data processing code running from internal Flash or RAM

Symbol	Parameter	Condition	f_{HCLK}	Typical value(1)		Unit
				Enable all peripherals(2)	Turn off all peripherals	
IDD	Power supply in sleep mode flow	External clock(3)	72MHz	15.1	5.4	mA

1. Typical values are measured at T_A = 25°C and V_{DD} = 3.3 V.

2. Each ADC in the analog section adds an additional 0.8 mA current consumption. In the application environment, this part of the current will only increase when the ADC is turned on (the ADON bit of the ADC_CR2 register is set).

3. The external clock is 8 MHz, and the PLL is enabled when f_{HCLK} > 8 MHz.

Built-in peripheral current consumption

The current consumption of the built-in peripherals is listed in Table 17. The operating conditions of the MCU are as follows:

• All I/O pins are in input mode and connected to a quiescent level - V_{DD} or V_{SS} (no load).

• All peripherals are turned off unless otherwise noted.

• The values given are calculated by measuring the current consumption

- Turn off clocks to all peripherals

- Only turn on the clock of one peripheral

• Ambient temperature and VDD supply voltage conditions are listed in Table 4.

Table 17. Current consumption of built-in peripherals(1)

Built-in peripherals		Typical power consumption at 25°C	Unit	Built-in peripherals		Typical power consumption at 25°C	Unit
APB1	TIM2	1.2	mA	APB2	GPIOA	0.47	mA
	TIM3	1.2			GPIOB	0.47	
	TIM4	0.9			GPIOC	0.47	
	SPI2	0.2			GPIOD	0.47	
	USART2	0.35			GPIOE	0.47	
	USART3	0.35			ADC1(2)	1.81	
	I^2C1	0.39			ADC2	1.78	
	I^2C2	0.39			TIM1	1.6	
	USB	0.65			SPI1	0.43	
	CAN	0.72			USART1	0.85	

1. f_{HCLK}=72MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, the prescaler coefficient of each peripheral is the default value.

2. Special conditions for ADC: f_{HCLK}=56MHz, fAPB1 = f_{HCLK}/2, f_{APB2} = f_{HCLK}, f_{ADCCLK} = f_{APB2}/4, ADON=1 in ADC_CR2 register.

5.3.6 External clock source characteristics

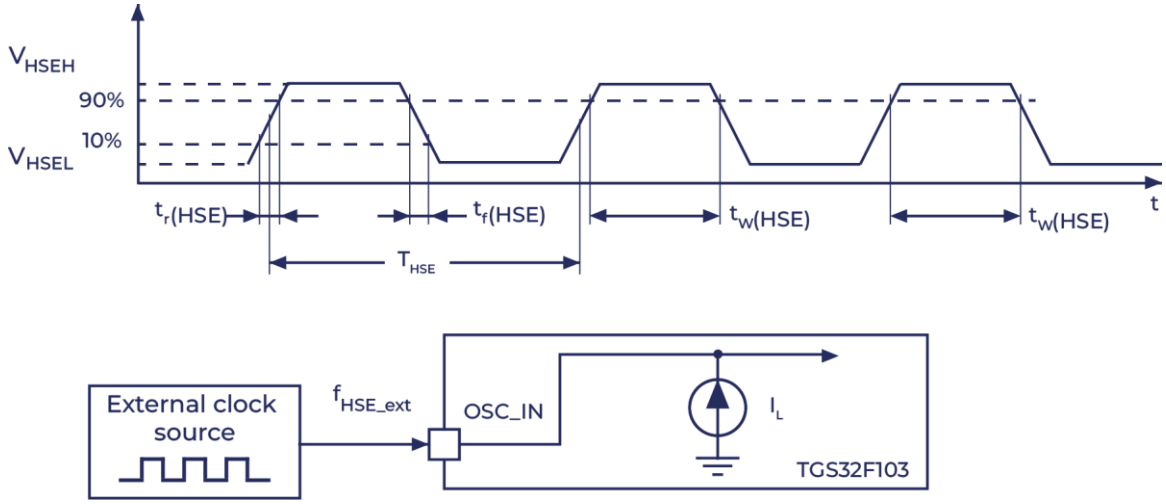
High-speed external user clock generated from external oscillator source the characteristic parameters given in the following table are measured using a high-speed external clock source, and the ambient temperature and supply voltage comply with the conditions of Table 6.

Table 18. High-speed external user clock characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HSE_ext}	User external clock frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		2.2	-	3.3	V
V_{HSEL}	OSC_IN input pin low level voltage		0	-	2.2	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitive reactance	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	50	55	%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$		0.3	±1	µA

1. Guaranteed by design, not tested in production.

Figure 12. AC timing diagram of external high-speed clock source



Low-speed external user clock generated from external oscillator source

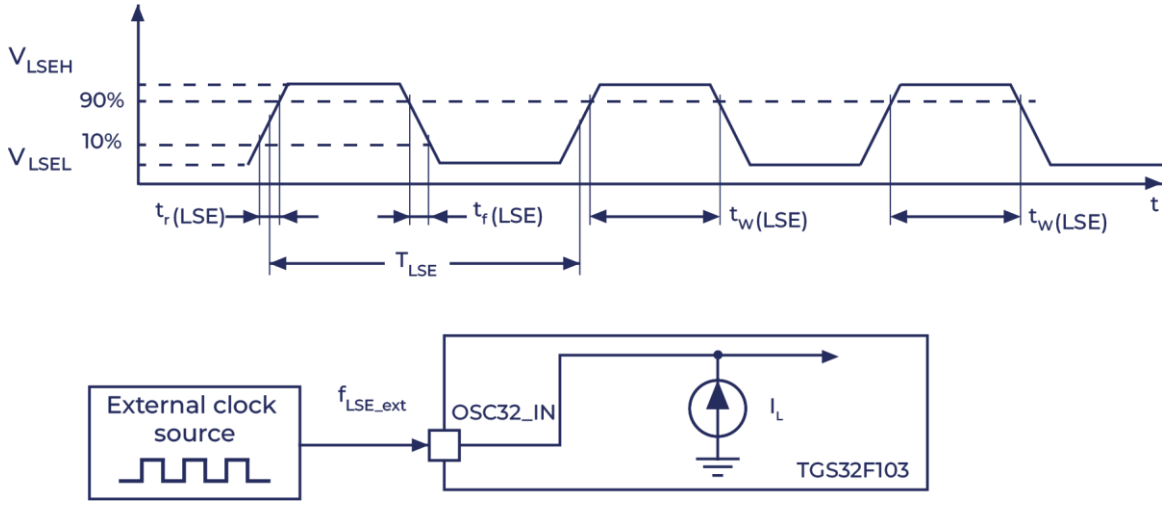
The characteristics parameters given in the following table are measured using a low-speed external clock source, and the ambient temperature and supply voltage comply with the conditions of Table 6.

Table 19. Low-speed external user clock characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{LSE_ext}	User external clock frequency(1)		0	32.768	4000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage		1.8		3.3	V
V_{LSEL}	OSC32_IN input pin low level voltage		0		1.7	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)				50	
$C_{in(LSE)}$	OSC32_IN input capacitive reactance			5		pF
$DuCy_{(LSE)}$	Duty cycle		30	50	70	%
I_L	OSC32_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$		-0.4	±1	µA

1. Guaranteed by design, not tested in production.

Figure 13. AC timing diagram of external low-speed clock source



High-speed external clock generated using a crystal/ceramic resonator

The high-speed external clock (HSE) can be generated using a 4 ~ 16 MHz crystal/ceramic resonator oscillator. The information given in this section is based on a comprehensive characteristic evaluation using typical external components listed in the table below. In the application, the resonator and load capacitor must be placed as close as possible to the oscillator pins to reduce output distortion and settling time at startup.

Table 20 HSE 4~16MHz oscillator characteristics(1)(2)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	feedback resistor	-	-	200	-	kΩ
C_{L1} C_{L2}(3)	Recommended load capacitance corresponds to Crystal Series Resistance (RS)(4)	Rs= 30Ω	-	30	-	pF
i_2	HSE drive current	V_{DD}=3.3V, V_{IN}=V_{SS} 30pF load	-	-	1	mA
g_m	Oscillator transconductance	Start up	25	-	-	mA/V
$t_{SU(HSE)}$ (5)	Start time	V_{DD} stable	-	2	-	ms

1. Characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

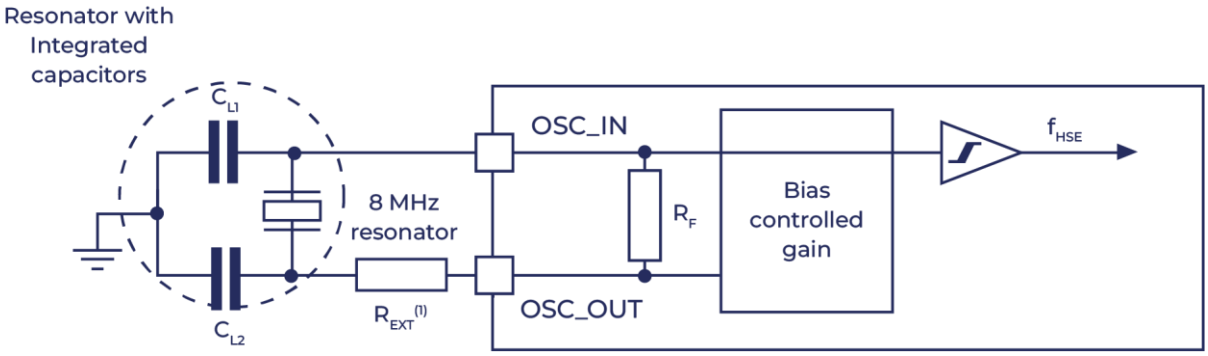
2. Derived from comprehensive evaluation and not tested in production.

3. For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors (typical value) between 5 pF and 25 pF designed for high-frequency applications, and select a crystal or resonator that meets the requirements. Typically C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually specify the load capacitance as a serial combination of C_{L1} and C_{L2}. When selecting C_{L1} and C_{L2}, the capacitive reactance of the PCB and MCU pins should be taken into consideration (the capacitance between the pins and the PCB board can be roughly estimated as 10pF).

4. The relatively low RF resistance value provides protection from problems caused by use in humid environments where leakage and bias conditions change. However, when the MCU is used in harsh humid conditions, this parameter needs to be taken into consideration during design.

5. $t_{SU(HSE)}$ is the startup time, which is the time from when the software enables HSE until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

Figure 14. Typical application using 8MHz crystal



1. The R_{EXT} value is determined by the characteristics of the crystal. Typical values are 5 to 6 times RS.

Low speed external clock generated using a crystal/ceramic resonator

The low-speed external clock (LSE) can be generated using a 32.768 kHz crystal/ceramic resonator oscillator. The information given in this section is based on a comprehensive characterization evaluation using typical external components listed in Table 21. In the application, the resonator and load capacitor must be as close as possible to the oscillator pins to reduce output distortion and settling time at startup.

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors between 5 pF ~ 15 pF and select a crystal or resonator that meets the requirements. Typically, C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually specify the load capacitance as a serial combination of C_{L1} and C_{L2}.

The load capacitance C_L is calculated by the following formula: $C_L = C_{L1}$.

Warning: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF), it is strongly recommended to use resonators with a load capacitance of $C_L \leq 7$ pF. Resonators with a load capacitance of 12.5 pF cannot be used.

For example: If a resonator with load capacitance $C_L = 6$ pF is selected and C_{stray}=2 pF, then $C_{L1} = C_{L2} = 8$ pF.

Table 21. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
R_F	Feedback resistor	-	-	5	-	MΩ
C_{L1} C_{L2}(2)	Recommended load capacitance corresponds to Crystal Series Resistance (RS)(3)	R_S = 30 kΩ	-	-	15	pF
I_2	LSE drive current	V_{DD} = 3.3V, V_{IN} = V_{SS}	-	-	1.4	µA
g_m	Oscillator transconductance	-	5	-	-	µA/V
$t_{SU(LSE)}$ (4)	Start time	V_{DD} stable		3	-	s

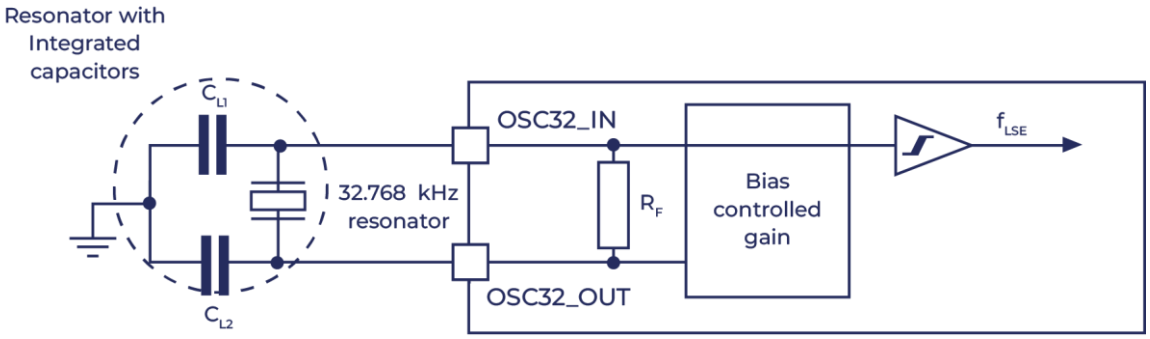
1. Derived from comprehensive evaluation and not tested in production.

2. See the Caution and Warning paragraphs above this form.

3. Choose a high-quality oscillator with a smaller RS value (such as MSIV-TIN32.768kHz) to optimize current consumption.

4. $t_{SU(HSE)}$ is the startup time, which is measured from when the software enables HSE until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

Figure 15. Typical application using 32.768kH crystal



5.3.7 Internal clock source characteristics

The characteristic parameters given in the table below were measured using ambient temperature and supply voltage conditions in accordance with Table 6.

High Speed Internal (HSI) RC Oscillator

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HSI}	Frequency		-	8	-	MHz
ACC_{HSI}	HSI Oscillator Accuracy	T_A= -45 ~ 105°C	-2	-	2.5	%
		T_A= -10 ~ 85°C	-1.5	-	2.2	%
		T_A= 0 ~ 70°C	-1.3	-	2	%
		T_A= 25°C	-1.1	-	1.8	%
$t_{SU(HSI)}$	HSI oscillator startup time		1	-	2	μs
$I_{DD(HSI)}$	HSI Oscillator Power Consumption		-	80	100	μA

1. V_{DD} = 3.3 V, T_A= -45 ~ 105°C, unless otherwise specified.

2. Guaranteed by design, not tested in production.

Low Speed Internal (LSI) RC Oscillator

Table 23. LSI oscillator characteristics(1)

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{SU(LSI)}$(3)	LSI oscillator startup time			85	μs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption		0.65	1.2	μA

1. V_{DD} = 3.3 V, T_A= -45 ~ 105°C, unless otherwise specified.

2. Derived from comprehensive evaluation and not tested in production.

3. Guaranteed by design, not tested in production.

Time to wake up from low power mode

The wake-up times listed in Table 24 were measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

• Stop or Standby mode: clock source is RC oscillator

• Sleep mode: The clock source is the clock used when entering sleep mode

All times are measured using ambient temperature and supply voltage conditions in accordance with Table 6.

Table 24. Wake-up time for low power modes

Symbol	Parameter	Condition	Typical value	Unit
$t_{WUSLEEP}$ (1)	Wake up from sleep mode	Wake up using HSI RC clock	1.7	μs
t_{WUSTOP} (1)	Wake up from shutdown mode (voltage regulation (the machine is in run mode)	HSI RC clock wake-up = 2μs	2.6	
	Wake up from shutdown mode (voltage regulation The device is in low power mode)	HSI RC clock wake-up = 2μs Regulator wake-up time from low-power mode = 5μs	5.1	
$t_{WUSTDBY}$ (3)	Wake up from standby mode	HSI RC clock wake-up = 2μs Regulator wake-up time from shutdown mode = 38μs	52	

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

5.3.8 PLL characteristics

The parameters listed in Table 25 were measured using ambient temperature and supply voltage conditions consistent with Table 6.

Table 25. PLL Characteristics

Symbol	Parameter	Numerical value			Unit
		Minimum value	Typical value	Maximum value	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	50	60	%
f_{PLL_OUT}	PLL multiplied output clock	16		72	MHz
t_{LOCK}	PLL phase lock time		43	200	μs

1. Derived from comprehensive evaluation and not tested in production.

2. It is necessary to pay attention to using the correct frequency multiplication factor so that f_{PLL_OUT} is within the allowable range according to the PLL input clock frequency.

5.3.9 Storage characteristics

Flash memory

Unless otherwise stated, all characteristic parameters are obtained at T_A= -45 ~ 105°C.

Table 26. Flash memory characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{prog}	16-bit programming time	T_A= -45~105°C	-	-	20	μs
t_{ERASE}	Page (1K Byte) erase time	T_A= -45~105°C	-	-	2	ms
t_{ME}	Whole chip erase time	T_A= -45~105°C	-	-	10	
I_{DD}	Supply current	Read mode, f_{HCLK}=72MHz, 2 wait cycles, V_{DD}=3.3V	-	-	21.6	mA
		write/erase mode, f_{HCLK}=72MHz, V_{DD}=3.3V	-	-	3	
		Standby mode, V_{DD}=3.3~3.6V	-	-	1	μA

1. Guaranteed by design, not tested in production.

Table 27. Flash memory life and data retention period

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
N_{END}	Life	T_A= -45 ~ 105°C	100	-	-	Thousands of times
t_{RET}	Data retention period	T_A = -45 ~ 105°C	10	-	-	Year

1. Derived from comprehensive evaluation and not tested in production.

5.3.10 EMC characteristics

Sensitivity testing is done on a sample basis during a comprehensive evaluation of the product.

Functional EMS (Electromagnetic Susceptibility)

When running a simple application (blinking 2 LEDs via the I/O port), the test sample is subjected to 2 types of electromagnetic interference until an error is generated, which is indicated by a blinking LED.

• Electrostatic discharge (ESD) (positive and negative discharge) is applied to all pins of the chip until a functional error occurs. This test meets IEC 1000-4-2 standard.

• FTB: Apply a burst of voltage transients (forward and reverse) through a 100 pF capacitor on V_{DD} and VSS until a functional error occurs. This test complies with IEC 1000-4-4 standard.

A chip reset can restore the system to normal operation. The test results are listed in the table below.

Table 28. EMS characteristics

Symbol	Parameter	Condition	Level/type
V_{FESD}	The voltage limit applied to any I/O pin, causing malfunction.	V_{DD} = 3.3 V, T_A= +25 °C, f_{HCLK} = 72 MHz. Conforms to IEC 1000-4-2	2B
V_{EFTB}	Applied through 100pF capacitors on V_{DD} and V_{SS}, resulting in power erroneous transient burst voltage limit	V_{DD} = 3.3V, T_A= +25 °C, f_{HCLK} = 72 MHz. Conforms to IEC 1000-4-4	4A

Designing Robust Software to Avoid Noise Problems

EMC evaluation and optimization at the device level is performed in a typical application environment. It should be noted that good EMC performance is closely related to the user application and specific software. Therefore, it is recommended that users perform EMC optimization on the software and conduct EMC-related certification tests.

Software recommendations

The software process must include control of program runaway, such as:

• Corrupted program counter

• Unexpected reset

• Critical data is corrupted (control registers, etc...)

Testing before certification

Many common failures (unexpected resets and program counter corruption) can be reproduced by artificially introducing a low level on NRST or a low level on the crystal pin for 1 second.

When conducting ESD testing, voltages that exceed application requirements can be applied directly to the chip. Where unexpected actions are detected, the software needs to be strengthened to prevent unrecoverable errors from occurring.

Electromagnetic Interference (EMI)

Monitor the electromagnetic fields emitted by the chip while running a simple application (blinking 2 LEDs via the I/O port). This emission test complies with the SAE J1752/3 standard, which specifies loading of the test board and pins.

Table 29. EMI Characteristics

Symbol	Parameter	Condition	Monitored frequency band	Maximum value (f_{HSE}/f_{HCLK})		Unit
				8/48MHz	8/72MHz	
S_{EMI}	Peak	V_{DD}= 3.3 V, T_A= 25°C, LQFP100 package, compliant with IEC 61967-2	0.1~30MHz	12	12	dBμV
			30~130MHz	22	19	
			130MHz~1GHz	23	29	
			SAM EMI level	4	4	-

5.3.11 Absolute maximum value (electrical sensitivity)

Based on three different tests (ESD, LU), using specific measurement methods, the chip is strength tested to determine its performance in terms of electrical susceptibility.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse after one second) is applied to all pins of all samples. The size of the sample is related to the number of power supply pins on the chip (3 pieces × (n+1) power supply pins). foot). This test complies with JESD22-A114/C101 standard.

Table 30. ESD absolute maximum values

Symbol	Parameter	Condition	Type	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T = +25 °C, per JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T = +25 °C, per JESD22-C101	II	500	

1. Derived from comprehensive evaluation and not tested in production.

Static latch

To evaluate latch performance, 2 complementary static latch tests were performed on 6 samples:

• Provide supply voltage beyond the limit for each power pin.

• Inject current on every input, output, and configurable I/O pin. This test complies with the EIA/JESD 78E integrated circuit latch-up standard.

Table 31. Electrical sensitivity

Symbol	Parameter	Condition	Type
L_U	Static latch class	T = +25 °C, per JESD78E	Class I A

5.3.12 I/O port characteristics

Universal input/output features

Unless otherwise stated, the parameters listed in the table below are measured according to the conditions in Table 6. All I/O ports are CMOS and TTL.

Table 32. I/O static characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}	low level input voltage	Standard I/O pin, input low level voltage	-	-	0.28 × (V_{DD}-2V) + 0.8V	V
		FT I/O[1] pin, input low level voltage	-	-	0.32 × (V_{DD} - 2V) + 0.75V	
		All I/O ports except BTOOT0	-	-	0.35 V_{DD}	
V_{IH}	High level input voltage	Standard I/O pin, input high power flat voltage	0.41 × (V_{DD}-2V) + 1.3V	-	-	
		FT I/O pin [1], input high level voltage	0.42 × (V_{DD}-2V) + 1V	-	-	
		All I/O ports except BTOOT0	0.65 V_{DD}[2]	-	-	
V_{hys}	Standard I/O Pin Schmidt Trigger voltage hysteresis[2]	-	200	-	-	mV
	5V Tolerant I/O Pin Schmitt Touch Generator voltage hysteresis[2]	-	5%V_{DD}[3]	-	-	-
I_{lkg}	Input leakage current[4]	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/O ports	-	-	±1	μA
		V_{IN} = 5 V, 5 V tolerant port	-	-	3	
R_{PU}	Weak pull-up equivalent resistance[5]	$V_{IN} = V_{SS}$	30	44	50	kΩ
R_{PD}	Weak pull-down equivalent resistance[5]	$V_{IN} = V_{DD}$	30	44	50	
C_{IO}	Capacitance of I/O pins	-	-	5	-	pF

1. FT = 5 V tolerance.

2. Hysteresis voltage of Schmitt trigger switching level. Derived from comprehensive evaluation and not tested in production.

3. Voltage is at least 100 mV.

4. If there is reverse current flow in adjacent pins, the leakage current may be higher than the maximum value.

5. The pull-up and pull-down resistors are designed as a real resistor in series with a switchable PMOS/NMOS implementation. The resistance of this PMON/NMOS switch is very small (about 10%).

All I/O ports are CMOS and TTL compatible (no software configuration required), and their features take into account the most stringent CMOS process or TTL parameters:

• For V_{IH}:

- If V_{DD} is between [2.00 V ~ 3.08 V]; use CMOS characteristics but include TTL.

- If V_{DD} is between [3.08 V ~ 3.60 V]; use TTL feature but include CMOS.

• For V_{IL}:

- If V_{DD} is between [2.00 V ~ 2.28 V]; use TTL feature but include CMOS.

- If V_{DD} is between [2.28 V ~ 3.60 V]; use CMOS characteristics but include TTL.

Output drive current

GPIOs (General Purpose Input/Output Ports) can sink or source up to +/-8 mA, and sink +20 mA (loosely V). In the user's application, the number of I/O pins must be such that the drive current does not exceed the absolute maximum ratings given in Section 5.2:

• The sum of the current drawn by all I/O ports from V_{DD}, plus the maximum operating current drawn by the MCU on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see Table 4).

• The sum of the currents drawn by all I/O ports and drawn from V_{DD}, plus the maximum operating current drawn by the MCU on V_{DD}, cannot exceed the absolute maximum ratings I_{VSS} (see Table 4).

Output voltage

Unless otherwise noted, the parameters listed in Table 33 were measured using ambient temperature and V_{DD} supply voltage conditions consistent with Table 6. All I/O ports are CMOS and TTL compatible.

Table 33. Output voltage characteristics

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$V_{OL}^{(1)}$	Output low level when 8 pins sink current at the same time	CMOS port, I_{IO} =+8mA 2.7V < V_{DD}< 3.6V	-	0.4	V
$V_{OH}^{(2)}$	Output high level, when 8 pins output current at the same time		V_{DD}-0.4	-	
$V_{OL}^{(1)}$	Output low level when 8 pins sink current at the same time	TLL port, I_{IO} = +8mA 2.7V < V_{DD}< 3.6V	-	0.4	
$V_{OH}^{(2)(3)}$	Output high level, when 8 pins output current at the same time		2.4		
$V_{OL}^{(1)(3)}$	Output low level when 8 pins sink current at the same time	I_{IO} = +20mA 2.7V < V_{DD}< 3.6V	-	1.3	
$V_{OH}^{(2)(3)}$	Output high level, when 8 pins output current at the same time		2.4	-	
$V_{OL}^{(1)(3)}$	Output low level when 8 pins sink current at the same time	I_{IO} = +6mA 2V < V_{DD}< 2.7V	-	0.4	
$V_{OH}^{(2)(3)}$	Output high level, when 8 pins output current at the same time		V_{DD}-0.4	-	

1. The current IIO drawn by the chip must always comply with the absolute maximum ratings given in Table 4, and the sum of IIO (all I/O pins and control pins) must not exceed IVSS.

2. The current IIO output by the chip must always comply with the absolute maximum ratings given in Table 4, and the sum of IIO (all I/O pins and control pins) cannot exceed IVDD.

3. Derived from comprehensive evaluation and not tested in production.

Input and output AC characteristics

The definitions and values of the input and output AC characteristics are given in Figure 16 and Table 34 respectively. Unless otherwise stated, the parameters listed are measured using ambient temperature and supply voltage conditions in accordance with Table 6.

Table 34. Input and output AC characteristics (1)

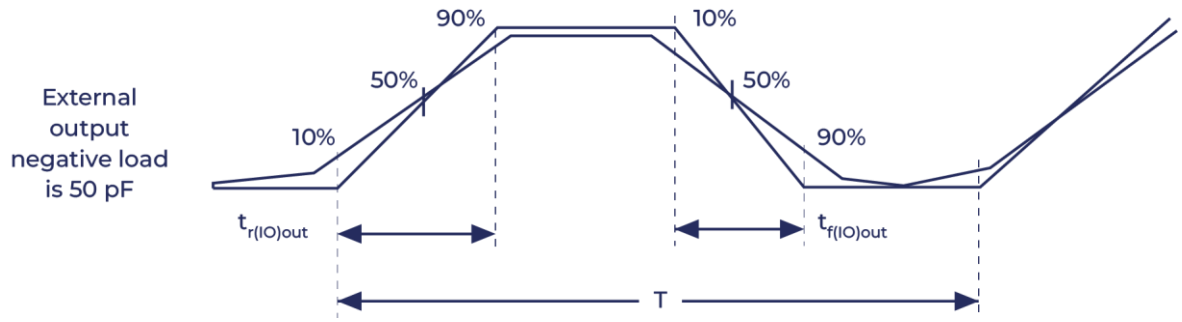
MODEx[1:0]	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD}= 2~3.6V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD}= 2~3.6V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high rise time		-	125(3)	
01 (10MHz)	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD}= 2~3.6V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF,V_{DD}= 2~3.6V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high rise time		-	25(3)	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 30 pF, V_{DD}= 2.7~3.6V	-	50	MHz
			C_L= 50 pF, V_{DD}= 2.7~3.6V	-	30	
			C_L=50 pF, V_{DD}= 2~2.7V	-	20	
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 30 pF, V_{DD}= 2.7~3.6V	-	5(3)	ns
			C_L= 50 pF, V_{DD}= 2.7~3.6V	-	8(3)	
			C_L=50 pF, V_{DD}= 2~2.7V	-	12(3)	
	$t_{r(IO)out}$	Output low to high rise time	C_L= 30 pF, V_{DD}= 2.7~3.6V	-	5(3)	
			C_L= 50 pF, V_{DD}= 2.7~3.6V	-	8(3)	
			C_L=50 pF, V_{DD}= 2~2.7V	-	12(3)	
-	t_{EXTIpw}	The EXTI controller detects the pulse of an external signal. punch width	-	10	-	ns

1. The speed of the I/O port can be configured through MODEx [1:0]. See the TGS32F103xB reference manual for a description of the GPIO port configuration registers.

2. Maximum frequency is defined in Figure 16.

3. Guaranteed by design, not tested in production.

Figure 16. Definition of input and output AC characteristics



5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology and is connected to a pull-up resistor, RPU, that cannot be disconnected (see Table 32). Unless otherwise noted, the parameters listed in Table 35 were measured using ambient temperature and VDD supply voltage conditions consistent with Table 6.

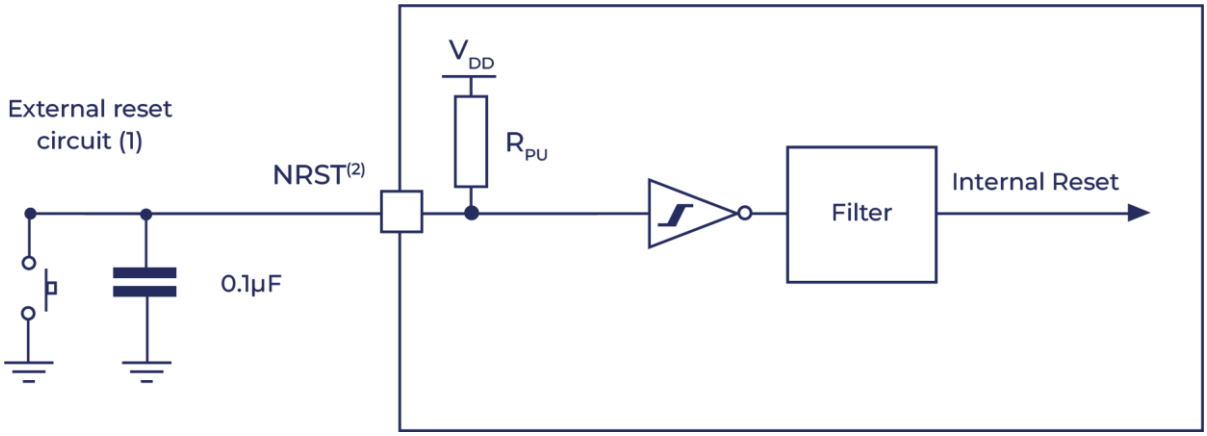
Table 35. NRST pin characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage		-0.5		0.8	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage		2		V_{DD}+0.5	
$V_{hys(NRST)}$ (1)	NRST Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistance(2)	V_{IN}=V_{SS}	30	40	50	kΩ
$V_{F(NRST)}$ (1)	NRST input filter pulse				100	ns
$V_{NF(NRST)}$ (1)	NRST input non-filtered pulse		300			ns

1. Guaranteed by design, not tested in production.

2. The pull-up resistor is designed as a real resistor in series with a switchable PMOS implementation. The resistance of this PMON/NMOS switch is very small (about 10%).

Figure 17. Recommended NRST pin protection



1. The reset network is to prevent spurious resets.

2. The user must ensure that the potential of the NRST pin can be lower than the maximum $V_{IL(NRST)}$ listed in Table 35, otherwise the MCU cannot be reset.

5.3.14 TIM timer characteristics

The parameters listed in Table 36 are guaranteed by design.

For details on the characteristics of input and output multiplexing function pins (output comparison, input capture, external clock, PWM output), see Chapter Section 5.3.12.

Table 36. TIM characteristics

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	13.9	-	ns
f_{EXT}	Timer external clock for CH1 to CH4 frequency		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 72MHz	0	36	MHz
Res_{TIM}	Timer resolution		-	16	bit
$t_{COUNTER}$	When the internal clock is selected, 16-bit counter clock period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count		-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	-	59.6	s

1. TIMx is a common name, representing TIM1~TIM4.

5.3.15 Communication interface

I2C interface features

Unless otherwise stated, the parameters listed in Table 50 and Table 37 are measured using ambient temperature, fPCLK1 frequency and V supply voltage in compliance with the conditions of Table 6.

The I2C interface of the TGS32F103xB standard product complies with the standard I2C communication protocol, but has the following limitations: SDA and SCL are not "true" open-drain pins. When configured as open-drain output, the PMOS tube between the pin and VDD is Closed, but still there.

The I2C interface characteristics are listed in Table 37. For details on the characteristics of the input and output alternate function pins (SDA and SCL), see Section 5.3.12.

Table 37. I2C interface characteristics

Symbol	Parameter	Standard I2C(1)		Fast I2C(1)(2)		Unit
		Maximum value	Minimum value	Maximum value	Minimum value	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{wSCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA establishment time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data retention time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1Cb	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated start condition establishment time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition establishment time	4.0	-	0.6	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	μs
C_b	Capacitive loading of each bus	-	400	-	400	pF

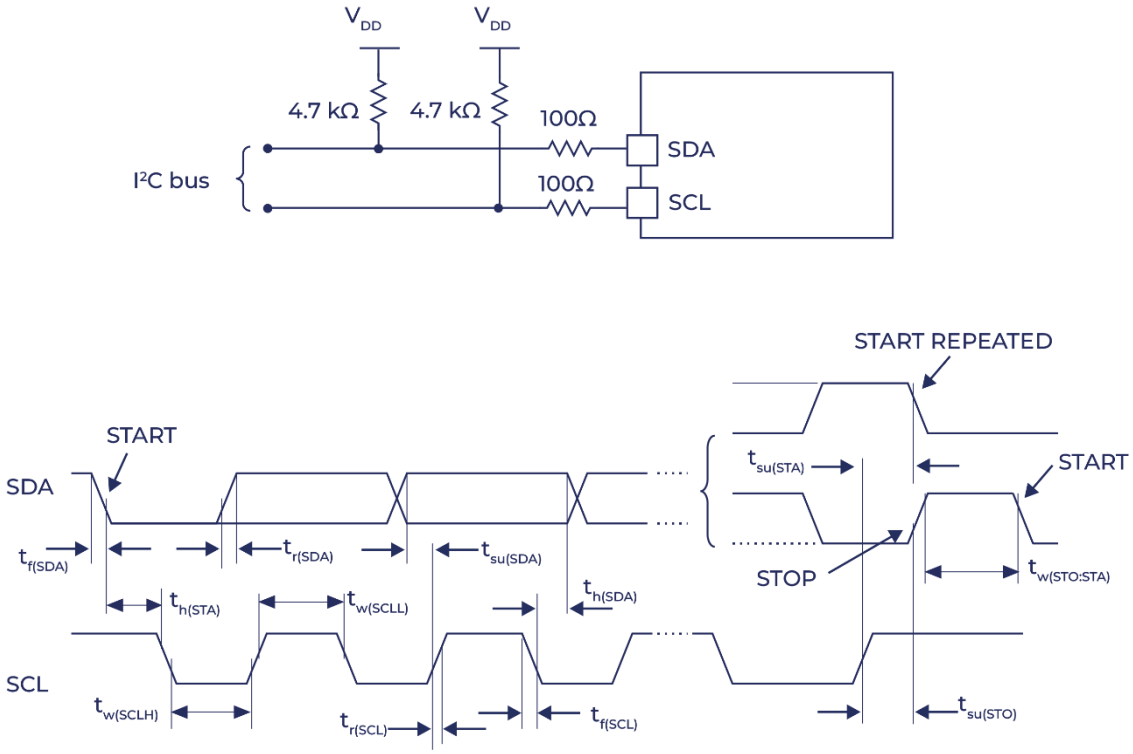
1. Guaranteed by design, not tested in production.

2. To reach the maximum frequency of standard mode I2C, fPCLK1 must be greater than 2 MHz. To reach the maximum frequency of fast mode I2C, fPCLK1 must be greater than 4 MHz.

3. If there is no requirement to extend the low-level time of the SCL signal, then only the maximum holding time of the start condition must be met.

4. In order to cross the undefined area of the SCL falling edge, a hold time of at least 300 ns on the SDA signal must be guaranteed internally in the MCU.

Figure 18. I2C bus AC waveform and measurement waveform



1. The measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 38. SCL frequency (f_{PCLK1} = 36MHz, V_{DD} = 3.3V)[1][2]

$f_{SCL(kHz)}$	I²C_CCR value
	RP=4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. RP=external pull-up resistor, f_{SCL}=I2C speed.

2. For speeds around 200 kHz, the speed error is ±5%. For other speed ranges, the speed error is ±2%. These variations depend on the accuracy of external components in the design.

SPI interface features

Unless otherwise stated, the parameters listed in Table 39 are measured using ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage consistent with the conditions of Table 6.

For details on the characteristics of the input and output alternate function pins (NSS, SCK, MOSI, MISO), see Section 5.3.12.

Table 39. SPI Characteristics(1)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$f_{SCK}1/t_{c(SCK)}$	SPI clock frequency	Main mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall times	Load capacitance: C = 30pF	-	8	ns
Ducy(SCK)	Slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (2)	NSS establishment time	Slave mode	$4t_{PCLCK}$	-	ns
$t_{h(NSS)}$ (2)	NSS hold time	Slave mode	$2t_{PCLCK}$	-	
$t_{w(SCKH)}$ (2) $t_{w(SCKL)}$ (2)	SCK high and low times	Master mode, f_{PCLK} = 36MHz, prescaler coefficient=4	50	60	
$T_{su(MI)}$(2) $T_{su(SI)}$	Data input setup time, master mode	Main mode	5	-	
		Slave mode	5	-	
$T_{h(MI)}$ (2) $T_{h(SI)}$(2)	Data input hold time, main mode	Main mode	5	-	
		Slave mode	4	-	
$T_{a(SO)}$ (2)(3)	Data output access time	Slave mode, f_{PCLK} =20 MHz	0	$3t_{PCLCK}$	
$t_{dis(SO)}$ (2)(4)	Data output prohibition time	Slave mode	2	10	
$t_{v(SO)}$(2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$ (2)(1)	Data output valid time	Master mode (after enable edge)		5	
$T_{h(SO)}$ (2)	Data output hold time	Slave mode (after enable edge)	15	-	
$T_{h(MO)}$ (2)		Master mode (after enable edge)	2	-	

1. The remapped SPI1 characteristics need to be further determined.

2. Derived from comprehensive evaluation and not tested in production.

3. The minimum value indicates the minimum time for driving output, and the maximum value indicates the maximum time for correctly obtaining data.

4. The minimum value indicates the minimum time to turn off the output, and the maximum value indicates the maximum time to put the data line in a high-impedance state.

Figure 19. SPI timing diagram - slave mode and CPHA=0

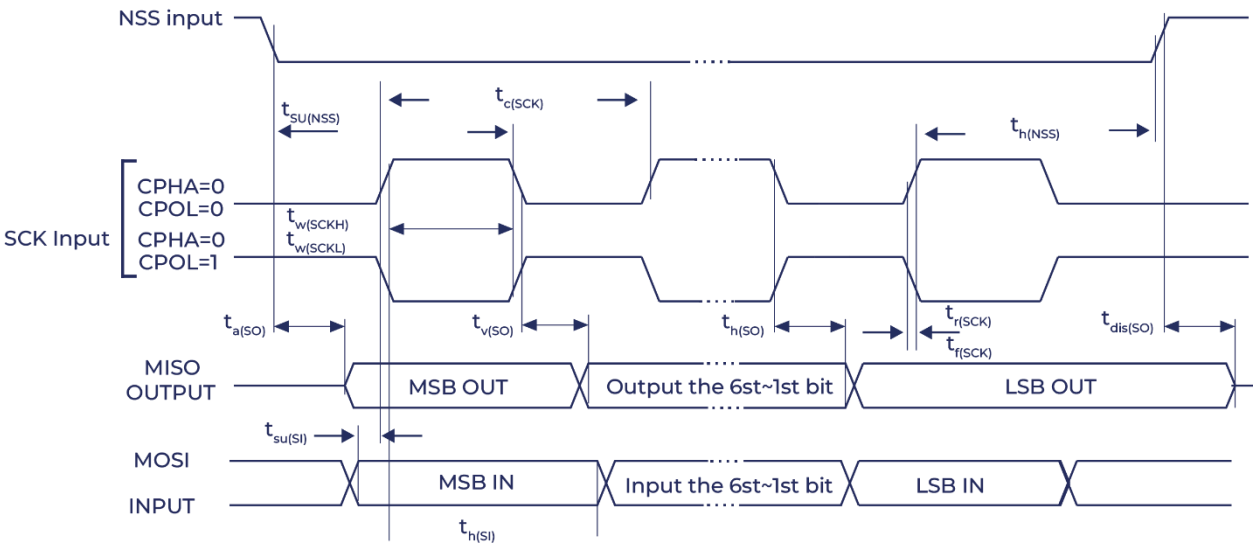
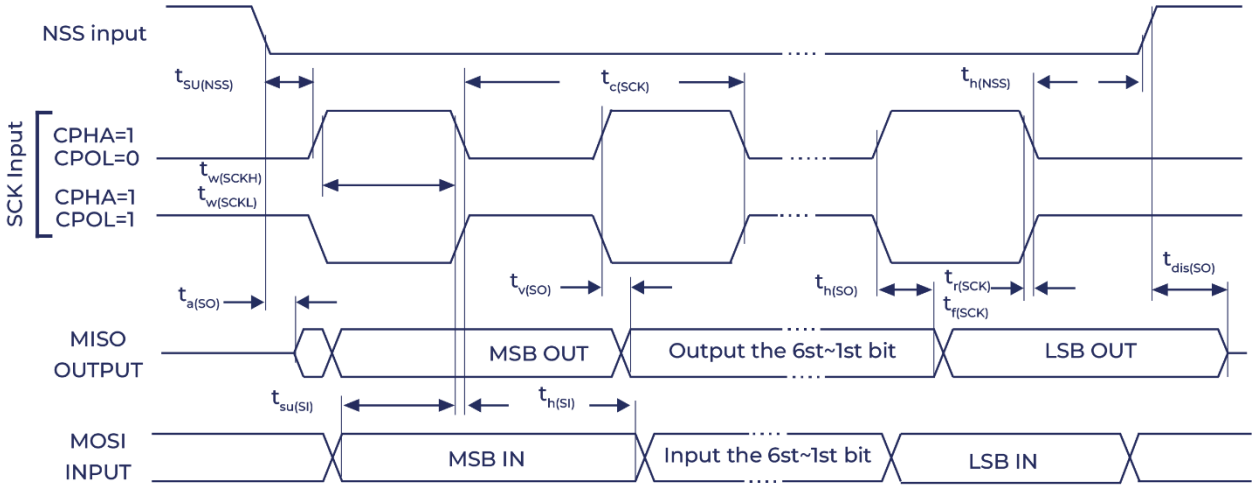
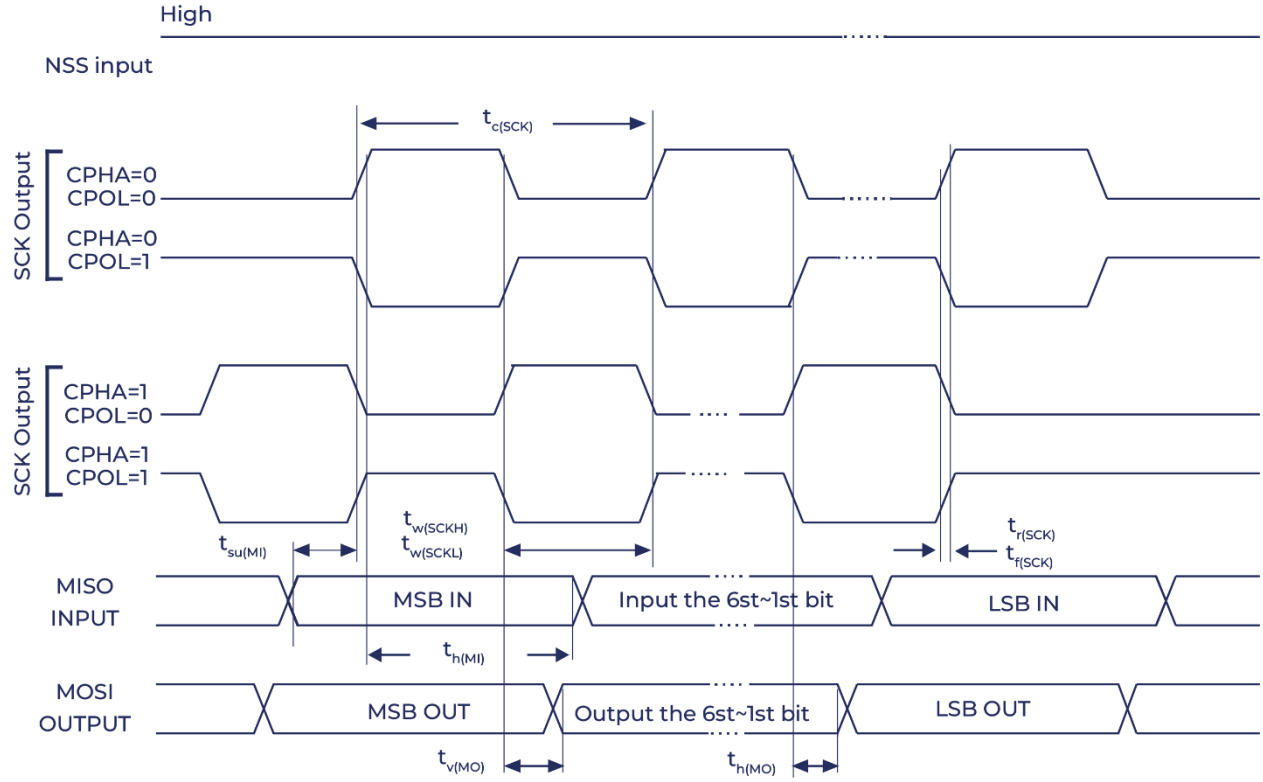


Figure 20. SPI Timing Diagram – Slave Mode and CPHA=1(1)



1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 21. SPI Timing Diagram - Master Mode(1)



1. Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB features

The USB (full speed) interface has passed USB-IF certification.

Table 40. USB boot time

Symbol	Parameter	Maximum value	Unit
$t_{STARTUP}$ (1)	USB transceiver startup time	1	μs

1. Guaranteed by design, not tested in production.

Table 41. USB DC characteristics

Symbol	Parameter	Condition	Minimum(1)	Max(1)	Unit
Input level					
V_{DD}	USB operating voltage(2)		3 0 (3)	3.6	V
V_{DI} (4)	Differential input sensitivity	I(USBDP, USBDM)	0.2	-	V
V_{CM} (4)	Differential common mode range	Contains V_{DI} scope	0.8	2.5	
V_{SE} (4)	Single-ended receiver threshold		1.3	2.0	
Output level					
V_{OL}	Static output low level	1.5kΩ RL to 3.6V(5)	-	0.3	V
V_{OH}	Static output high level	RL of 15kΩ to V_{SS}(5)	2.8	3.6	

1. All voltage measurements are based on the equipment ground wire.

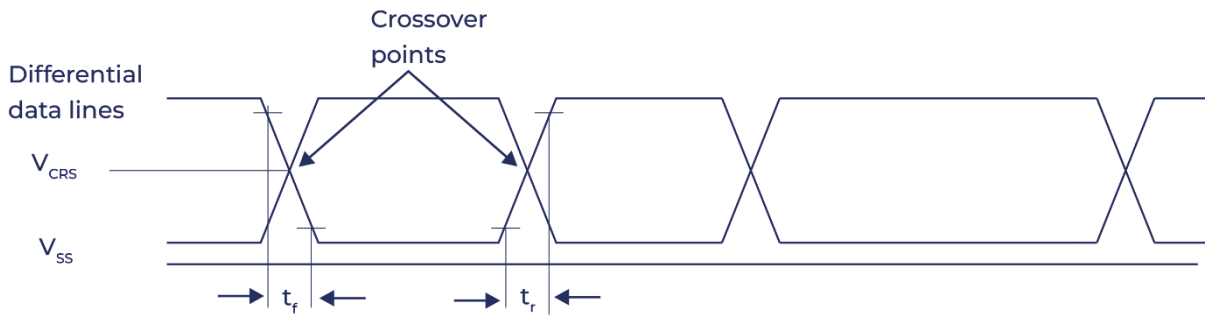
2. In order to be compatible with the USB 2.0 full-speed electrical specification, the USB DP(D+) pin must be connected to the 3.0 ~ 3.6V voltage through a 1.5 kΩ resistor.

3. The correct USB function of TGS32F103xB can be guaranteed at 2.7 V, instead of degrading the electrical characteristics in the 2.7 ~ 3.0 V voltage range.

4. Guaranteed by comprehensive evaluation and not tested in production.

5. RL is the load connected to the USB drive.

Figure 22. USB timing: data signal rise and fall time definition



1. Guaranteed by design, not tested in production.

2. Measure the data signal from 10% to 90%.

Table 42. USB full-speed electrical characteristics (1)

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
t_r	Rise time(2)	$C_L \leq 50$ pF	4	20	ns
t_f	Fall time(2)	$C_L \leq 50$ pF	4	20	ns
t_{rfm}	Rise and fall time matching	t_r / t_f	90	110	%
VCRS	Output signal cross voltage		1.3	2.0	V

5.3.16 CAN (Controller Area Network) interface

For details on the characteristics of the input-output alternate function pins (CAN_TX and CAN_RX), see Section 5.3.12.

5.3.17 12-bit ADC characteristics

Unless otherwise noted, the parameters in Table 43 are measured using ambient temperature, f_{PCLK2} frequency, and V_{DDA} supply voltage consistent with the conditions of Table 6.

Note: It is recommended to perform a calibration at every power-up.

Table 43. ADC Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{DDA}	Supply voltage	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on VREF input pin	-	-	160(1)	220(1)	μA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0(V_{SSA} or V_{REF-} connected to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance		-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance		-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor		-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			μs
			83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion delay	f_{ADC} = 14 MHz	-	-	0.214	μs
			-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Normal trigger conversion delay	f_{ADC} = 14 MHz	-	-	0.143	μs
			-	-	2(4)	$1/f_{ADC}$
t_s(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	μs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power on time		0	0	1	μs
t_{CONV}(2)	Total conversion time (Including sampling time)	f_{ADC} = 14 MHz	1	-	18	μs
			14 ~ 252 (sampling t_S + gradually approaching 12.5)			$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation and not tested in production.

2. Guaranteed by design, not tested in production.

3. In QFN36, LQFP48 and LQFP64 package products, V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to

4. Receive V_{SSA}. See Table 2 for details.

5. For external triggering, a delay of $1/f_{PCLK2}$ must be added to the delays listed in Table 43.

Formula 1: Maximum RAIN formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above equation (Equation 1) is used to determine the maximum external impedance such that the error can be less than 1/4 LSB. Where N = 12 (meaning 12-bit resolution).

Table 44. Maximum R_{AIN} when f_{ADC} = 14 MHz(1)

T_S(period)	t_S(μs)	Maximum R_{AIN}(kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	-
239.5	17.1	-

1. Guaranteed by design, not tested in production.

Table 45. ADC Accuracy – Limited Test Conditions(1)(2)

Symbol	Parameter	Test conditions	Typical value	Max(3)	Unit
ET	Comprehensive error	f_{PCLK2} = 56 MHz f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 ~ 3.6V, T_A= 25 °C Measurements are taken after ADC calibration	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linear error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.

2. Relationship between ADC accuracy and reverse injection current: Injecting reverse current on any standard analog input pin needs to be avoided, as this will significantly reduce the accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to a standard analog pin that may generate reverse injection current.

3. If the injected current is in the forward direction, it will not affect the ADC accuracy as long as it is within the range of IINJ(PIN) and ΣIINJ(PIN) given in Section 5.3.12.

4. Guaranteed by comprehensive evaluation and not tested in production.

Table 46. ADC accuracy(1)(2)(3)

Symbol	Parameter	Test conditions	Typical value	Max(3)	Unit
ET	Comprehensive error	f_{PCLK2} = 56 MHz f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 ~ 3.6 V Measurements are taken after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linear error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.

2. Optimum performance can be achieved within restricted V_{DD}, frequency, V_{REF} and temperature ranges.

3. ADC accuracy versus reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, as this will significantly reduce the accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to a standard analog pin that may generate reverse injection current.

4. If the injection current is in the forward direction, it will not affect the ADC accuracy as long as it is within the range of IINJ(PIN) and ΣIINJ(PIN) given in Section 5.3.12.

5. Guaranteed by comprehensive evaluation and not tested in production.

Figure 23. ADC accuracy characteristics

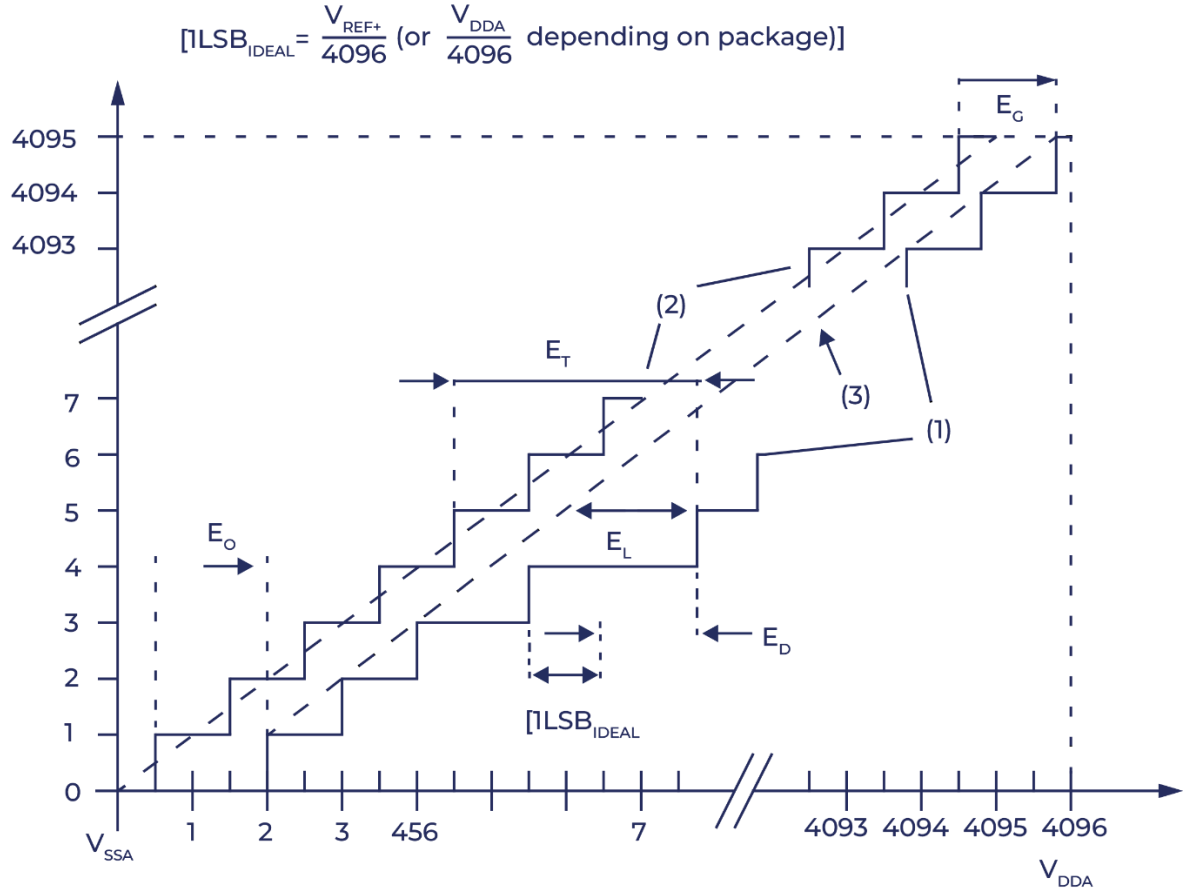
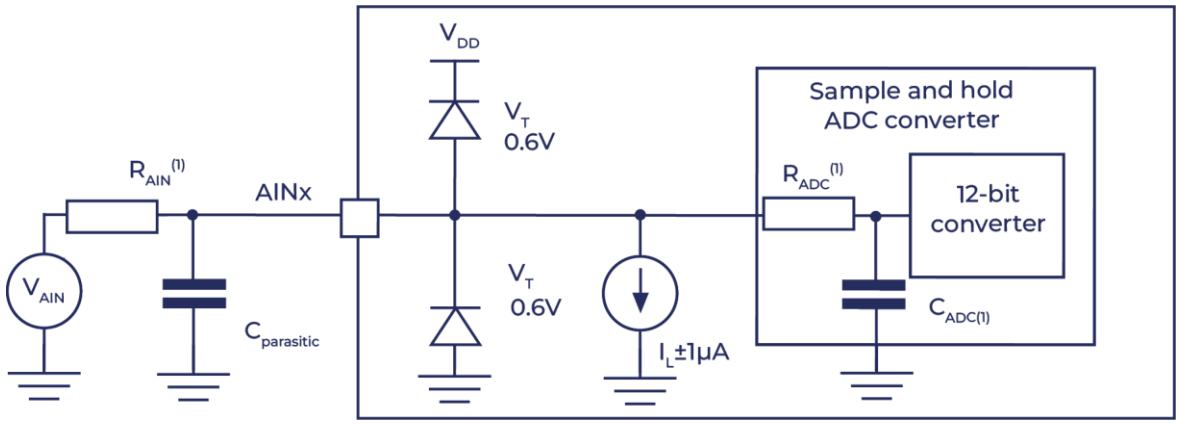


Figure 24. Typical connection diagram using ADC



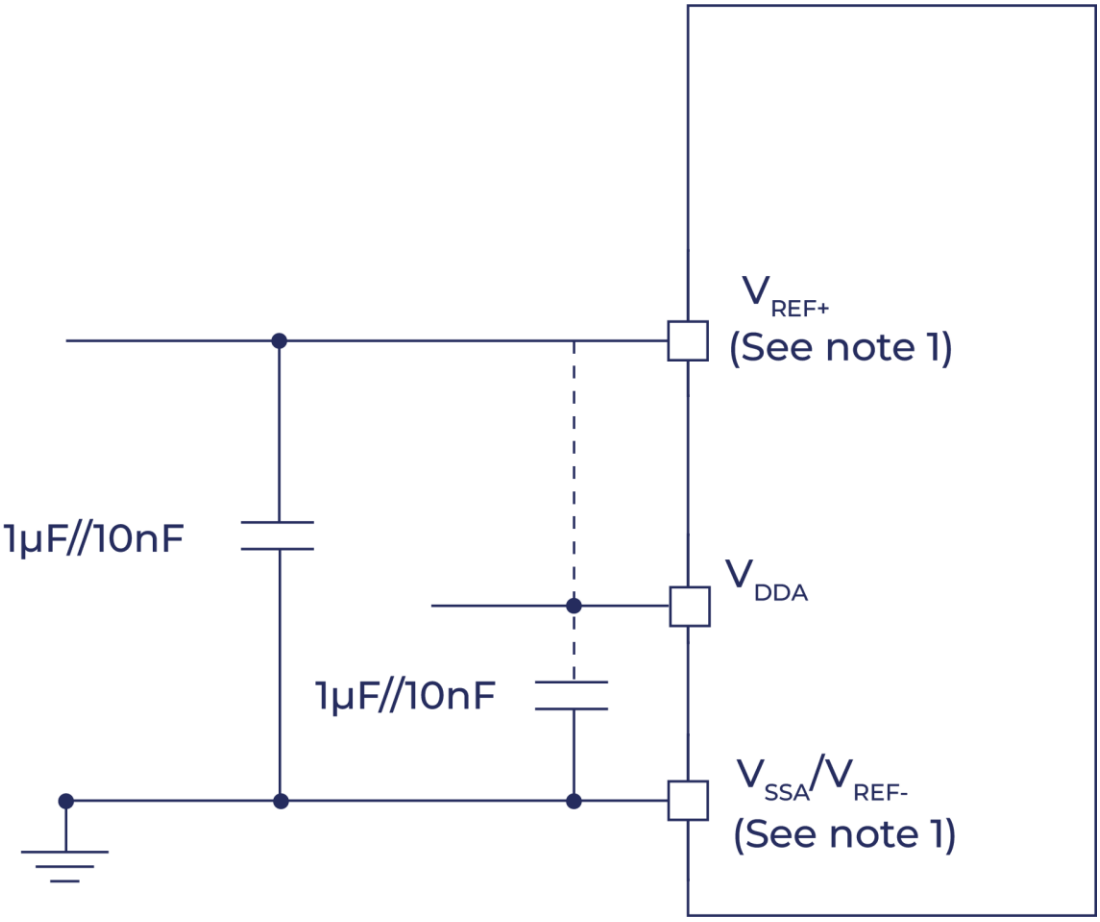
1. See Table 46 for R_{AIN}, R_{ADC}, and C_{ADC} values.

2. Cparasitic represents the parasitic capacitance (about 7pF) on the PCB (related to soldering and PCB layout quality) and pad. Larger Cparasitic values will reduce the accuracy of the conversion, and the solution is to reduce f_{ADC}.

PCB design advice

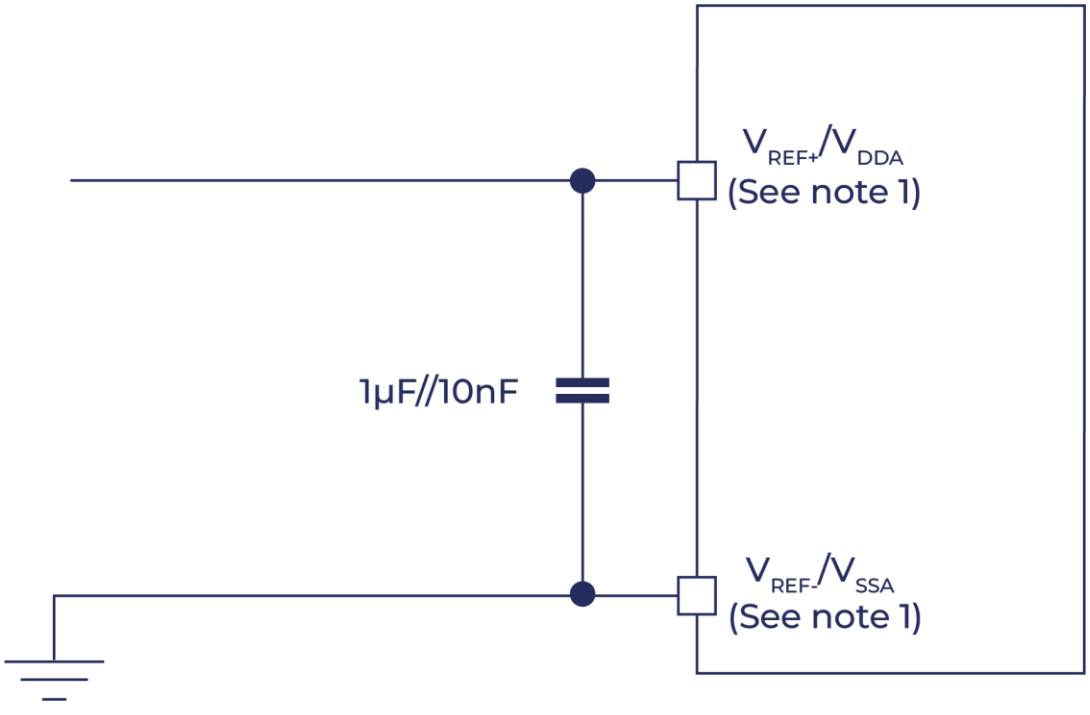
Depending on whether V_{REF+} is connected to V_{DDA}, the decoupling of the power supply must be connected as shown in Figure 25 or Figure 26. The 10nF capacitors in the picture must be ceramic capacitors, and they should be as close to the MCU chip as possible.

Figure 26. Power supply and reference power decoupling circuit (V_{REF+} is not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs only appear on products with more than 100 pins.

Figure 27. Power supply and reference power decoupling circuit (V_{REF+} is connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs only appear on products with pins above 100.

5.3.18 Temperature sensor characteristics

Table 47. Temperature sensor characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
T_L[1]	V_{SENSE} linearity with respect to temperature	-	±1	±2	ºC
AVG slope[1]	Average slope	4.0	4.3	4.6	mV/ºC
V_{25}[1]	Voltage at 25ºC	1.34	1.43	1.52	V
T_{start}[2]	Setup time	4	-	10	µs
T_{s_temp}[2][3]	When reading temperature, ADC sampling time	-	-	17.1	µs

1. Guaranteed by comprehensive evaluation and not tested in production.

2. Guaranteed by design, not tested in production.

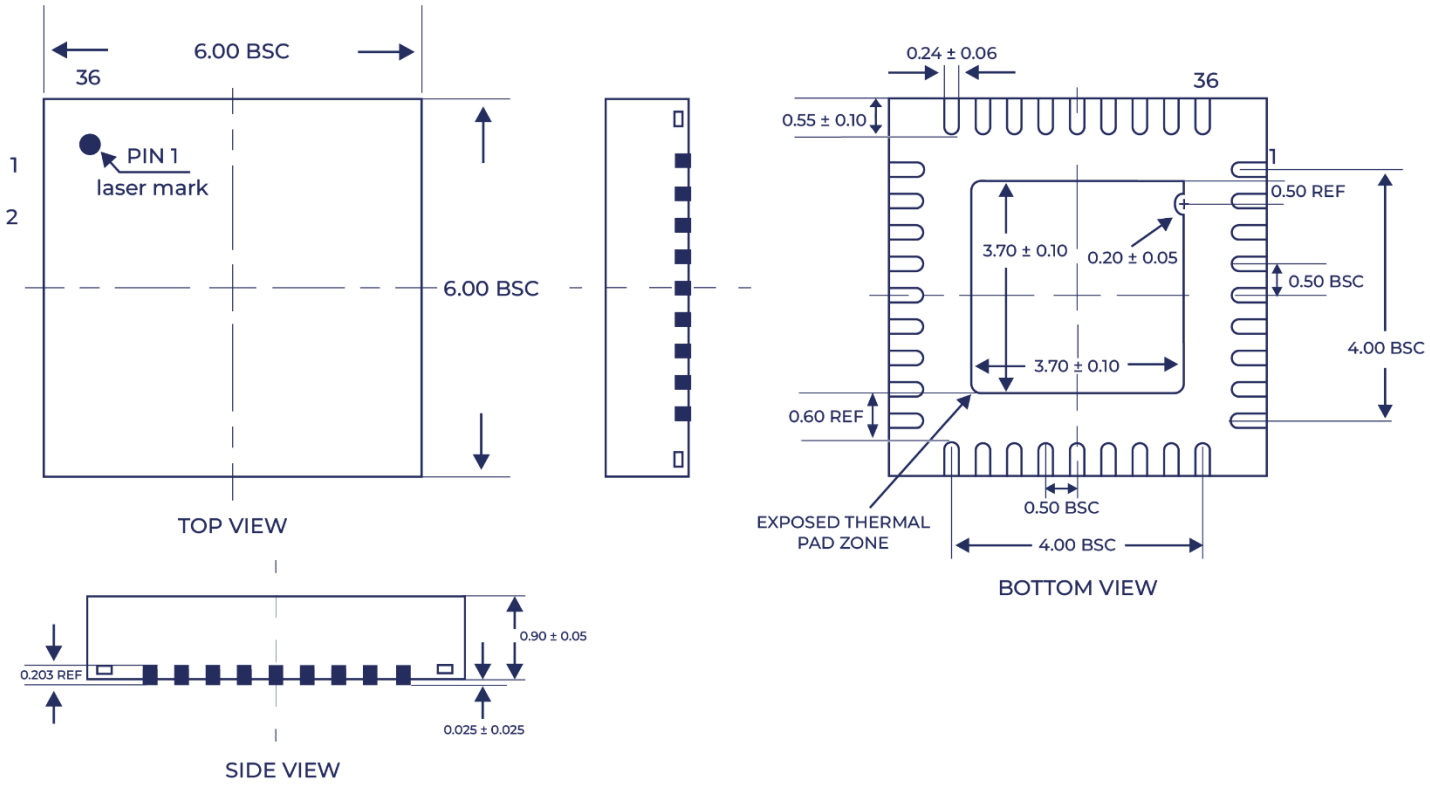
3. The minimum sampling time can be determined by the application through multiple loops.

6. Packaging characteristics

6.1 Packaging mechanical data

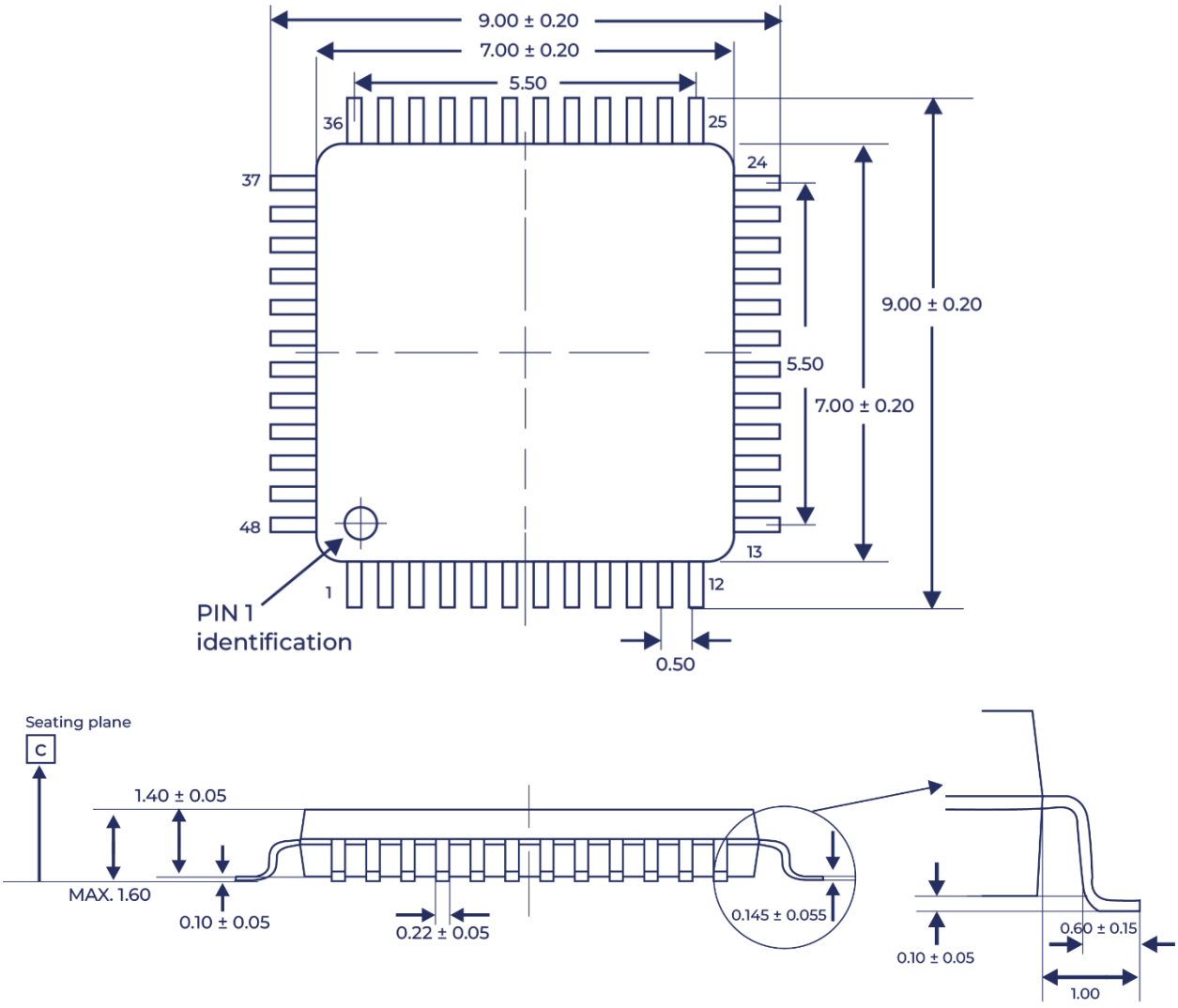
6.1.1 QFN36

Figure 27. QFN36 package diagram



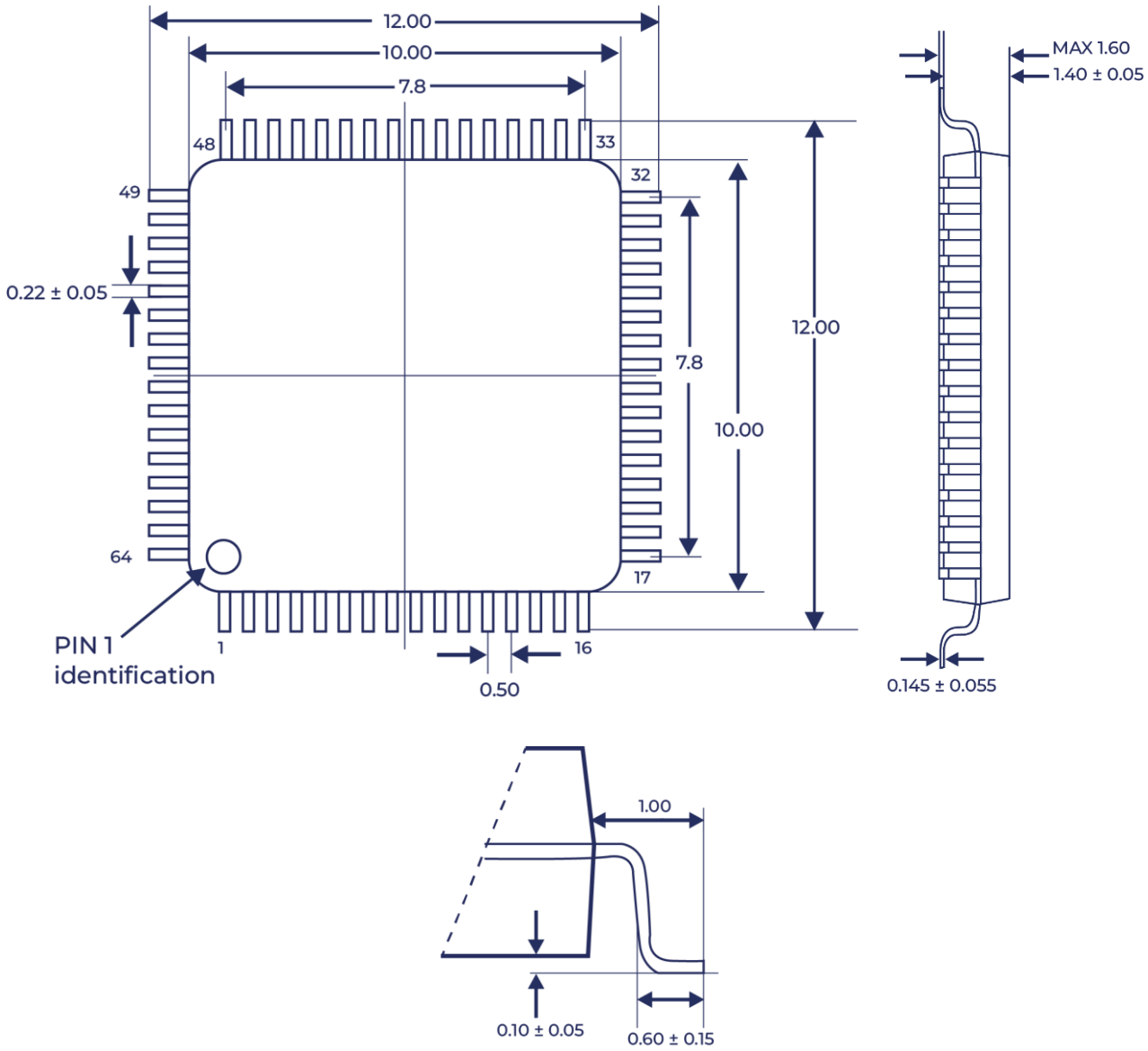
6.1.2 LQFP48

Figure 28. LQFP48, 48-pin low profile square flat package



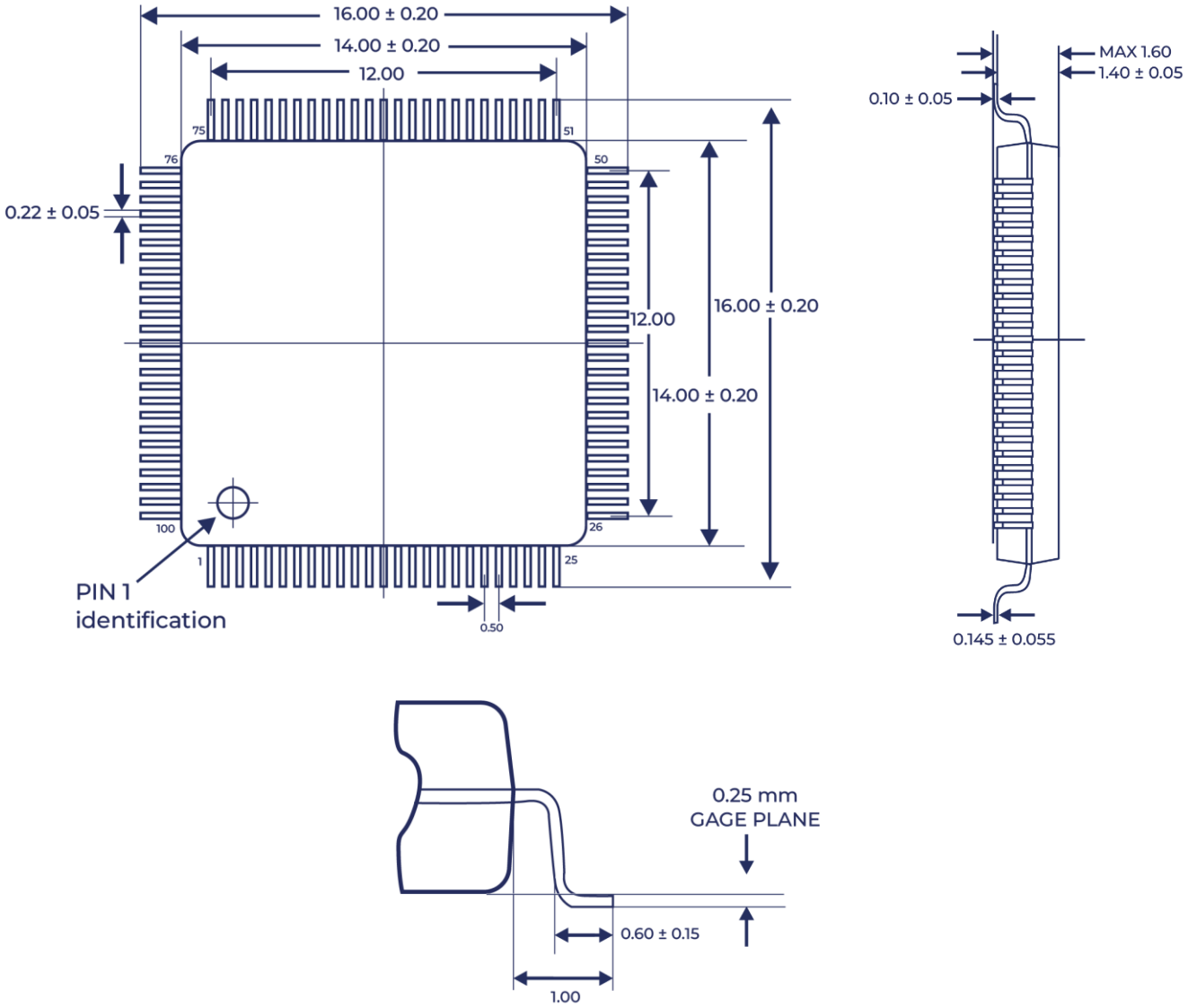
6.1.3 LQFP64

Figure 29. LQFP64, 64-pin low-profile square flat package diagram



6.1.4 LQFP100

Figure 30. LQFP100, 100-pin low-profile square flat package diagram



6.2 Thermal characteristics

The maximum junction temperature (T_{Jmax}) of the chip must not exceed the numerical range given in Table 6.

The maximum junction temperature (T_{Jmax}) of the chip is expressed in degrees Celsius and can be calculated by the following formula:

$$T_Jmax = T_Amax + (P_Dmax \times \Theta_{JA})$$

in:

• T_{Amax} is the maximum ambient temperature in °C,

• ΘJA is the junction-to-ambient thermal impedance of the package, expressed in °C/W,

• P_{Dmax} is the sum of P_{INTmax} and PI/Omax ($P_{Dmax} = P_{INTmax}$ + PI/Omax),

• P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts, and is the maximum internal power consumption of the chip.

PI/Omax is the maximum power consumption of all output pins:

$$PI/Omax = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$$

Consider the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} for low and high levels on the I/Os in the application.

Table 52. Package Thermal Characteristics

Symbol	Parameter	Numerical value	Unit
ΘJA	Junction to ambient thermal impedance – LQFP100 – 14×14mm/0.5mm pitch	46	°C/ W
	Junction to ambient thermal impedance – LQFP64 – 10×10mm/0.5mm pitch	45	
	Junction to ambient thermal impedance – LQFP48 – 7×7mm/0.5mm pitch	55	
	Junction to ambient thermal impedance - QFN36-6×6mm/0.5mm pitch	18	

7. Model naming

TGS32	F	407	R	B	T	7
Device family: TGS32 - ARM-base 32-bit microcontroller	**Product type: F - General purpose**	**Sub family 103 - TGS32F103**	**Pin count: V - 100 pins R - 64 pins C - 48 pins K - 36 pins**	**User code memory size: B - 128 Kbytes**	**Package: T - LQFP U - QFN**	**Temperature range: 7 - Temperature range, -40 to 105 °C**

8. Order model

Model	Encapsulation	Number of pins	Working temperature
TGS32F103KBU7	QFN	36	-45℃~ +105℃
TGS32F103CBT7	LQFP	48	-45℃~ +105℃
TGS32F103RBT7	LQFP	64	-45℃~ +105℃
TGS32F103VBT7	LQFP	100	-45℃~ +105℃