TGS2S80

Resolver-to-Digital Converter

Data sheet

Features

- 10/12/14/16 bit resolution is set by the user
- Low power consumption: 600 mW (typical value)
- Dynamic performance can be set by the user
- High tracking rate: 1040 rps (10 bits, maximum value)
- Provide speed output signal Level 2 ESD protection (2,000 V, minimum)
- The operating temperature range can reach -55°C ~ +125°C

Overview

The TGS2S80 is a monolithic, 10/12/14/16-bit Resolver-to-Digital Converter (RDC), available in 44-pin CLCC. This converter allows the user to select the desired resolution and dynamic performance via external components, offering significant flexibility to tailor the converter to specific system requirements. With this converter, the user can select a resolution of 10, 12, 14, or 16 bits; when set to 10-bit resolution, it can track resolver signals at speeds up to 1040 revolutions per second (62,400 rpm). The converter is designed and manufactured to meet the requirements for Grade B circuits per GJB597 "General Specification for Semiconductor Integrated Circuits", with an operating temperature range of -55°C to +125°C.
Benchmarked against Analog Devices AD2S80A

Application area

Radar antenna position monitoring, navigation system, fire control system, servo system and robot and other fields.

Rated conditions and recommended working conditions

Absolute maximum rating	Positive power supply voltage ($+V_S$): 14 V
	Negative power supply voltage ($-V_S$): -14 V
	Logic supply voltage (V_L):
	Digital signal input: -0.4 V ~ V_L
	Analog input voltage (V_{COS}, V_{SIN} and V_{REF}): $-V_S$ ~ $+V_S$
	Signal and reference phase shift (PS): -10°C ~ +10°C
	Storage temperature range (T_P): -65°C ~ 150°C
	Lead soldering temperature (T_M): 300°C (10s)
Recommended working conditions	Positive power supply voltage ($+V_S$): 10.8 V ~ 13.2 V
	Negative power supply voltage ($-V_S$): -13.2 V ~ -10.8 V
	Logic power supply voltage (V_L): 4.5 V ~ 5.5 V

	Signal input voltage (V_{COS} and V_{SIN}): 1.8 V (RMS) ~ 2.2 V (RMS)
	Reference input voltage (V_{REF}): 1 V (V_{PK}) ~ 8 V (V_{PK})
	Operating frequency (f_{IN}): 50 Hz ~ 20 kHz
	Operating temperature range (T_C): -55°C ~ 125°C

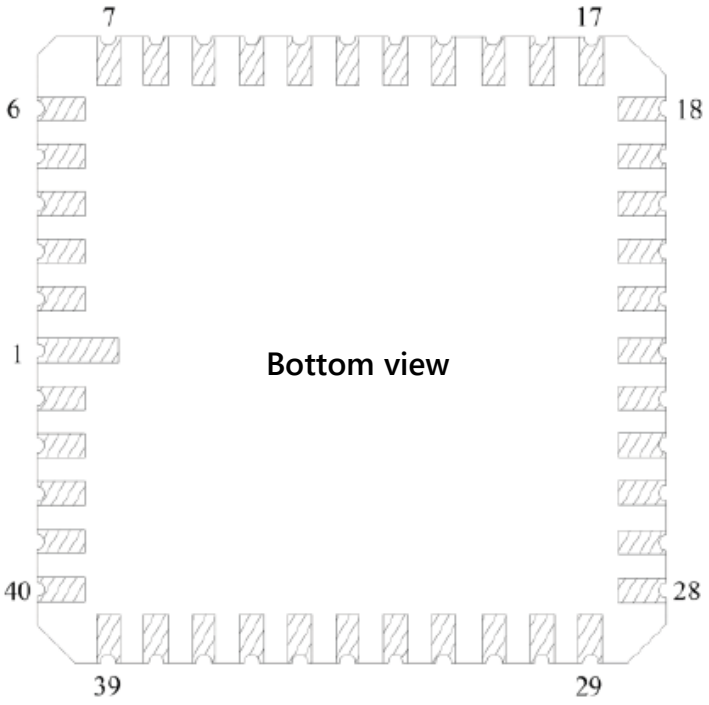
Performance indicators

Parameter	Condition	Min.	Typ.	Max.	Unit
Signal input					
Frequency		50		20.000	Hz
Level		1.8	2.0	2.2	Vrms
Maximum voltage				8.0	V_{PK}
Reference input					
Frequency		50		20.000	Hz
Level		1.0		8.0	V_{PK}
Dynamic parameters					
Repeatability				1	LSB
Allowable phase shift	Phase difference between reference	-10		+10	°
Tracking rate	10 bits			1040	rps
	12 bits			260	rps
	14 bits			65	rps
	16 bits			16.25	rps
Accuracy					
Angular accuracy	K			±(4+1)LSB	arc min
	L			±(2+1)LSB	arc min
Speed signal					
Linearity	Full scale range			±3	%FSD
Reverse error				±7	%FSD
Zero voltage				6	mV
Full scale voltage	1 mA load, maximum tracking rate.	±8		±10.5	V
$\overline{\text{INHIBIT}}$	Output data refresh is prohibited when the logic is low				
The time it takes for the data to reach stability				600	ns
$\overline{\text{ENABLE}}$	Logic low enable position output, logic high the output is in a high impedance state				
$\overline{\text{ENABLE}}$ time		35		110	ns
BYTE SELECT	When logic is high, pin DB1-DB8 output the data is 8 bits high, and the logic pin is low the output data of DB1-DB8 is the lower 8 bits.				
Time required to provide data		60		140	ns
Resolution control	Internal pull-up (100k Ω) to $+V_S$				
SC1 SC2					
0 0	10 bits				
0 1	12 bits				
1 0	14 bits				
1 1	16 bits				

DATA LOAD	Internal pull-up (100k Ω) to $+V_S$. Allow data from the data line when the logic is low, load the internal counter of the chip			
BUSY Width		200	600	ns
Digital input High voltage V_{IH} Low voltage V_{IL}	Disable, enable, byte selection	 2.0	 0.8	 V V
Digital output High voltage V_{OH} Low voltage V_{OL}	Zero crossing, direction, DB1-DB16 I_{OH} = 100 μA I_{OL} = 1.2 mA	 2.4	 0.4	 V V
Power supply Voltage $+V_S$ $-V_S$ $+V_L$ Current $\pm I_S$ I_L	 $\pm V_S$ = ± 12 V V_L = 5 V	 + 10.8 - 10.8 + 5 	 ± 24 1.0	 V V V mA mA
Temperature Operating temperature Storage temperature		 -55 -65	 125 150	 °C °C
Physical properties Specification: 44CLCC Weight: 44CLCC		 16.8 x 16.8 x 3.1 1.8	 2.0	 mm^3 g
Quality level		GJB597 Class B		-

Pin definition

Ceramic seal 44CLCC package pin definition:

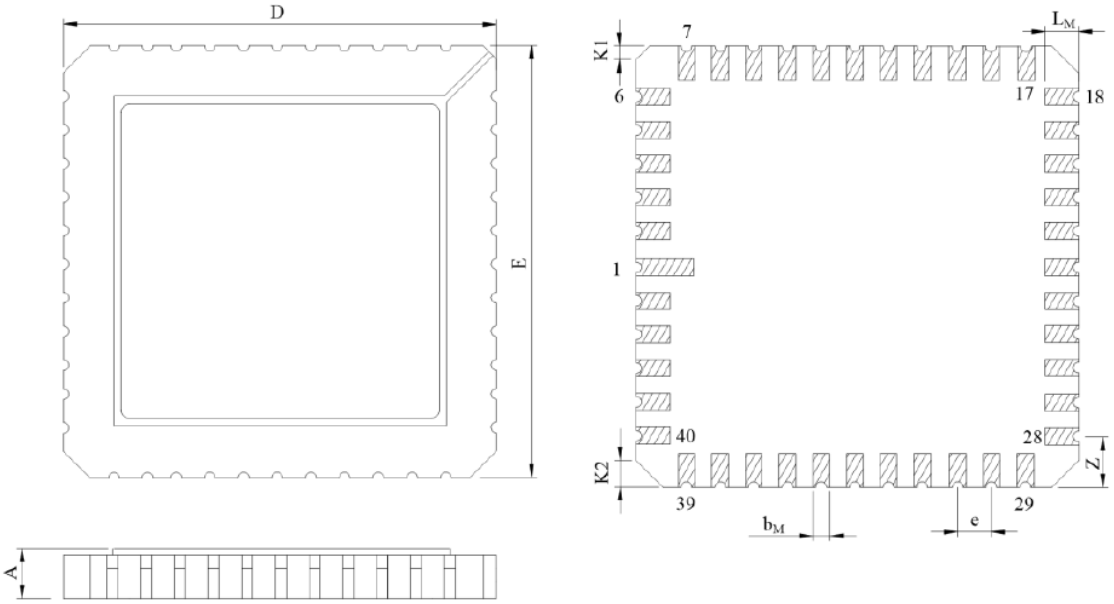


Serial Number	Symbol	Function	Serial Number	Symbol	Function
1	REFERENCE I/P	Reference signal input	23	DB14	Weight 0.021° digital angle output terminal
2	DEMOD I/P	Phase sensitive demodulation input	24	DB15	Weight 0.010° digital angle output terminal
3	AC ERROR O/P	AC error signal output terminal	25	DB16 LSB	Weight 0.005° digital angle output terminal
4	COS	Cosine signal input terminal	26	V_L	+5 V power supply
5	ANALOG GND	Simulated ground	27	$\overline{\text{ENABLE}}$	Enable signal input
6	SIGNAL GND	Signal ground	28	BYTE SELECT	Byte selection signal input terminal
7	SIN	Sinusoidal signal input terminal	29	NC	No connect
8	$+V_S$	+12 V power supply	30	$\overline{\text{INHIBIT}}$	Disable signal input terminal
9	NC	No connect	31	DIGITAL GND	Digital ground
10	DB1 MSB	Weight 180.000° digital angle output terminal	32	SC1	Resolution control high input terminal
11	DB2	Weight 90.000° digital angle output terminal	33	SC2	Resolution control low input terminal
12	DB3	Weight 45.000° digital angle output terminal	34	NC	No connect
13	DB4	Weight 22.500° digital angle output terminal	35	DATA LOAD	Data loading signal input terminal
14	DB5	Weight 11.250° digital angle output terminal	36	BUSY	Busy signal output
15	DB6	Weight 5.625° digital angle output terminal	37	DIRECTION	Direction signal output terminal
16	DB7	Weight 2.812° digital angle output terminal	38	RIPPLE CLOCK	Zero crossing signal output terminal
17	DB8	Weight 1.406° digital angle output terminal	39	$-V_S$	-12 V power supply
18	DB9	Weight 0.703° digital angle output terminal	40	VCO I/P	Voltage controlled oscillator input
19	DB10	Weight 0.351° digital angle output terminal	41	NC	No connect

20	DB11	Weight 0.175° digital angle output terminal	42	INTEGRATOR I/P	Integrator input
21	DB12	Weight 0.087° digital angle output terminal	43	INTEGRATOR O/P	Integrator output
22	DB13	Weight 0.043° digital angle output terminal	44	DEMOD O/P	Phase sensitive demodulator output

Package size (unit, mm)

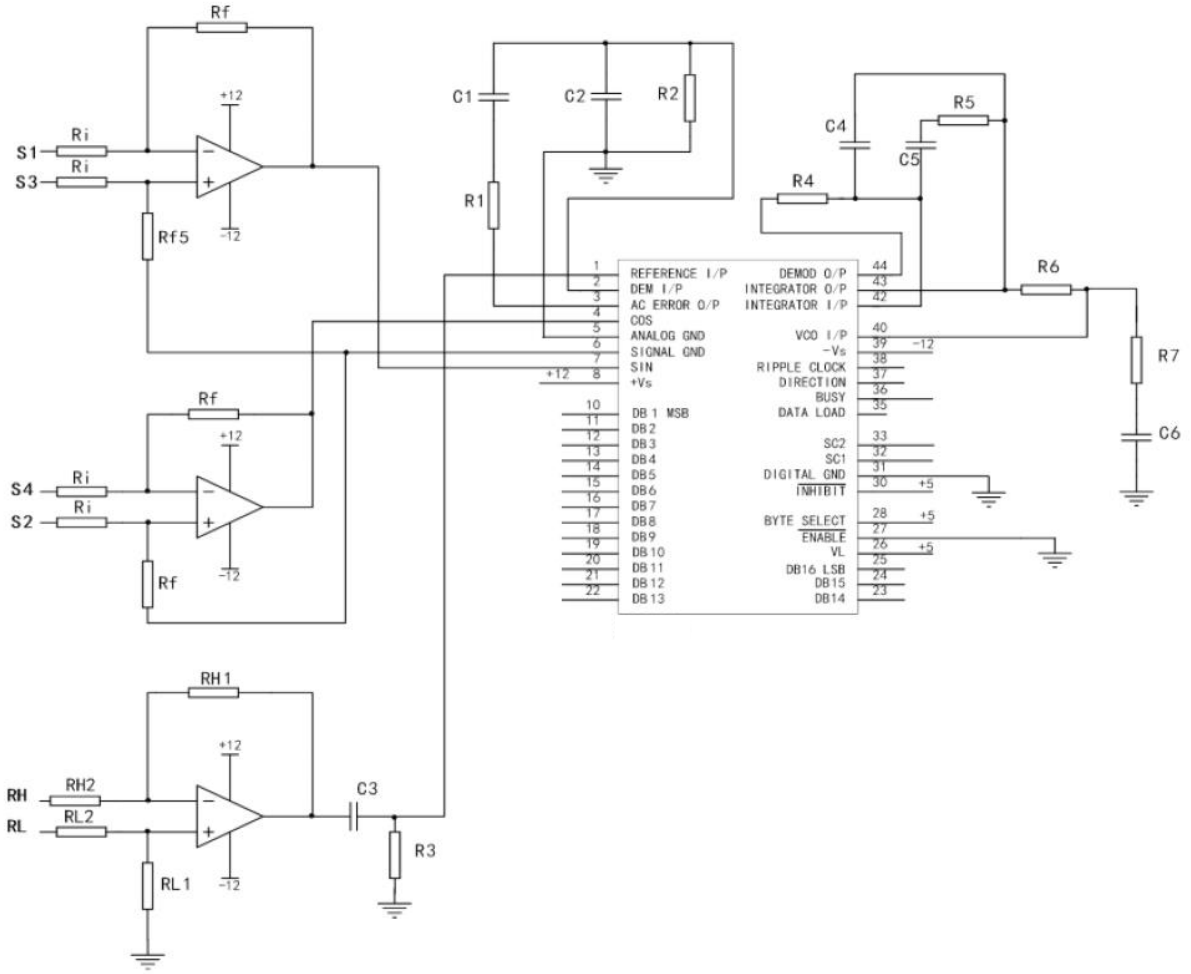
The shape of the ceramic seal 44CLCC package TGS2S80 is shown in the figure below, in mm.



Size symbol	Value		
	Min.	Typ.	Max.
A	1.63	-	3.05
b_M	0.56	-	0.71
D (E)	-	-	16.81
e	-	1.27	-
K_1	-	-	0.63
K_2	0.77	-	-
L_M	1.07	-	1.47
Z	1.65	1.91	2.16

Typical application diagram

The converter is easy to use, and its typical application connection diagram is shown in the figure below. It is recommended to use the ANALOG GND of the power cord $+V_S$, $-V_S$, and the spitting neighbor converter. The recommended values are 100 nF (ceramic capacitor) and 10 pF (ceramic capacitor). In addition, the DIGITAL GND of the $+V_L$ and spitting converter should also be, connect 100 nF (ceramic capacitor) and 10 pF (ceramic capacitor) between them.



Note:

1. Precision resistors should be used for Ri and Rf, with relative accuracy < 0.05%, temperature drift < 10ppm, the power should meet the requirements of the input signal voltage.
2. If the resolver signal voltage is Vi, the ratio of Ri to Rf is Ri/Rf = Vi/2. Examples for 11.8V and 90V:
   At 11.8 V input, Ri = 70.8 kΩ, Rf = 12 kΩ
   At 90 V input, Ri = 270 kΩ, Rf = 6 kΩ
3. When designing the PCB layout, to avoid signal interference, the grounds of S1, S2, S3, S4 should be connected individually to SIGNAL GND (Pin 6), and the grounds of RH, RL should be connected individually to ANALOG GND (Pin 5). Importantly, SIGNAL GND and ANALOG GND are interconnected internally within the chip and should not be connected externally

Product selection guide

Product model specification	Conversion accuracy	Quality grade	Standard	Package form
TGS2S80	± (4 arc min + 1LSB)	B	GJB597	44CLCC