TGS1567, TGS1568

Bus transceiver

Data sheet

General Description

The TGS1567 and TGS1568 are low power CMOS dual transceivers designed to meet the requirements of MIL-STD-1553 and MIL-STD-1760 specifications.

The transmitter section of each bus takes complementary CMOS/TTL Manchester II bi-phase data and converts it to differential voltages suitable for driving the bus isolation transformer. Separate transmitter inhibit control signals are provided for each transmitter.

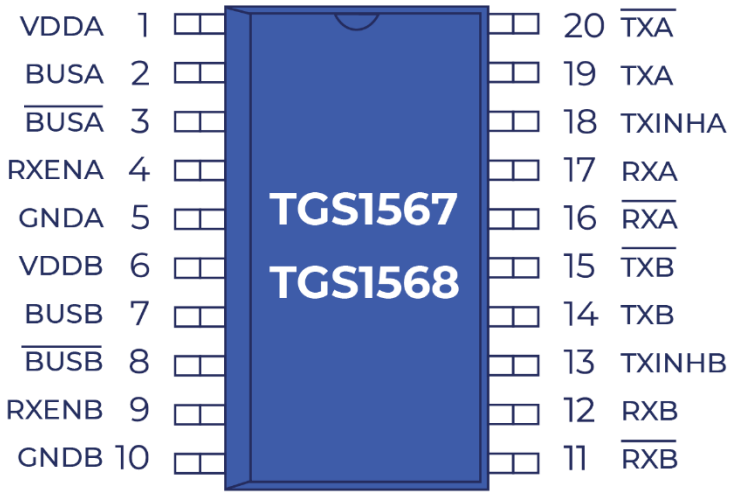
The receiver section of each bus converts the 1553 bus biphasedata to complementary CMOS / TTL data suitable for input to a Manchester decoder. Each receiver has a separate enable input which can be used to force the output of the receiver to a logic 0 (TGS1567) or logic 1 (TGS1568).

To minimize the package size for this function, the transmitter outputs are internally connected to the receiver inputs, so that only two pins are required for connection to each coupling transformer.

Features

- Compliant to MIL-STD-1553A and B, MIL-STD-1760 ARINC 708A
- Power supply voltage range 5.0 V ± 5%
- CMOS technology for low standby Power、
- Less than 1.0 W maximum power
- Industrial and extended temperature ranges

Pin Configuration



Pin Plastic ESOP - 20

Pin Description

Pin	Symbol	Function	Description
1	VDDA	Power Supply	+5 V power for transceiver A
2	BUSA	Analog	MIL-STD-1533 bus driver A, positive signal
3	$\overline{\text{BUSA}}$	Analog	MIL-STD-1553 bus driver A, negative signal
4	RXENA	Digital Input	Receiver A enable. If low, forces RXA and $\overline{\text{RXA}}$ low (TGS1567) or High (TGS1568)
5	GNDA	Power Supply	Ground for transceiver A
6	VDDB	Power Supply	+5 V power for transceiver B
7	BUSB	Analog	MIL-STD-1533 bus driver B, positive signal
8	$\overline{\text{BUSB}}$	Analog	MIL-STD-1553 bus driver B, negative signal
9	RXENB	Digital Input	Receiver B enable. If low, forces RXB and $\overline{\text{RXB}}$ low (TGS1567) or High (TGS1568)
10	GNDB	Power Supply	Ground for transceiver B
11	$\overline{\text{RXB}}$	Digital Output	Receiver B output, inverted
12	RXB	Digital Output	Receiver B output, non-inverted
13	TXINHB	Digital Input	Transmit inhibit, bus B. If high BUSB, $\overline{\text{BUSB}}$ disabled
14	TXB	Digital Input	Transmitter B digital data input, non-inverted
15	$\overline{\text{TXB}}$	Digital Input	Transmitter B digital data input, inverted
16	$\overline{\text{RXA}}$	Digital Output	Receiver A output, inverted
17	RXA	Digital Output	Receiver A output, non-inverted
18	TXINHA	Digital Input	Transmit inhibit, bus A. If high BUSA, $\overline{\text{BUSA}}$ disabled
19	TXA	Digital Input	Transmitter A digital data input, non-inverted
20	$\overline{\text{TXA}}$	Digital Input	Transmitter A digital data input, inverted

Ordering Information

Type Number	Package Name	Package Quantity	Operating Temperature
TGS1567ESN1	ESOP-20	100	-40℃ to +125℃
TGS1568ESN1	ESOP-20	100	-40℃ to +125℃

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply voltage (VDD)	-0.3	7	V
Logic input voltage range	-0.3	5.5	V
Receiver differential voltage	50		Vp-p
Driver peak output current	+1.0 A		A
Operating Temperature Range	-40°C	125	°C
Solder Reflow Temperature		260	°C
Junction Temperature		175	°C
Storage Temperature	-65°C	150	°C

DC Electrical Characteristics

VDD = 5.0 V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating Voltage	VDD		4.75	5.0	5.25	V
Total Supply Current	ICC1	Not Transmitting		14	22	mA
	ICC2	Transmit one bus @50% duty cycle		200	330	mA
	ICC3	Transmit one bus @100% duty cycle		420	550	mA
Power Dissipation	PD1	Not Transmitting		0.10	0.120	W
	PD2	Transmit one bus @100% duty cycle		0.75	0.95	W
Min. Input Voltage (HI)	V_{IH}	Digital inputs	2.0	1.4		V
Max. Input Voltage (LO)	V_{IL}	Digital inputs		1.4	0.8	V
Min. Input Current (HI)	I_{IH}	Digital inputs			20	µA
Max. Input Current (LO)	I_{IL}	Digital inputs	-20			µA
Min. Output Voltage (HI)	V_{OH}	I_{OUT} = -0.4 mA, Digital outputs	2.7			V
Max. Output Voltage (LO)	V_{OL}	I_{OUT} = 4.0 mA, Digital outputs			0.4	V
RECEIVER (Measured at Point “AD“ in Figure 3 unless otherwise specified)						
Input resistance	R_{IN}	Differential (at chip pins)	20			kOhm
Input capacitance	C_{IN}	Differential			5	pF
Common mode rejection ratio	CMRR		40			dB
Input common mode voltage	V_{ICM}		-10.0		10.0	V-pk
Threshold Voltage - Direct-coupled Detect	V_{THD}	1 MHz Sine Wave Measured at Point “AD” in Figure 3 RXA/B, $\overline{RXA/B}$, pulse width > 70 ns	1.15			Vp-p
Threshold Voltage - Direct-coupled No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.28	Vp-p
Threshold Voltage - Transformer-coupled Detect	V_{THD}	1 MHz Sine Wave Measured at Point “AD” in Figure 4 RXA/B, $\overline{RXA/B}$, pulse width > 70 ns	0.86			Vp-p
Threshold Voltage - Transformer-coupled No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$			0.20	Vp-p

VDD = 5.0 V, GND = 0 V, TA = Operating Temperature Range (unless otherwise specified).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
TRANSMITTER (Measured at Point "AD" in Figure 3 unless otherwise specified)						
Output Voltage Direct coupled	V_{OUT}	35 Ohm load (Measured at Point "AD" in Figure 3)	6.5		9.0	Vp-p
Output Voltage Transformer coupled	V_{OUT}	70 Ohm load (Measured at Point "AT" in Figure 4)	20.0		27.0	Vp-p
Output Noise	V_{ON}	Differential, inhibited			10.0	mVp-p
Output Dynamic Offset Voltage Direct coupled	V_{DYN}	35 Ohm load (Measured at Point "AD" in Figure 3)	-90		90	mV
Output Dynamic Offset Voltage Transformer coupled	V_{DYN}	70 Ohm load (Measured at Point "AT" in Figure 4)	-250		250	mV
Output resistance	R_{OUT}	Differential, not transmitting	10			kOhm
Output Capacitance	C_{OUT}	1 MHz sine wave			15	pF

AC Electrical Characteristics

VDD = 5.0 V, GND = 0 V, TA = Operating Temperature Range (unless otherwise specified).

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
RECEIVER (Measured at Point "AT" in Figure 4)						
Receiver Delay	t_{DR}	From input zero crossing to RXA/B or $\overline{RXA/B}$			500 Note 3	ns
Receiver gap time	t_{RG}	Spacing between RXA/B and $\overline{RXA/B}$ pulses	60 Note 1		380 Note 2	ns
Receiver Enable Delay	t_{REN}	From RXENA/B rising or falling edge to RXA/B or $\overline{RXA/B}$			40	ns
TRANSMITTER (Measured at Point "A_D" in Figure 3)						
Driver Delay	t_{DT}	TXA/B, $\overline{TXA/B}$ to BUSA/B, $\overline{BUSA/B}$,			150	ns
Rise time	t_r	35 Ohm load	100		300	ns
Fall Time	t_f	35 Ohm load	100		300	ns
Inhibit Delay	t_{DI-H}	Inhibited output			100	ns
	t_{DI-L}	Active output			150	ns

Note 1. Measured using a 1 MHz sinusoid, 20 V peak to peak, line to line at point "AT" (Guaranteed but not tested).

Note 2. Measured using a 1 MHz sinusoid, 860 mV peak to peak, line to line at point "AT" (100% tested).

Note 3. Measured using a 1 MHz sinusoid, 860 mV peak to peak, line to line at point "AT". Measured from input zero crossing point.

Functional Description

The TGS1567 family of data bus transceivers contain differential voltage source drivers and differential receivers. They are intended for applications using a MIL-STD-1553 A/B data bus. The device produces a trapezoidal output waveform during transmission.

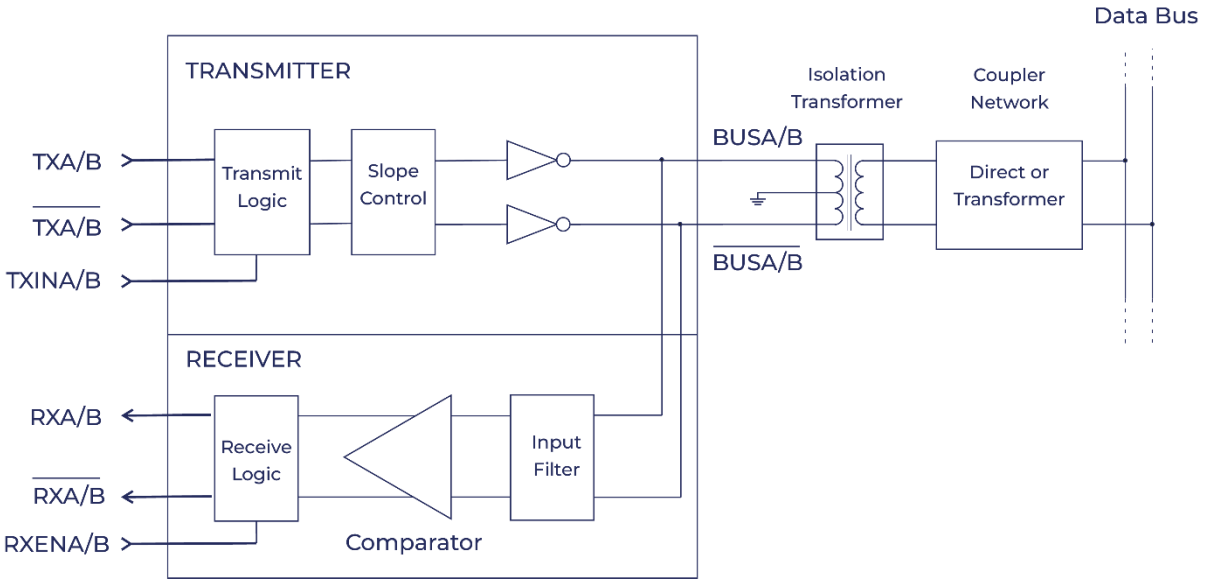
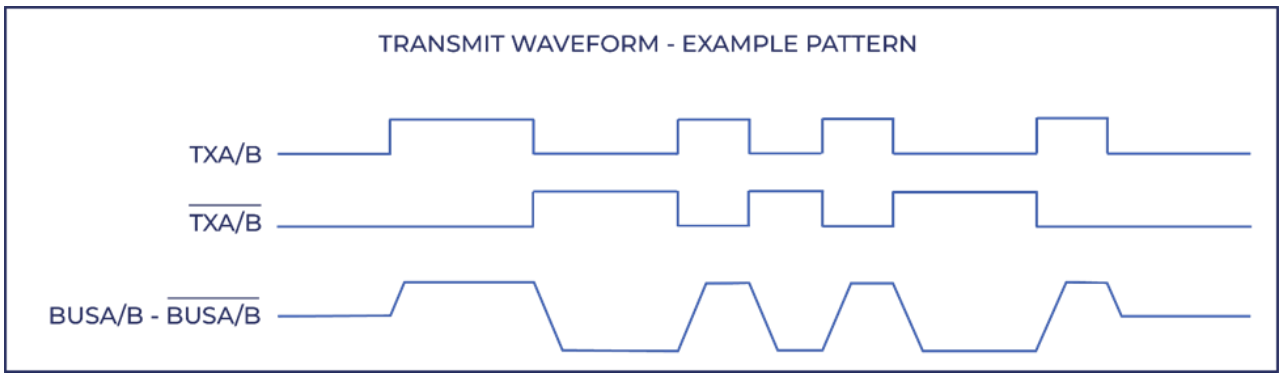


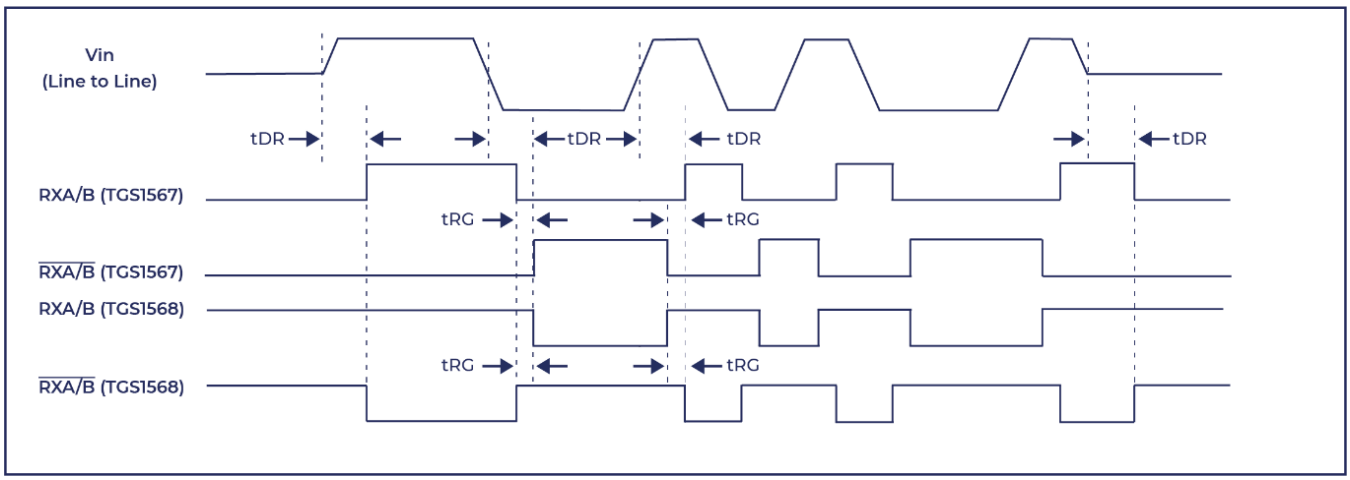
Figure 1. TGS1567/TGS1568 Block Diagram

Transmitter

Data input to the device's transmitter section is from the complementary CMOS inputs TXA/B and $\overline{\text{TXA/B}}$. The transmitter accepts Manchester II bi-phase data and converts it to dif ferential voltages on BUSA/B and $\overline{\text{BUSA/B}}$. The transceiver outputs are either direct- or transformer-coupled to the MIL STD-1553 data bus. Both coupling methods produce a nominal voltage on the bus of 7.5 volts peak to peak.

The transmitter is automatically inhibited and placed in the high impedance state when both TXA/B and $\overline{\text{TXA/B}}$ are driven with the same logic state. A logic "1" applied to the TXINHA/B input will force the transmitter to the high impedance state, regardless of the state of TXA/B and $\overline{\text{TXA/B}}$.





Receiver

The receiver accepts bi-phase differential data from the MILSTD-1553 bus through the same direct- or transformer-coupled interface as the transmitter.

The receiver's differential input stage drives a filter and threshold comparator that produces CMOS data at the $\overline{\text{RXA/B}}$ and RXA/B output pins. When the MIL-STD-1553 bus is idle and RXENA or RXENB are high, RXA/B will be logic "0" on TGS1567 and logic "1" on TGS1568.

The receiver outputs are forced to the bus idle state (logic "0" on TGS1567 or logic "1" on TGS1568) when RXENA or RXENB is low.

MIL-STD-1553 Bus Interface

A direct-coupled interface (see Figure 2) uses a 1:2.5 ratio isolation transformer and two 55 Ohm isolation resistors between the transformer and the bus.

In a transformer coupled interface (see Figure 2), the transceiver is connected to a 1:1.79 isolation transformer which in turn is connected to a 1:1.4 coupling transformer. The transformer coupled method also requires two coupling resistors equal to 75% of the bus characteristic impedance (Zo) between the coupling transformer and the bus.

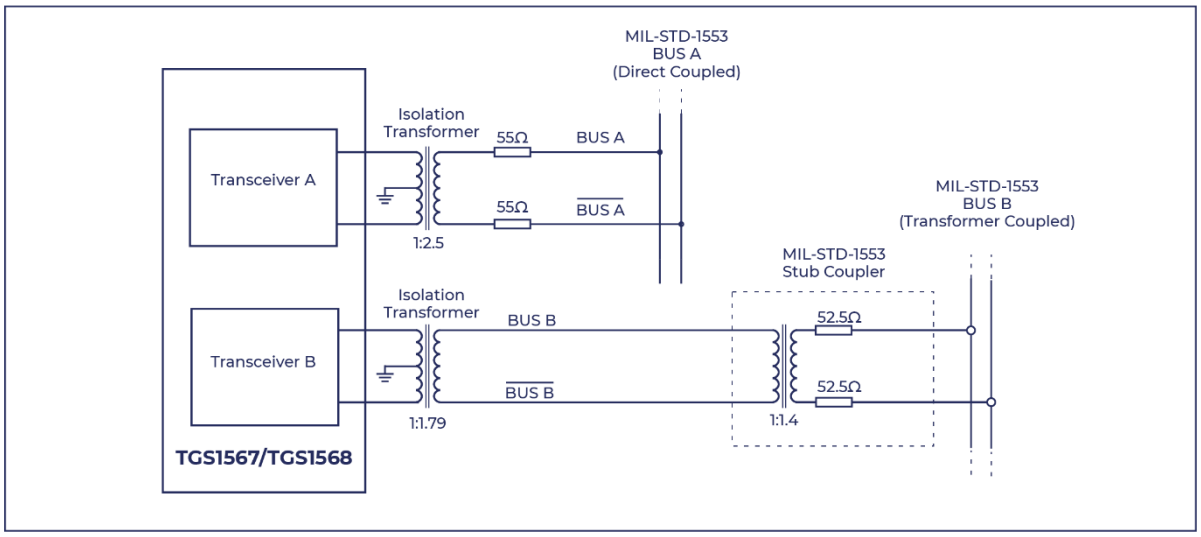


Figure 2. Bus Connection Example using TGS1567 or TGS1568

Figure 3 and Figure 4 show test circuits for measuring electrical characteristics of both direct- and transformer coupled interfaces respectively. (See electrical characteristics on the following pages).

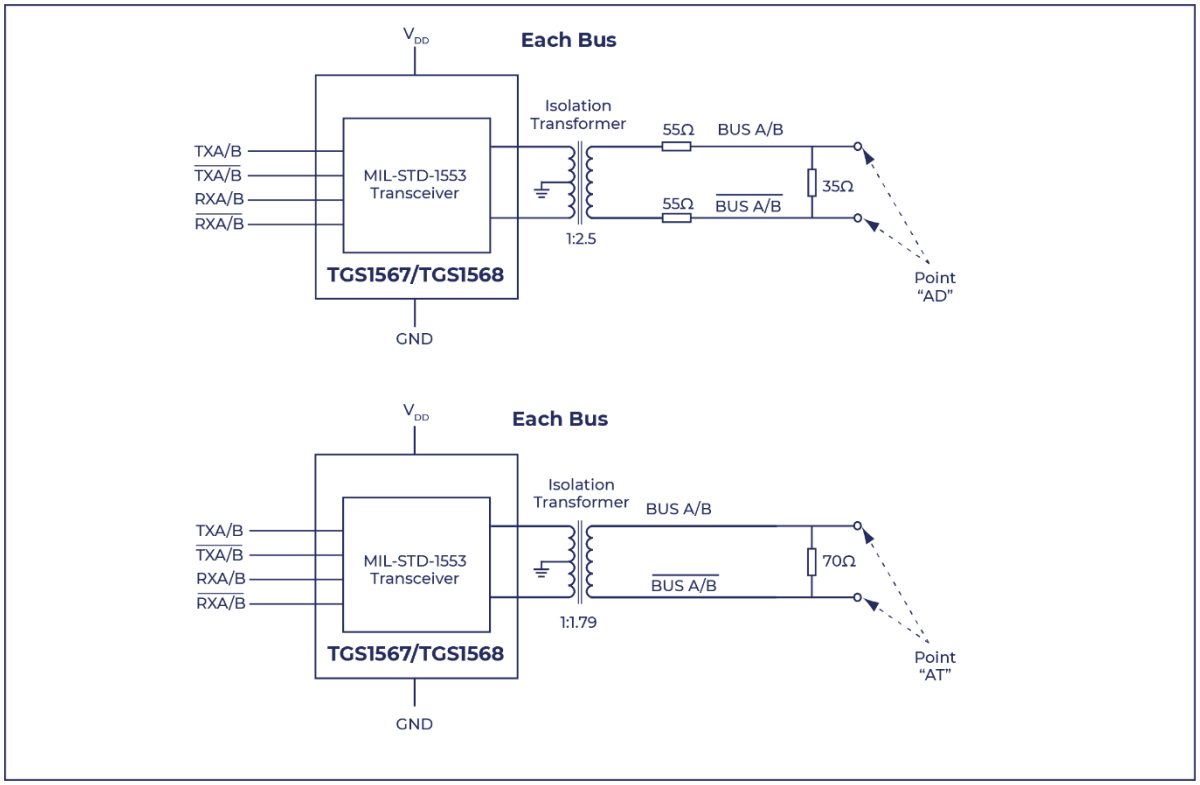


Figure 3 and 4. Direct Coupled Test Circuit and Transformer Coupled Test Circuit

Package Information

Plastic ESOP-20 Package