TGS9253

4-channel, 14 Bit 80/100/110 MSPS ADC

Data sheet

Main performance

- 1.8 V power supply
- Low power consumption: 110 mW per channel (110 MSps)
- Signal-to-Noise Ratio (SNR): 73 dB (to Nyquist frequency)
- Differential Nonlinearity (DNL): ±0.75 LSB (typical value)
- Integral Nonlinearity (INL): ±2.5 LSB (typical value)
- Serial-LVDS
- 2 V PP Input voltage range
- Fully compatible with AD9253
- QFN-48 package 7 mm × 7 mm

Application

- Medical Imaging and Noninvasive Ultrasound Testing
- Test Equipment
- Radio receiver
- Optic fiber network

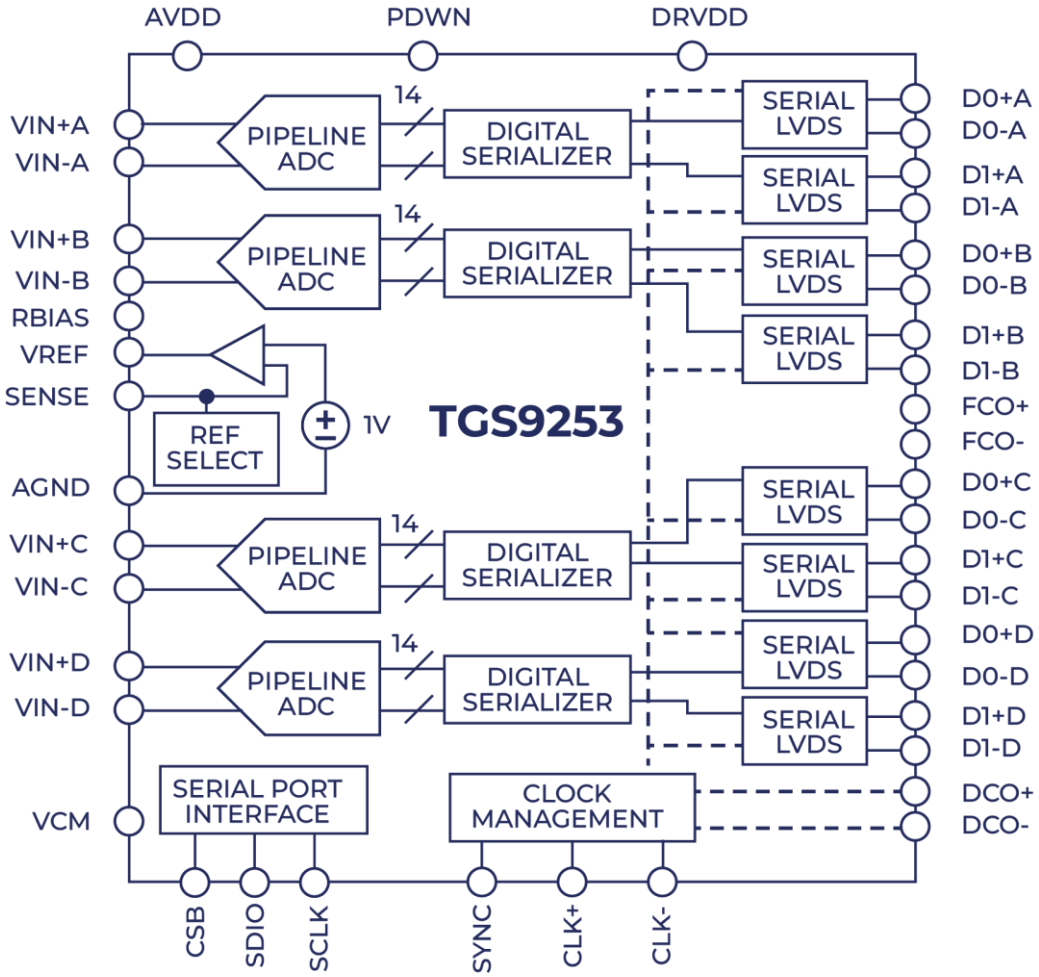

Figure 1. Schematic diagram of chip module

Product Overview

The TGS9253 is a 4-channel, 14-bit, 80 MSps/ 100 MSps/ 110 MSps analog-to-digital converter (ADC) with a built-in sample and hold circuit, designed for low cost, low power consumption, small size and ease of use. The conversion rate of this product can reach up to 110 MSps, with outstanding dynamic performance and low power consumption.

The ADC operates from a single 1.8 V supply and operates with an LVPECL/CMOS/LVDS compatible sample rate clock signal to maximize its performance. For most applications, no external reference power source or driving device is required.

To obtain the proper LVDS serial data rate, the ADC automatically multiplies the sample rate clock. It provides a data clock output (DCO) for capturing data at the output and a frame clock output (FCO) for signaling new output bytes. It also allows each channel to enter a power-saving state independently; typical power consumption is less than 2mW when all channels are disabled.

The TGS9253 is available in a ROHS-compliant 48-pin QFN package.

Technical Specifications

ADC DC characteristics

AVDD = 1.8 unless otherwise specified V, DRVDD = 1.8 V, 110 MSps Sampling rate,

VIN = −1.0 dBFS differential input, 1.0 V Internal reference voltage.

Table 1. ADC DC characteristics

Parameter	Temp.	Minimum	Typical value	Maximum	Unit
Resolution			14		bit
No missing codes	All		Guarantee		
Offset error	All	- 0.7	- 0.3	+0.1	%FSR
Gain error	All	- 10	- 5	0	%FSR
Differential Nonlinearity (DNL)[1]	All 25℃	- 2.0	 ±0.75	+2.0	LSB LSB
Integral Nonlinearity (INL)[1]	All 25℃	- 5.0	 ±2	+5.0	LSB LSB
Internal reference voltage error	All		±5		mV
Input referred noise (VREF=1V)	25℃		0.94		LSB rms
Analog input range (VREF=1 V)	All		2		Vpp
Input Capacitor[2]	All		3		pF
Input common mode voltage	All		0.95		V
AVDD voltage	All	1.7	1.8	1.9	V
DRVDD voltage	All	1.7	1.8	1.9	V
I_{AVDD} supply current	All		196		mA
I_{DRVDD} supply current (ANSI-644 mode)	All		62.6		mA
DC input power consumption	25℃		429		mW
Sine wave input power consumption[1] (ANSI-644 mode)	All		465.5		mW
Shutdown power consumption	25℃		2		mW

1. The measurement conditions are: 10MHz input frequency, full-scale sine wave, and approximately 5pF load per output bit.

2. Effective capacitance between a differential input pin and AGND.

ADC AC characteristics

AVDD = 1.8 unless otherwise specified V, DRVDD = 1.8 V, 110MSps sample, VIN = −1.0 dBFS differential input, 1.0 V Internal reference voltage.

Table 2. ADC AC characteristics

Parameter	Temp.	Minimum	Typical value	Maximum	Unit
Differential Clock Input (CLK+/-)					
Compatible Logic			CMOS/LVDS/LV		
Internal Common Mode Bias Differential Input	Full		PECL 0.9		V
Voltage	Full	0.3		3.6	V
Input Voltage Range	Full	0		1.8	V
Input resistance	Full		15		kΩ
Input capacitance	Full		3.5		pF
Logic input					
(PDWN, SYNC, SCLK, CSB, SDIO)					
logic 1 Voltage	Full	1.2		AVDD 0.6	V
logic 0 Voltage	Full	0			V
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
Digital output (D0±x, D1±x)					
ANSI- 644					
Output Differential Voltage	Full	290	345	400	mV
Output Common Mode Voltage	Full	1.15	1.25	1.35	V
Encoding format (default)			two's complement		

Switch Specifications

AVDD = 1.8 unless otherwise specified V, DRVDD = 1.8 V, 110 MSps sample, VIN = −1.0 dBFS differential input, 1.0 V Internal reference voltage.

Table 3. Switch Parameters

Parameter	Temp	Minimum	Typical value	Maximum	Unit
Clock input parameters					
Input Clock Rate	Complete			880	MHz
Conversion Speed				110	MHz
Aperture Delay (t_A)	All		1		ns
Aperture Jitter	All		0.14		ps rms
Data output parameters					
t_A	All		1		ns
t_{EH}	All		6.25/5/4.55		ns
t_{EL}	All		6.25/5/ 4.55		ns
t_{CPD}	All		t_{FCO} + (t_{SAMPLE} /16)		ns
t_{FCO}	All	1.5	2.3	3.1	ns
t_{FRAME}	All	(t_{SAMPLE} /16)−300	(t_{SAMPLE} /16)	(t_{SAMPLE} /16)+300	ps
t_{PD}	All	1.5	2.3	3.1	ns
t_{DATA}	All	(t_{SAMPLE} /16)−300	(t_{SAMPLE} /16) 90	(t_{SAMPLE} /16)+300	ps
t_{LD}	All				ps

Note: t_{SAMPLE} = 1/f

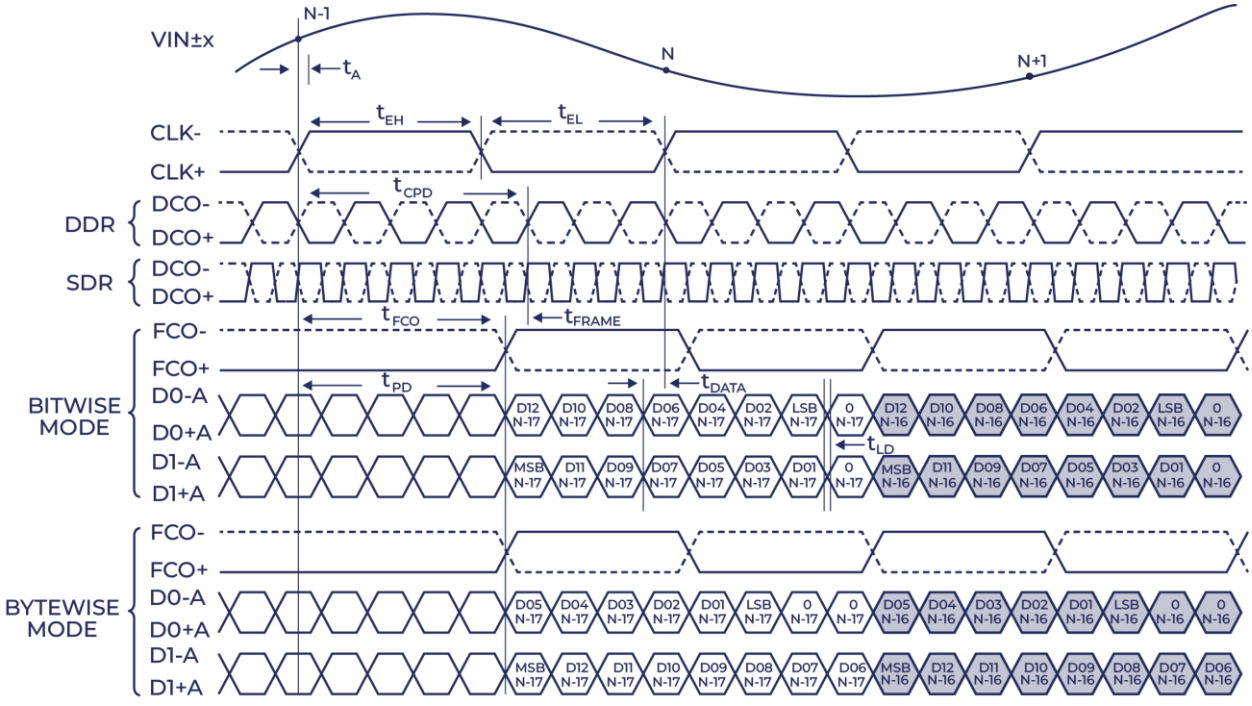

Figure 2. 16-Bit DDR/SDR, Two-Lane, 1 × Frame (Default) working sequence diagram

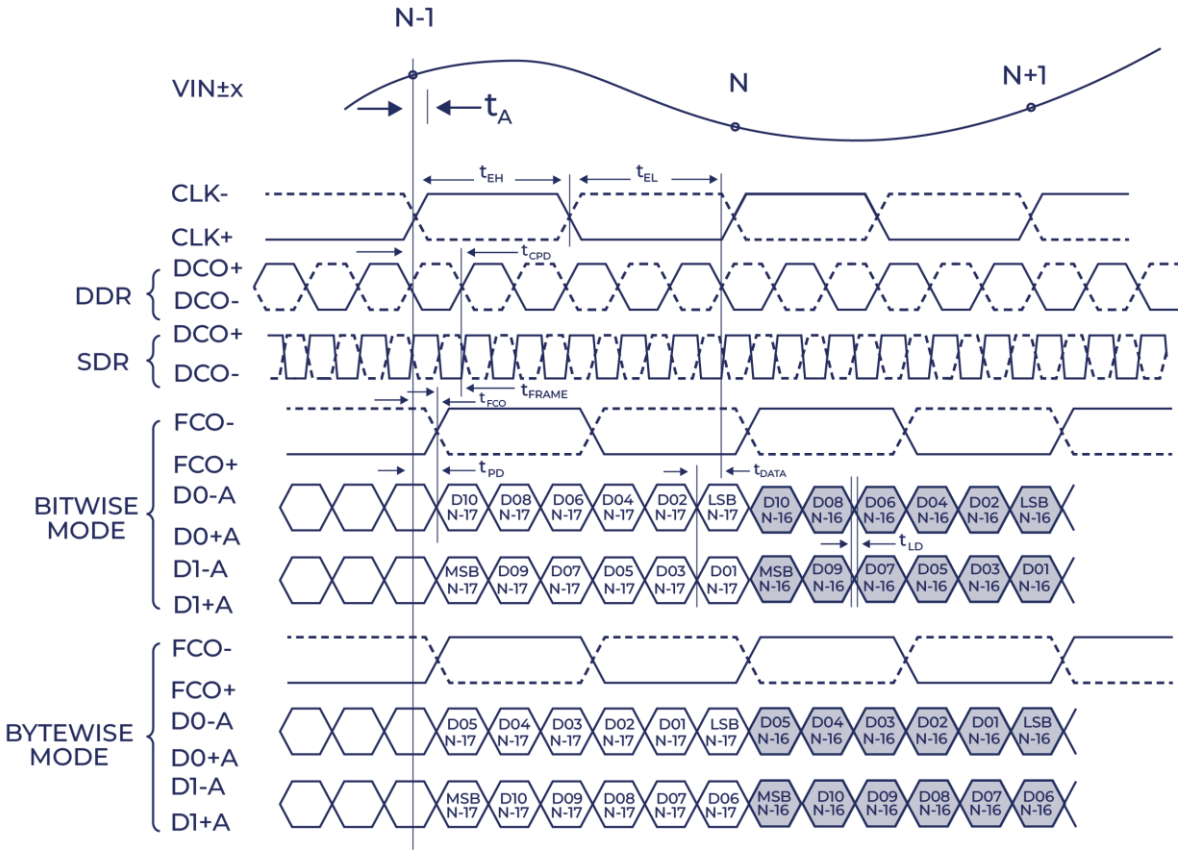

Figure 3. 12-Bit DDR/SDR, Two-Lane, 1 × Frame working sequence diagram

Table 5. SPI Timing parameters

Parameter	Condition	Limit
t_{DS}	Data and SCLK Setup time between rising edges	2 ns, min
t_{DH}	Data and SCLK Hold time between rising edges	2 ns, min
t_{CLK}	SCLK cycle	40 ns, min
t_S	CSB with SCLK settling time between	2 ns, min
t_H	CSB with SCLK hold time between	2 ns, min
t_{HIGH}	SCLK High level pulse width	10 ns, min
t_{LOW}	SCLK Low level pulse width	10 ns, min

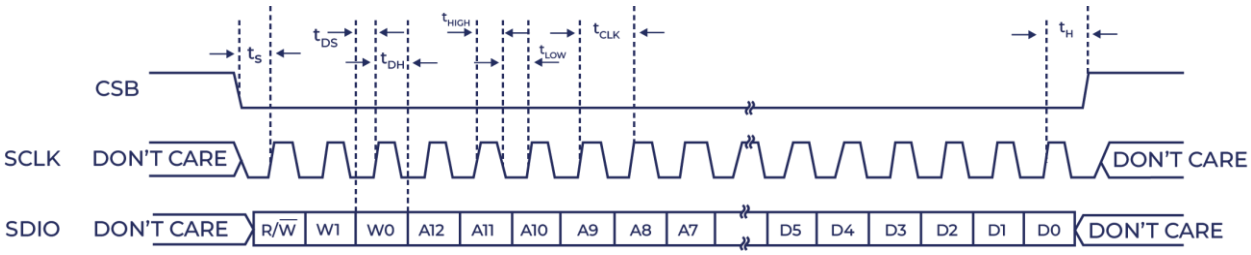

Figure 4. Serial Port Interface Timing

Limit parameters

Voltage (AVDD, DRVDD) to AGND: **-0.3 V to 2 V**

Input Voltage (VIN +/-, CLK +/-, VREF, SENSE, VCM, RBIAS, CSB, SCLK, SDIO, PDWN):

-0.3 V to 2 V

Output voltage (DCO, FCO, DxA/B/C/D): **-0.3 V to 2 V**

Maximum Junction Temperature $T_{J(max)}$: **150°C**

Operating temperature range: **-40°C to 85°C**

Storage Temperature Range: **-65°C to 150°C**

ESD (Human Body Model): **2000 V**

NOTE: For the maximum limits listed above, permanent damage to the device is likely to occur if the device is operated in an environment exceeding these limits. In practice, it is best not to operate the device at or beyond this limit.

ESD Protect

This product is an electrostatic sensitive device. When handling, take appropriate ESD protection measures to avoid performance degradation or functional failure.

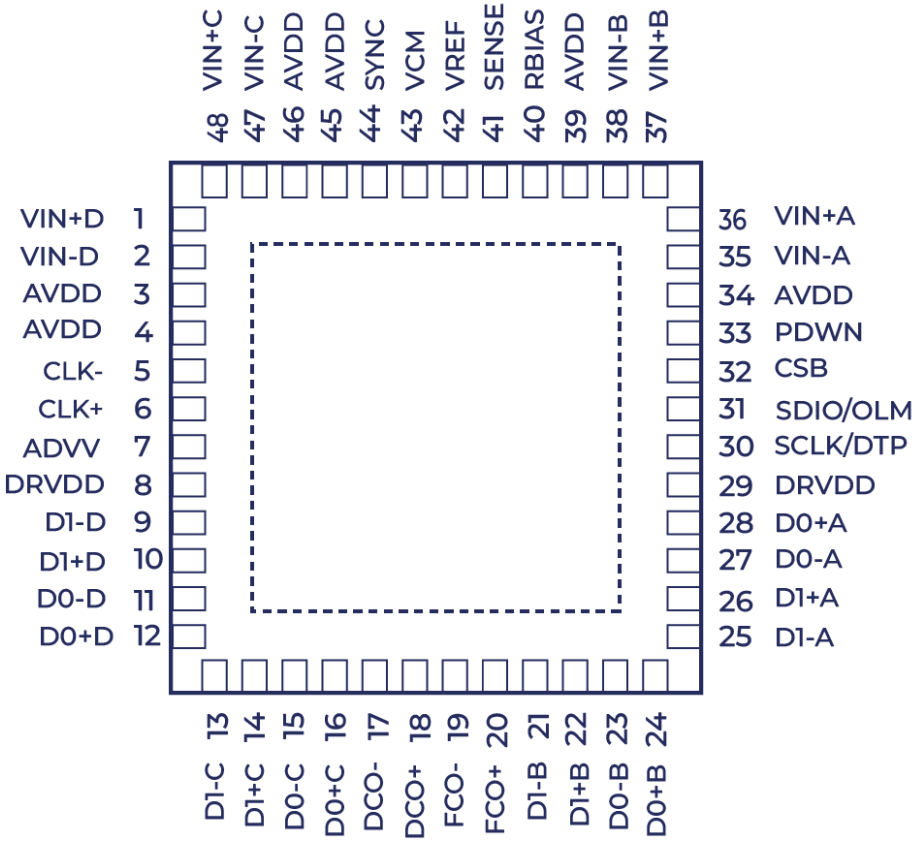

Figure 5. Pin (pad) configuration.

Table 6. Pin Definition.

Pin number	Name	Function
0	AGND, Exposed pad	Analog ground, pad exposed. The bottom pad of the package provides the analog ground for the chip. This exposed pad must be grounded for proper operation.
1	VIN+D	Channel D analog input +
2	VIN−D	Channel D analog input -
3, 4, 7, 34, 39, 45, 46	AVDD	Analog Power, 1.8 V
5, 6	CLK−, CLK+	Differential clock input
8, 29	DRVDD	Digital Output Drive Voltage Source, 1.8 V
9, 10	D1−D, D1+D	Channel D digital output
11, 12	D0−D, D0+D	Channel D digital output
13, 14	D1−C, D1+C	Channel C digital output
15, 16	D0−C, D0+C	Channel C digital output
17, 18	DCO−, DCO+	Data clock output

19, 20	FCO−, FCO+	Frame clock output
21, 22	D1−B, D1+B	Channel B digital output
23, 24	D0−B, D0+B	Channel B digital output
25, 26	D1−A, D1+A	Channel A digital output
27, 28	D0−A, D0+A	Channel A digital output
30	SCLK/DTP	SPI Clock Input / Digital Test Mode
31	SDIO/OLM	SPI Data Input and Output / Data Output Modes
32	CSB	SPI Chip select bar, low enable operation, 30 kΩ Internal pull-up
33	PDWN	Digital input, 30 kΩ internal pull-down
		PDWN high = power off
		PDWN low = device running, normal operation
35	VIN−A	Channel A Analog Input -
36	VIN+A	Channel A Analog Input +
37	VIN+B	Channel B analog input +
38	VIN−B	Channel B Analog Input -
40	RBIAS	Analog Current Bias, with 10 kΩ (1%) resistor to ground
41	SENSE	Reference mode selection
42	VREF	Reference voltage input / output
43	VCM	Analog input common mode
44	SYNC	Digital Input, Sync Input Clock Divider
47	VIN−C	Channel C analog input -
48	VIN+C	Channel C analog input +

Typical curve

Unless otherwise noted, AVDD = 1.8 V, DRVDD = 1.8 V, VIN = −1.0 dBFS differential input, 1.0 V internal reference. Unless otherwise specified, TA=27ºC, 110M sampling.

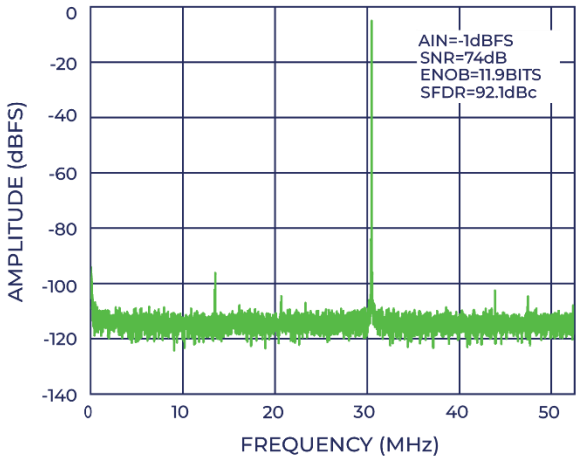

Figure 6. Single-tone FFT
(fin = 30.5MHz@110MSps)

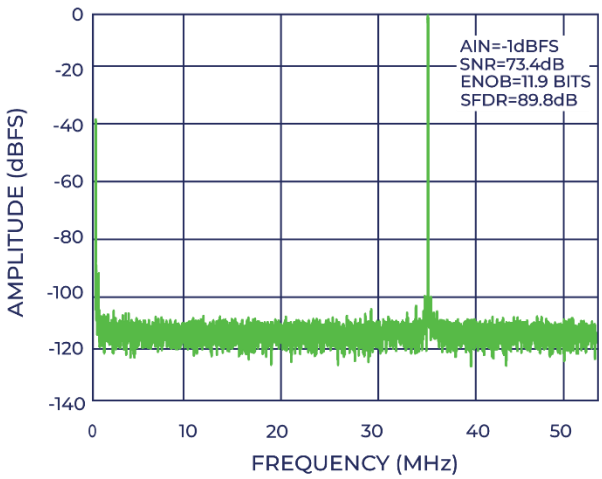

Figure 7. Single-tone FFT
(fin = 70MHz@110MSps)

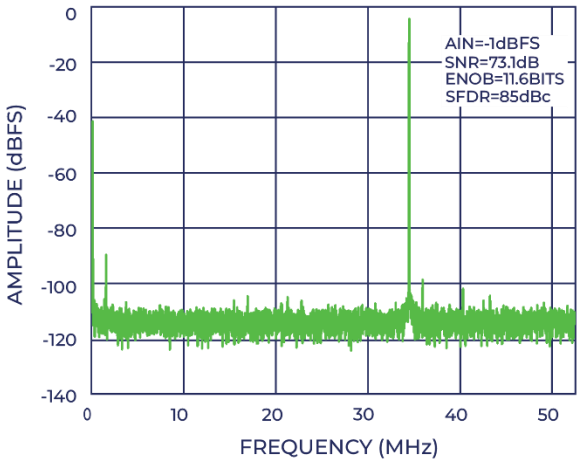

Figure 8. Single-tone FFT
(fin = 140MHz@110MSps)

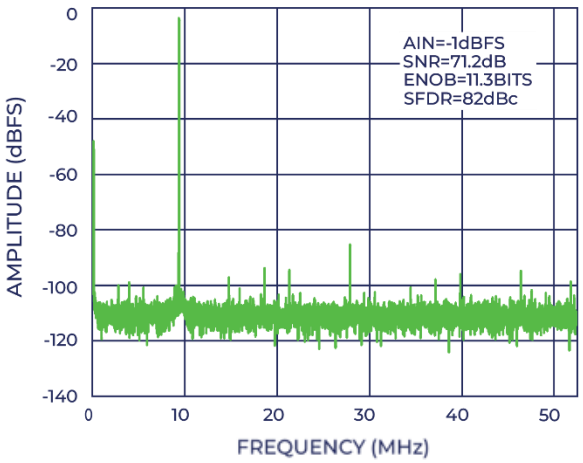

Figure 9. Single tone FFT (fin
= 200MHz@110MSps)

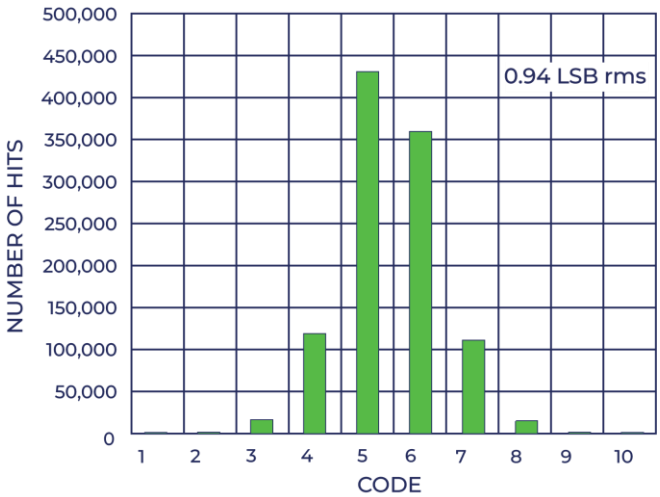

Figure 10. Ground input histogram

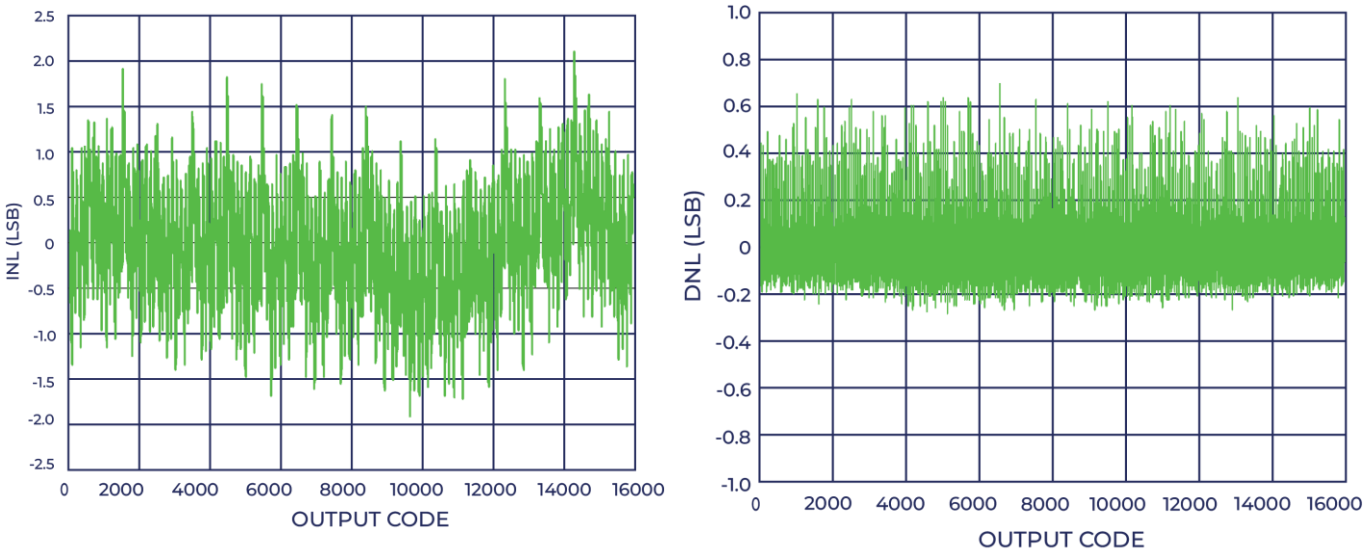

Figure 11. DNL/INL error

Typical Application Circuit

TGS9253 typical application circuits for peripheral devices such as input signals, input clocks, and external DC pins are as follows.

Analog input network

ADC The best performance is achieved by driving the analog inputs differentially. Drives the TGS9253 using a differential dual balun configuration, providing excellent performance and a flexible ADC for baseband applications interface (see Figure 12). When the input frequency is in the second or higher Nyquist region, the noise performance of most amplifiers cannot meet the requirements to achieve the TGS9253 true SNR performance, differential transformer coupling is the recommended input configuration (see Figure 13). Regardless of configuration, parallel capacitor C1 The value of is dependent on the input frequency and may need to be reduced or removed. It is not recommended to drive the TGS9253 input single-ended.

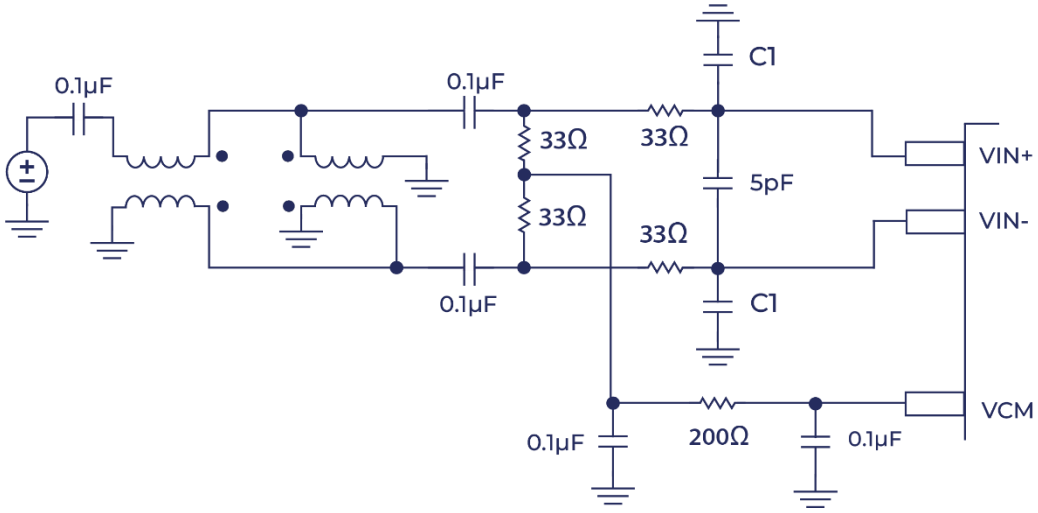

Figure 12. Differential Dual Balun Input Configuration

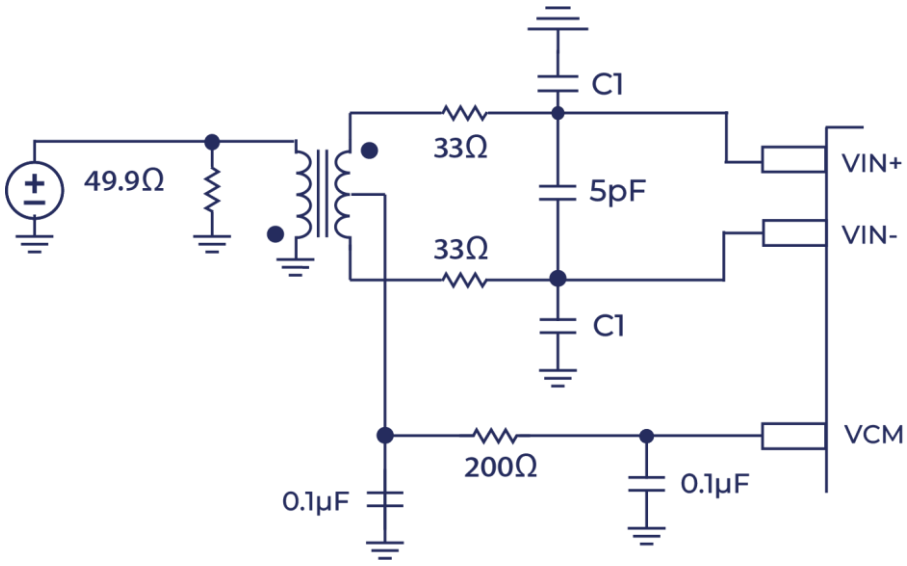

Figure 13. Differential Transformer Coupled Input Configuration

Clock input network

In order to take full advantage of the performance of the chip, a differential signal should be used as the clock signal of the TGS9253 sampling clock input (CLK +/-). The input clock pins are internally biased and do not require external biasing. It is recommended to sample the RF transformer configuration as shown in Figure 14 shown. Back-to-back Schottky diodes across the transformer can connect the input to the TGS9253 The clock signal in is limited to about differential 0.8 V peak-to-peak. This prevents the large voltage swings of the clock from feeding through to other parts, while preserving the fast rise and fall times of the signal, which are important for low jitter performance.

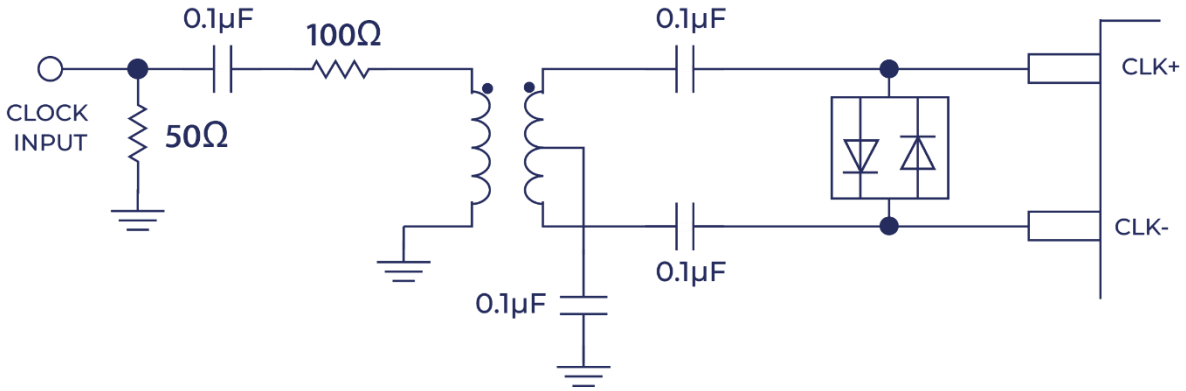

Figure 14. Clock Input Configuration

Internal reference connection

The built-in comparator of the TGS9253 detects the voltage on the SENSE pin, thereby configuring the reference voltage into two different modes (see Table 7). If the SENSE pin is connected to ground, the reference amplifier switch reference amplifier switch is connected to an internal resistor divider internally sets VREF to 1.0 V. If the TGS9253's internal reference is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be taken into account. When the pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference, which must be limited to a maximum of 1.0 V. It is not recommended to leave the SENSE pin floating.

Table 7. Summary of Reference Voltage Configurations

Selected mode	SENSE Voltage	Corresponding VREF (V)	Corresponding Scoring Range (Vpp)
External reference voltage Internal reference voltage	AVDD AGND to 0.2	1.0 1.0	2.0 2.0

Digital output format

TGS9253 output driver is 1.8 V CMOS logic series interface, the timing is shown in Figure 2. The output driver should be able to provide enough output current to drive various logic circuits, and the driving force can be adjusted through registers. However, large drive currents can cause glitches in the power supply signal, affecting the performance of the converter. Therefore, in applications that require the ADC to drive large capacitive loads or large fanouts, external buffers or latches may be required. The format of the output data is two's complement by default, and the example of the output encoding format is shown in Table 8. The format of the output data can also be modified through the register.

Table 8. Data output format

Input (V)	Condition	Offset binary mode	Two's complement mode
VIN+ - VIN-	< -VREF – 0.5LSB	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ - VIN-	= - VREF	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ - VIN-	= 0	1000 0000 0000 0000	0000 0000 0000 0000
VIN+ - Vin-	= +VREF – 1LSB	1111 1111 1111 1100	0111 1111 1111 1100
VIN+ - Vin-	> +VREF – 0.5LSB	1111 1111 1111 1100	0111 1111 1111 1100

When using SPI, the DCO phase can be adjusted in 60° increments relative to one data cycle (30° relative to one DCO cycle). This enables the user to optimize the system timing margin as needed. As shown in Figure 2, the default DCO± output data edge timing is 180° relative to one data period (90° relative to one DCO period). In default mode, as shown in Figure 2, the MSB is first in the data output serial stream. This can be reversed by using SPI so that the LSB is first in the data output serial stream.

There are 12 digital output test mode options that can be initiated via SPI. This is a useful feature to verify receiver acquisition and timing. See Table 9 for available output bit ordering options. Some test patterns have two consecutive words that alternate in various ways depending on the chosen test pattern. Note that some schemas do not match the data format selection options. Additionally, custom user-defined test patterns can be assigned in register addresses 0x19, 0x1A, 0x1B, and 0x1C.

PN sequence short produces a pseudorandom bit sequence that repeats every 29−1 or 511 bits. For the description of the PN sequence and its generation, please refer to Section 5.1 of the ITU-T 0.150 (05/96) standard. The initial values are all 1s (see Table 10 for initial values). The output is a parallel representation of the serial PN9 sequence in MSB first format. The first output word is the first 14 bits of the PN9 sequence, in MSB-aligned form.

PN sequence long produces a pseudorandom bit sequence that repeats every 223−1 or 8388607 bits. For the description of the PN sequence and its generation, please refer to Section 5.6 of the ITU-T 0.150 (05/96) standard. The initial values are all 1s (see Table 10 for the initial values), and the TGS9253 inverts the bit stream according to the ITU standard. The output is a parallel representation of the serial PN23 sequence in MSB first format. The first output word is the first 14 bits of the PN23 sequence, in MSB-aligned form.

Table 9. Flexible Output Test Modes

Output Test Mode Bit Sequence	Schema name	Digital output word 1	Digital output word 2	Select according to data format	Notes
0000	Off (default)	N/A	N/A	N/A	
0001	Midscale short	1000 0000 0000 (12- bit) 1000 0000 0000 0000 (16- bit)	N/A	Yes	Offset binary code shown
0010	+Full-scale short	1111 1111 1111 (12- bit) 1111 1111 1111 1100 (16- bit)	N/A	Yes	Offset binary code shown
0011	−Full-scale short	0000 0000 0000 (12- bit) 0000 0000 0000 0000 (16- bit)	N/A	Yes	Offset binary code shown
0100	Checkerboard	1010 1010 1010 (12- bit) 1010 1010 1010 1000 (16- bit)	0101 0101 0101 (12- bit) 0101 0101 0101 0100 (16- bit)	No	
0101	PN sequence long	N/A	N/A	Yes	PN23 ITU 0.150 $X^{23}+ X^{18} +1$
0110	PN sequence short	N/A	N/A	Yes	PN9 ITU 0.150 $X^{9} + X^{5} +1$
0111	One-/zero-word Toggle	1111 1111 1111 (12- bit) 111 1111 1111 1100 (16- bit)	0000 0000 0000 (12- bit) 0000 0000 0000 0000 (16- bit)	No	
1000	User input	Register 0x19 to Register 0x1A	Register 0x1B to Register 0x1C	No	
1001	1-/0-bit toggle	1010 1010 1010 (12- bit) 1010 1010 1010 1000 (16- bit)	N/A	No	
1010	1× sync	0000 0011 1111 (12- bit) 0000 0001 1111 1100 (16- bit)	N/A	No	
1011	One bit high	1000 0000 0000 (12- bit) 1000 0000 0000 0000 (16- bit)	N/A	No	Pattern associated with the external pin
1100	Mixed frequency	1010 0011 0011 (12- bit) 1010 0001 1001 1100 (16- bit)	N/A	No	

Table 10. PN Sequence

Sequence	Initial value	The next three output samples (MSB priority) two's complement
PN Sequence Short	0x1FE0	0x1DF1, 0x3CC8, 0x294E
PN Sequence Long	0x1FFF	0x1FE0, 0x2001, 0x1C00

See the register list for information on how to change the timing characteristics of these additional digital outputs via SPI.

SCLK/DTP Pin

The SCLK/DTP pin is used for applications that do not require SPI mode operation. If this pin and the CSB pin are held high during device power-up, a single digital test mode can be enabled. When SCLK/DTP is connected to AVDD, the ADC channel output is shifted out in the following pattern: 1000 0000 0000 0000. The FCO and DCO function normally, while all channels are shifted out of a repeatable test pattern. This mode allows the user to perform timing alignment adjustments between the FCO, DCO and output data. This pin has an internal 10 kΩ resistor to ground. It can be disconnected.

Table 11. Digital Test Mode Pin Settings

Selected DTP	DTP Voltage	Result D0±x and D1±x
Normal Operation DTP	10 kΩ to AGND AVDD	Normal Operation 1000 0000 0000 0000

Additional and custom test patterns can also be observed when commands are issued from the SPI port. See the register list for available options.

CSB Pin

For applications that do not require SPI mode operation, the CSB pin should be tied to AVDD. By setting CSB high, all SCLK and SDIO information will be ignored.

RBIAS Pin

The TGS9253 requires the user to place a 10 kΩ resistor between the RBIAS pin and ground. This resistor is used to set the main reference current for the ADC core and has a tolerance of at least 1%.

Output test mode

The output test options are described in Table 9 and are controlled by the output test mode bits at Address 0x0D. When the output test mode is enabled, the analog portion of the ADC is disconnected from the digital backend block and the test mode runs through the output format block. Some test modes are constrained by the output format, some are not. The PN generator in the PN sequence test can be reset by setting Register 0x0D, Bit 4 or Bit 5. These tests can be done on an analog signal (if present, ignore the analog signal), but they require an encoded clock.

Serial Port Interface (SPI)

The TGS9253 serial port interface (SPI) allows the user to configure the corresponding function registers inside the ADC to meet the needs of specific functions and operations. Through the serial port, the address space can be accessed, read and written. The SPI of this ADC consists of three parts: SCLK pin, SDIO pin and CSB pin. The SCLK (serial clock) pin is used to synchronize read and write data from the ADC; the SDIO (serial data input/output) dual function pin allows data to be sent to or read from internal registers; CSB (Chip Select) pin is an active low control pin that enables or disables read and write cycles. The timing requirements are shown in Figure 3.

Internal Register List

Table 12. Register List

Address (HEX)	Register name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Defaults (HEX)	Notes
0x00	Port config	0 =SDO active	LSB first	Soft reset	1 =16-bit address	1=16-bit address	Soft reset	LSB first	0 =SDO active	0x18	ADC default setting is 16bit pattern
0x01	Chip ID	0x8F = quad 14-bit 80 MSPS/100 MSPS/110 MSPS serial LVDS								0x8F	Unique chip ID used to distinguish devices; read only
0x02	Speed grade		100 = 80 MSPS 101 = 100 MSPS 110 = 110 MSPS								Unique speed class ID that distinguishes the device; read only
0x05	Channel selection			Clock Channel DCO	Clock Channel FCO	Data Channel D	Data Channel C	Data Channel B	Data Channel A	0x3F	Determines which channel on the chip receives the next write command; the default is all channels on the chip
0x08	Model	External Power-down enable	External pin function 0x00 Full power-down 0x01 standby					00 = chip run 01 = full power-down 10 = standby 11 = digital reset		0x80	Identify various general modes of chip operation
0x0B	Clock division						Clock divide ratio[2:0] 000 = divide by 1 001 = divide by 1 010 = divide by 2 011 = divide by 3 100 = divide by 4 101 = divide by 5 110 = divide by 6 111 = divide by 7			0x00	

Address (HEX)	Register name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Defaults (HEX)	Notes
0x0D	test mode	User input test mode 00 = single 01 = alternate 10 = single once 11 = alternate once		Reset PN long sequence	Reset PN short sequence	Output test mode:0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = one/zero word toggle 1000 = user input 1001 = 1-/0-bit toggle 1010 = 1x sync 1011 = one bit high 1100 = mixed bit frequency				0x00	After setting the test data is put on the output pin instead of the normal data
0x10	Offset Adjustment	8-bit device offset adjustment [7:0] Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	Offset fine-tuning
0x14	ADC output mode		LVDS-ANSI/LVDS-IEEE option 0=LVDSANSI 1=LVDSIEEE reduced range link				Output Invert		Output format 0 = offset binary 1 = two's completion	0x01	Configure output and data formats
0x19	USER_PATT1_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Mode, 1 LSB
0x1A	USER_PATT1_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User defined mode, 1 MSB
0x1B	USER_PATT2_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Mode, 2 LSB
0x1C	USER_PATT2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Mode, 2 MSB
0x21	serial output out data control	LVDS output LSB first	SDR/DDR one-lane/two-lane, bitwise/bytewise [6:4] 000 = SDR two-lane, bitwise 001 = SDR two-lane, bytewise 010 = DDR two-lane, bitwise 011 = DDR two-lane, bytewise 100 = DDR one- lane				Select 2x frame		output number of bits 00 = 16 bits 10 = 12 bits	0x30	Serial flow control
0x22	Serial channel status							Channel output reset	Channel Power-down	0x00	Used to cut off power to various parts of the converter
0x102	I/O control					VCM Power-down				0x00	VCM control
0x109	SYNC							SYNC only first pulse	SYNC enable	0x00	

Application Information

Power and Grounding Recommendations

It is recommended to use two separate 1.8 V supplies to power the TGS9253: one for the analog AVDD and one for the digital output DRVDD. For AVDD and DRVDD, several different decoupling capacitors should be used to support high and low frequencies. Decoupling capacitors should be placed close to the PCB entry point and close to the device pins, keeping trace lengths as short as possible. The TGS9253 requires only one PCB ground plane. Proper decoupling and clever separation of PCB analog, digital, and clock blocks makes it easy to get the best performance.

Exposed Pad Heatsink Recommendations

For best electrical and thermal performance, the exposed pad on the bottom of the ADC must be connected to the analog ground, AGND. The exposed continuous copper plane on the PCB should match the exposed pad of the TGS9253. There should be multiple vias on the copper planes to get the lowest possible thermal resistance path for heat dissipation through the bottom of the PCB. These vias should be filled or plugged to prevent the vias from seeping tin and affecting the connection performance. In order to maximize the coverage and connection between the ADC and the PCB, a silkscreen layer should be covered on the PCB to divide the continuous plane on the PCB into multiple equal parts. In this way, multiple connection points can be provided between the ADC and the PCB during the reflow process. A continuous, undivided plane guarantees only one connection point between the ADC and the PCB.

VCM

The VCM pin should be decoupled to ground with a 0.1 uF capacitor.

Reference Decoupling

The VREF pin should be externally decoupled to ground with a low ESR 0.1 uF ceramic capacitor in parallel with a low ESR 1.0 uF capacitor.

SPI port

The SPI port should be disabled when the converter is required to take advantage of its full dynamic performance. Usually the SCLK, CSB, and SDIO signals are asynchronous to the ADC clock, so noise in these signals can degrade converter performance. If other devices use the on-board SPI bus, a buffer may need to be connected between this bus and the TGS9253 to prevent these signals from changing at the input of the converter during critical sampling periods.

Dimensions

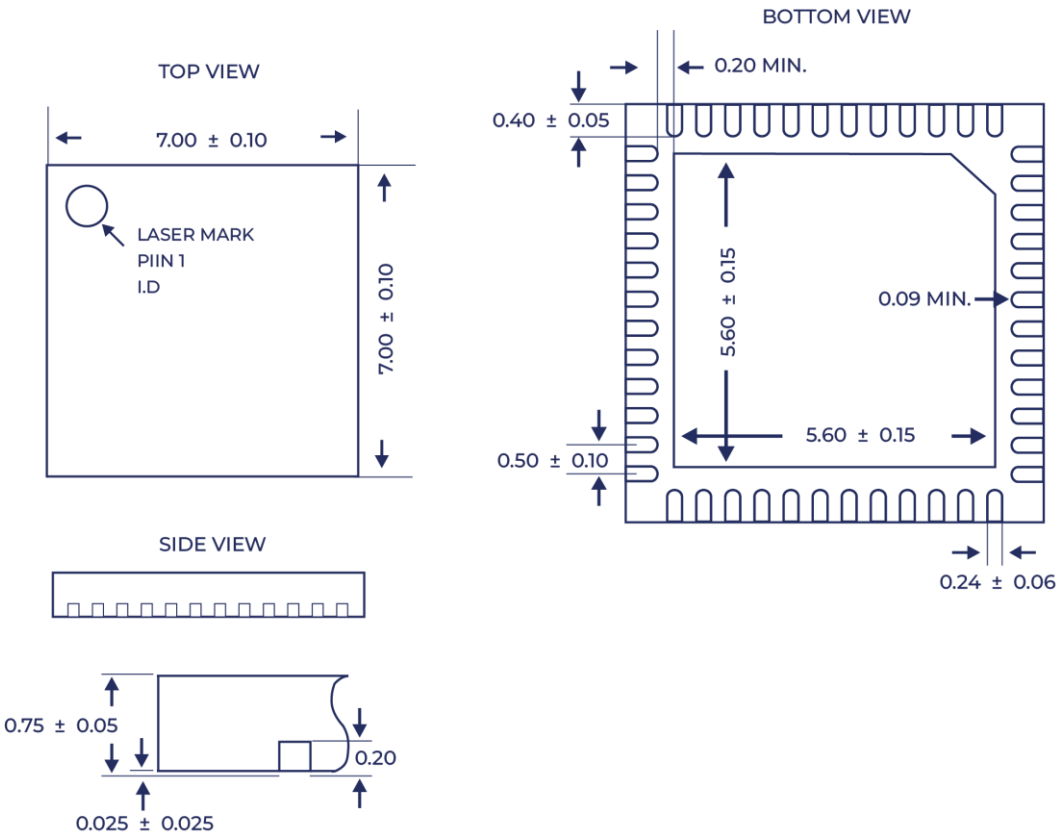

Figure 15. Dimensions of 48-pin QFN package

Product Marking

PN: TGS9253

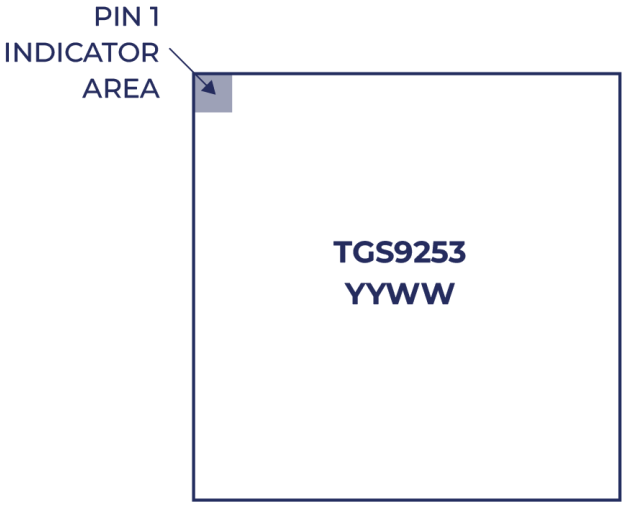

Figure 16. Marking code

First line: Part number model
Second line: Manufacturer date code*

Note*
YY - last two digits of the calendar year
WW - last two digits being the week of the year