TGS8591-P

ARINC 429 Bus Receiver

Data sheet

1. Product usage and application scope

Semiconductor integrated circuit TGS8591-P type ARINC 429 bus-receiver (hereinafter referred to as TGS8591-P) is an ARINC 429 bus receiver. It can be used in ARINC 429 bus transmission system to receive 429 bus signals and convert them into TTL digital level signals. Its functions and pins are compatible with HOLT company's HI-8591PST.

2. Product standards and quality levels

The quality level of the TGS8591-P chip meets the Class B requirements specified in GJB 597B-2012.

3. Product features

TGS8591-P is a ARINC 429 bus receiver circuit. It is a digital-analog hybrid circuit, powered by a single 3.3V or 5V, and adopts SOP-8 small ceramic package.

TGS8591-P inputs the 10V differential typical signal on the ARINC 429 bus to the window comparator and latch, and then converts it into a TTL level output under logic control. The conversion threshold follows the ARINC 429 protocol requirements: the minimum threshold voltage for receiving valid data is 6.5V, and the maximum threshold for null signals is 2.5V.

The TESTA and TESTB input ports can bypass the bus input signal for testing purposes. TESTA and TESTB When the ports are set high, the digital outputs are forced to zero.

3.1 Main features

The main features of TGS8591-P are as follows:

a. ARINC 429 bus receiver small SOP-8 package

b. 3.3V or 5V single power supply

c. +/-30V common mode voltage range

d. >140KΩ input impedance

e. Receiver input hysteresis is at least 2V

f. Bypassing the test input signal as an analog signal can force the digital output to 1,0 and empty states

3.2 Pin definition

The appearance and pin distribution of TGS8591-P are shown in Figure 1.

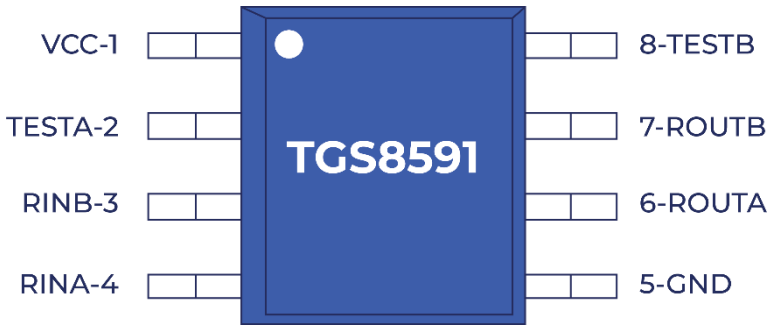

Figure 1 Pin layout

TGS8591-P pin definition is shown in Table 1.

Table 1 Receiver pin descriptions

Terminal number	Symbol	Name	I/O	Remark
1	VCC	Power supply	Pair	3.3V or 5V supply voltage
2	TESTA	Test input	Lose	Logic input port A for testing
3	RINB	Input port B	Lose	Bus input port B
4	RINA	Input port A	Lose	Bus input port A
5	GND	Land	Pair	power ground
6	ROUTA	Output port A	Lose	Bus output port A
7	ROUTB	Output port B	Lose	Bus output port B
8	TESTB	Test input	Lose	Logic input port B for testing

3.3 Main functions

The TGS8591-P chip is powered by a 3.3V or 5V single power supply. The chip has high input impedance to minimize bus load, and a special common-mode input voltage range of +/-30V to reduce the impact of aircraft ground offset on the circuit. The two inputs RINA and RINB can be connected directly to the ARINC 429 bus.

The receiver inputs the 10V differential typical signal on the ARINC429 bus to the window comparator and latch, and then controls the output through logic. The reference voltage of the comparator is set to a voltage value below the minimum threshold voltage of ARINC429 valid data of 6.5V, but above the maximum threshold of the null signal of 2.5V.

The chip functional block diagram is shown in Figure 2.

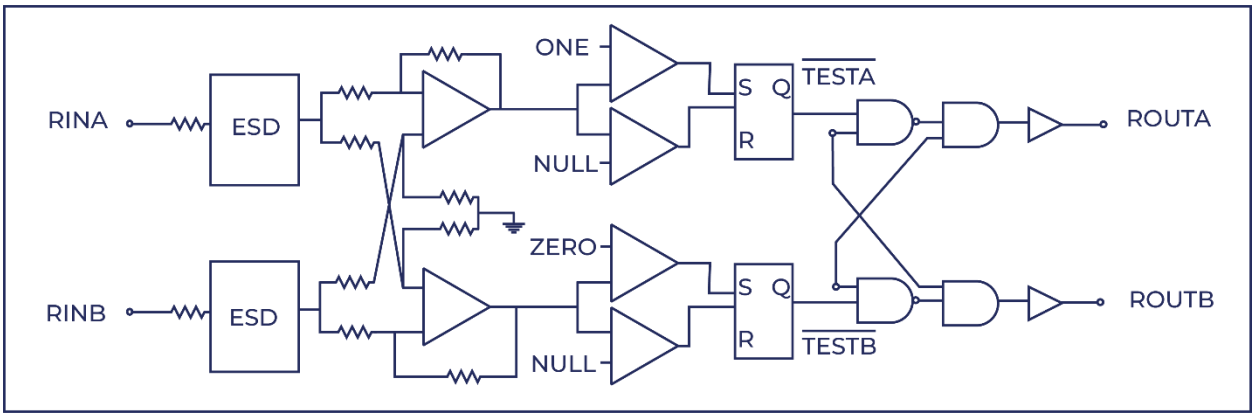

Figure 2 TGS8591-P functional block diagram

TGS8591-P can be directly connected to the 429-bus. It inputs the typical 10V differential signal on the ARINC429 bus to the window comparator and latch, and then controls the output through logic.

TGS8591-P functions are shown in Table 2.

Table 2 TGS-8591-P function table

RINA	**RINB**	**TESTA**	**TESTB**	**ROUTA**	**ROUTB**
-1.25V–1.25V	-1.25V–1.25V	0	0	0	0
-3.25V–-6.5V	3.25V–6.5V	0	0	0	1
3.25V–6.5V	-3.25V–-6.5V	0	0	1	0
×	×	0	1	0	1
×	×	1	0	1	0
×	×	1	1	0	0

4. Dimensions

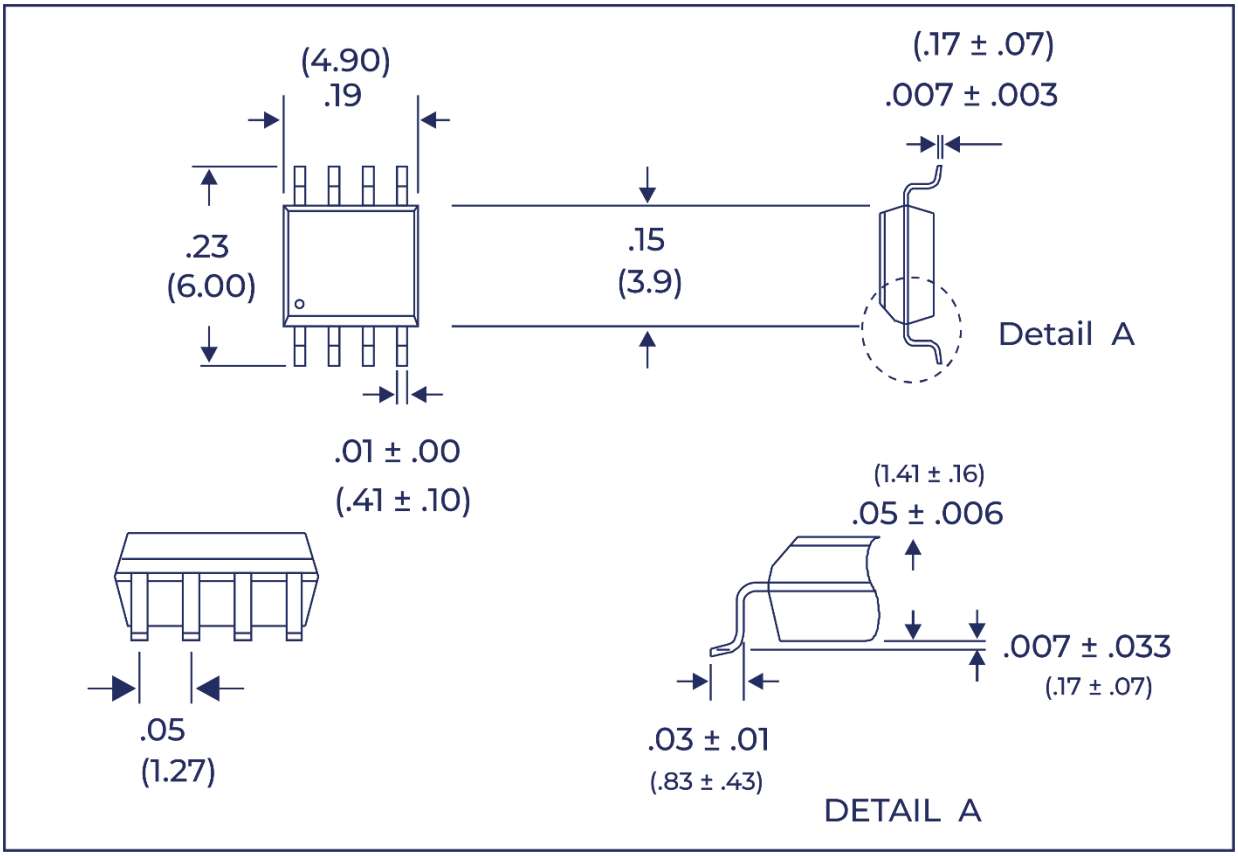

Figure 3 Schematic diagram of shell appearance

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Absolute maximum ratings are shown in Table 4.

Table 4 Absolute Maximum Ratings

Parameter name	Min.	Typ.	Max.	unit
Supply voltage	-0.3	-	+7	V
Input port input voltage	-120	-	120	V
Current	-10	-	+10	mA
Power consumption	-	0.7	-	W
Welding temperature	-	260	-	℃
storage temperature	-65	-	+150	℃

5.2 Recommended working conditions

Recommended operating conditions are shown in Table 5.

Table 5 Recommended working conditions

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Supply voltage	V_{CC}	3	-	3.6	V
Supply voltage	V_{CC}	4.5	-	5.5	V
Working temperature		-55	-	125	℃

5.3 DC characteristics

The DC characteristics of the receiver chip are shown in Table 6.

Table 6 Receiver DC Characteristics

The recommended application environment for this chip is as follows: V_{CC}=5V±0.5V or 3.3V±0.3V, GND=0V, T_A=+25℃.

Parameter	Symbol	Test conditions	Minimum value	Typical value	Maximum value	Unit
1 or 0 NULL Common mode level	V_{DIN} V_{NIN} V_{COM}	Differential voltage, pin3&4 ground reference	6.5 - -30	10 - -	13 2.5 +30	V V V
Digital input voltage high	V_{IH}		75%V_{CC}	-	-	V
Low	V_{IL}			-	25% V_{CC}	V
ARINC input impedance RINA to RINB RINA or RINB to ground RINA or RINB to V_{CC}	R_{DIFF} R_{GND} R_{VCC}	Power supply floating	- - -	300 150 150	- - -	KΩ KΩ KΩ
Digital input current source leak	I_{IH} I_{IL}	V_{IN}=2.0V V_{IN}=0.8V	- -	- -	20 20	μA μA

5.4 AC characteristics

The AC characteristics of the receiver chip are shown in Table 7. Receiver chip timing descriptions are shown in Figures 4 and 5.

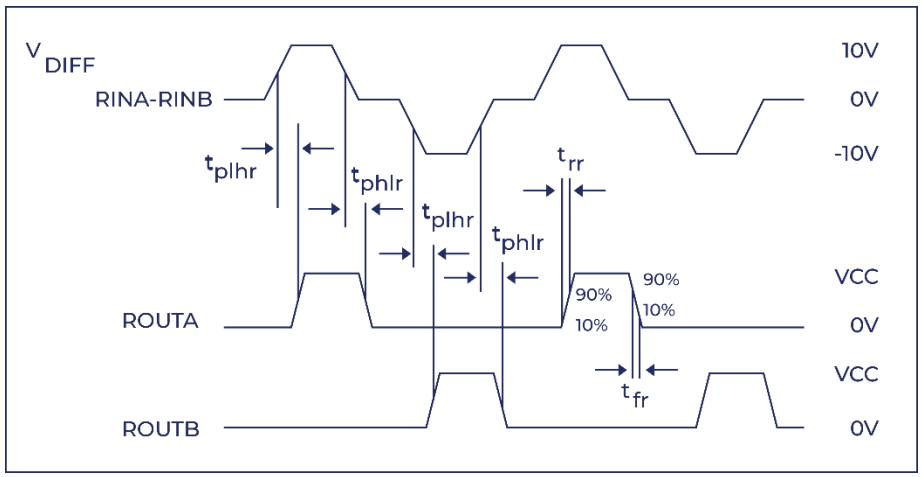

Figure 4 Receive port timing

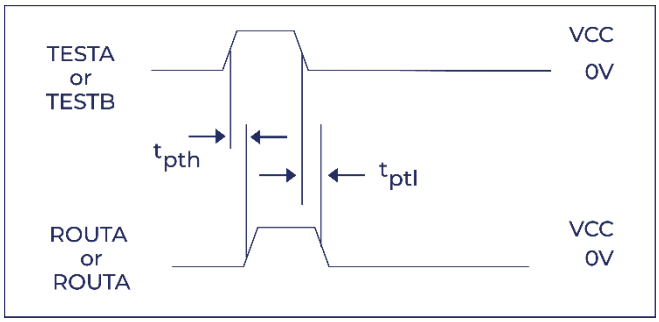

Figure 5 Test port timing

Table 7 Receiver AC Characteristics

The recommended application environment for this chip is as follows: V_{CC}=5V±0.5V or 3.3V±0.3V, GND=0V, T_A=+25℃.

Parameter	Symbol	Condition	Min. value	Typ. value	Max. value	One Bit
Output from high to low	T_{phlr}	As shown in Figure 4, the output load is 50pF, V_{CC}=5V±0.5V	-	600	900	ns
Output from low to high	T_{plhr}		-	600	900	ns
Output from high to low	T_{phlr}	As shown in Figure 4, the output load is 50pF, V_{CC}=3.3V±0.3V	-	600	1000	ns
Output from low to high	T_{plhr}		-	600	1000	ns
Output from high to low	T_{pth}	As shown in Figure 5 V_{CC}=5V±0.5V	-	-	60	ns
Output from low to high	T_{ptl}		-	-	60	ns
Output from high to low	T_{pth}	As shown in Figure 5 V_{CC}=3.3V±0.3V	-	-	100	ns
Output from low to high	T_{ptl}		-	-	100	ns
Output from high to low	T_{fr}	V_{CC}=3.3V±0.3V or 5V±0.5V	-	15	50	ns

Output from low to high	T_{rr}		-	15	50	ns

Note: 1. This is for design considerations only, not test results.

6. Precautions for use

a) When using, it is recommended to use plastic tweezers to prohibit direct contact between the skin and the product to prevent contamination and scratches on the product;

b) The product can be used directly, cleaning is not recommended. If cleaning, it is forbidden to use acid, alkali, etc. for treatment. It is recommended to use ethanol, acetone, etc. After cleaning, ensure that the cleaning is thorough and there is no residue.

c) Before welding, it is recommended to remove the gold from the leads. It is not recommended to solder directly on the lead gold plating. Recommended Tin treatment has achieved the purpose of removing gold. The actual removal effect shall prevail. Please refer to standard QJ 3267;

d) Lead welding can be done by reflow welding or manual welding. Please refer to standards GJB 3243, QJ 3173, QJ3117 and SJ/T10670. It is forbidden for solder to flow to the bending and forming position of the lead, so that the lead can maintain its inherent buffering effect. During board-level use, lead deformation, tearing and falling off due to mismatch between lead material and circuit board should be avoided;

e) In order to ensure the reliability of board-level installation, it is recommended to use special glue to reinforce the device after lead welding. When reinforcing, be careful not to let the glue flow to the bend of the lead;

f) When handling or removing chips, anti-static measures must be taken, such as wearing anti-static gloves or anti-static bracelets;

g) When installing or removing the chip, pay attention to the direction of force application to ensure that the chip pins are evenly stressed. Do not use excessive force, which may cause damage to the pins and render them unusable.