Tegsemi

TGS8588-P

ARINC 429 Line receiver

Data sheet

1. Product usage and application scope

The semiconductor integrated circuit TGS8588-P type ARINC 429-line receiver (hereinafter referred to as TGS8588-P) is an ARINC 429 bus receiver. It can be used in ARINC 429 bus transmission system to receive 429 bus signals and convert them into TTL digital levels.

2. Product standards and quality levels

Semiconductor integrated circuit TGS8588-P type ARINC 429-line receiver detailed specification, number: AFNP-Q/XTME 20000-2018. It was inspected at the Guangzhou Testing Center for Military Electronic Components and passed the first identification. The report number is: MXA190050.

The quality level of the TGS8588-P chip meets the Class B requirements specified in GJB 597B-2012.

3. Product features

TGS8588-P is a 429-bus receiver circuit. It is a digital-analog hybrid circuit with a single 5V power supply.

SOP-8 small ceramic package.

TGS8588-P inputs the 10V differential typical signal on the ARINC429 bus to the window comparator and latch, and then converts it into a TTL output under logic control. The conversion threshold follows the ARINC429 protocol requirements: the minimum threshold voltage for valid data is 6.5V, and the maximum threshold for null signals is 2.5V.

TGS8588-P provides test mode and power saving mode. The TESTA and TESTB input ports can bypass the bus input signal for testing purposes. When both the TESTA and TESTB ports are set high, the power saving mode can be entered and the output is placed in a high impedance state.

3.1 Main features

The main features of TGS8588-P are as follows:

- Directly connected to the ARINC 429 bus and has a small SOP package;
- 5V single power supply;
- >30KΩ input impedance;
- ±5V common mode voltage range;
- At least 2V receiver input hysteresis;
- Provide test mode and power saving mode;
- Functionally and pin-compatible with HOLT's HI-8588.

3.2 Pin definition

The appearance and pin distribution of TGS8588-P are shown in Figure 1.

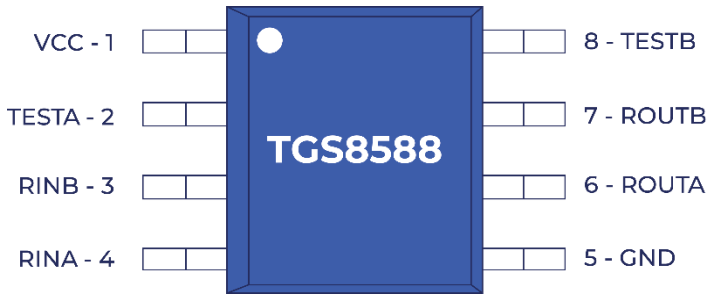


Figure 1 Pin layout

TGS8588-P pin definition is shown in Table 1.

Table 1 Receiver pin descriptions

Symbol	Name	I/O	Remark
V_{CC}	Power supply	Two-way	5V supply voltage
TESTA	Test input port A	enter	Logic input port A for testing
RINB	Input port B	enter	Bus input port B
RINA	Input port A	enter	Bus input port A
GND	Land	Two-way	land
ROUTA	Output port A	output	Bus output port A
ROUTB	Output port B	output	Bus output port B
TESTB	Test input port B	enter	Logic input port B for testing

3.3 Main functions

The structural block diagram of the TGS8588-P receiving chip is shown in Figure 2. The chip uses a single 5V power supply. The input port RINA and RINB have a series resistance with a typical value of 35KΩ and are connected to a ground resistance with a typical value of 10KΩ to form a level shift circuit. Therefore, adding an external series resistor will affect bus transmission.

The 429 bus signal passes through the level transfer circuit, and the input becomes a differential signal and is input to the differential amplifier. The amplifier output signal is compared to the decision circuit and the status information is input to the latch. NULL sets the latch to 0, and a One or Zero signal sets the latch to 1.

The TEST signal controls the logic output. When the TESTA and TESTB signals are both 1, the receiver enters power saving mode and the output port is in a high impedance state. In power-saving mode, the connection relationship between the bus input port and the internal resistor will not be changed.

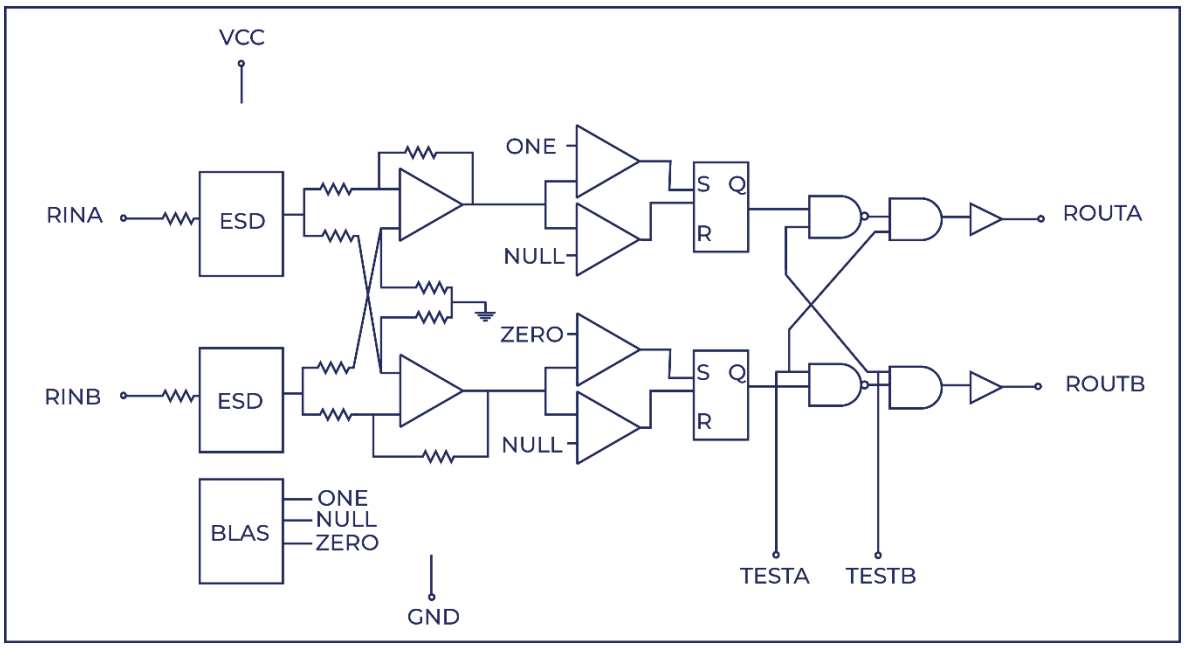


Figure 2 TGS8588-P functional block diagram

TGS8588-P can be directly connected to the 429 bus. It inputs the 10V typical differential signal on the ARINC429 bus to the window comparator and latch, and then controls the output through logic.

TGS8588-P functions are shown in Table 2.

Table 2 TGS8588-P function table

RINA	RINB	TESTA	TESTB	ROUTA	ROUTB
-1.25V–1.25V	-1.25V–1.25V	0	0	0	0
-3.25V–-6.5V	3.25V–6.5V	0	0	0	1
3.25V–6.5V	-3.25V–-6.5V	0	0	1	0
×	×	0	1	0	1
×	×	1	0	1	0
×	×	1	1	Hi-Z	Hi-Z

4. Dimensions

TGS8588-P is a plastic package with SOP-8 appearance. The specific appearance is shown in Figure 3, and the overall dimensions are shown in Table 3.

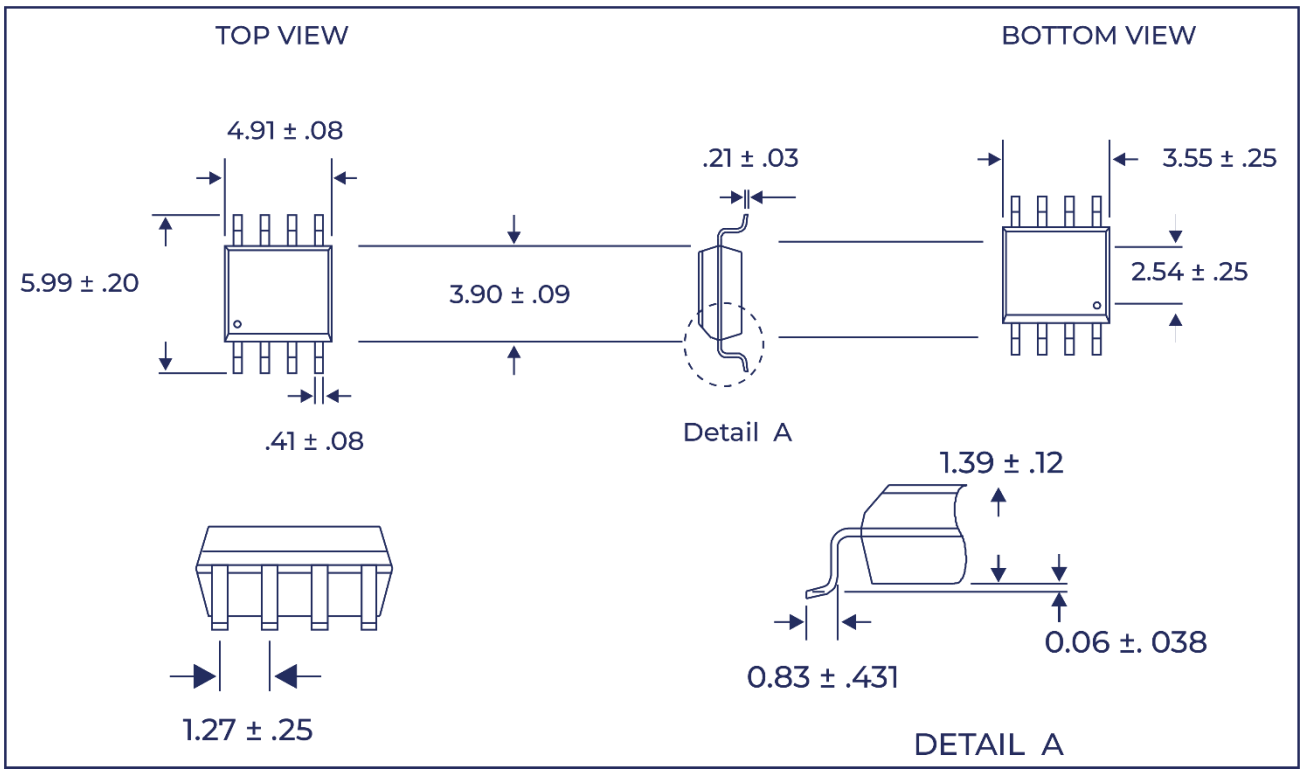
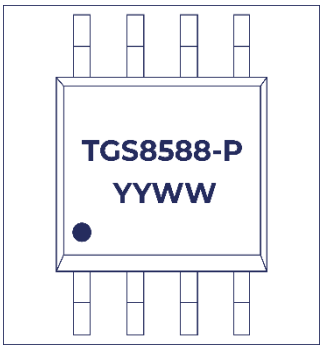


Figure 3 TGS8588-P package outline diagram

4.1 Product marking

PN: TGS8588-P



First line: Part number model
Second line: Manufacturer date code*

Note*
YY - last two digits of the calendar year
WW - last two digits being the week of the year

5. Electrical characteristics

5.1 Absolute maximum ratings

Absolute maximum ratings are shown in Table 4.

Table 4 Absolute Maximum Ratings

Parameter name	**Minimum value**	**Typical value**	**Maximum value**	**Unit**
Supply voltage	-0.3	-	+7	V
Current	-10	-	+10	mA
Power consumption	-	0.7	-	W
Welding temperature	-	260	-	℃
Storage temperature	-65	-	+150	℃

5.2 Recommended working conditions

Recommended operating conditions are shown in Table 5.

Table 5 Recommended working conditions

Parameter	Symbol	Min. value	Typical value	Max. value	Unit
Supply voltage	V_{CC}	4.75	-	5.25	V
Working temperature		-55	-	125	℃

5.3 DC Characteristics

The DC characteristics of TGS8588-P are shown in Table 6.

Table 6 TGS8588-P DC characteristics

Unless otherwise specified, the test conditions are: VCC=5.0V±5%, GND=0V, TA=-55~125℃

Parameter	Symbol	Test conditions	Min. value	Typical value	Max. value	Unit
ARINC input voltage 1 or 0 NULL common mode	V_{DIN} V_{NIN} V_{COM}	Differential voltage, pin3&4 referenced to ground	6.5 - -	10 - -	13 2.5 5.0	V V V
Digital input voltage high or low	V_{IH} V_{IL}		3.5	- -	1.5	V V
ARINC input impedance RINA to RINB RINA or RINB to ground or VCC	RDIFF RSUP	Power supply floating	30 19	75 40	- -	KΩ KΩ
Digital input current Source and drain	IIH IIL	V_{IN}=0V V_{IN}=5V	- -	- -	0.1 0.1	μA μA
Digital output drive current 1 0	IOH IOL	V_{OH}=4.6V V_{OL}=0.4V	3.6	-1.6 5.6	-0.8	mA mA

Current consumption Power saving mode while working	ICC1 ICC2	Pin 2, 8=0V; pin 3, 4 open circuit Pin 2, 8=5V; pin 3, 4 open circuit	- -	2.3 0.36	6.3 0.6	mA mA

5.4 AC characteristics

The AC characteristics of TGS8588-P are shown in Table 7.

Table 7 TGS8588-P AC characteristics

Unless otherwise specified, the test conditions are: VCC=5.0V±5%, GND=0V, TA=-55~125℃

Parameter	Symbol	Test conditions	Min. value	Typ. value	Max. value	Unit
Input transmission delay Output from high to low	T_{phlr}		-	600	800	ns
Output from low to high	T_{plhr}	Definition as shown in Figure 4, CL=50pF	-	600	800	ns
Output edge rise and fall time Output from high to low	tfr		-	50	80	ns
Output from low to high	trr		-	50	80	ns
Input capacitance 1 ARINC Differential Signaling	CAD		-	5	10	pF
ARINC signal ends to ground	CAS		-	-	10	pF
logic	CIN		-	-	10	pF

Note: 1. Design guarantee

TGS8588-P timing description is shown in Figure 4.

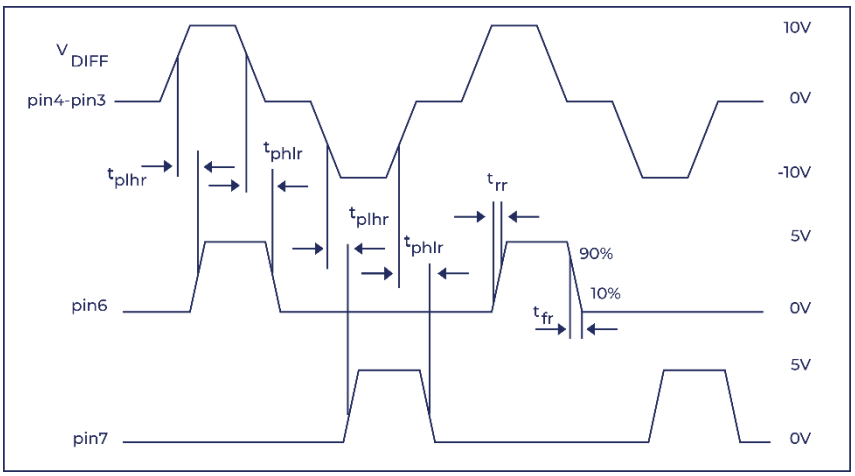


Figure 4 TGS8588-P timing description

6. Precautions for use

a) When using, it is recommended to use plastic tweezers to prohibit direct contact between the skin

and the product to prevent contamination and scratches on the product;

b) The product can be used directly cleaning is not recommended. If cleaning, it is forbidden to use acid, alkali, etc. for treatment. It is recommended to use ethanol, acetone, etc. After cleaning, make sure that there is no residue after cleaning.

c) Before welding, it is recommended to remove the gold from the leads. It is not recommended to solder directly on the lead gold plating. It is recommended to carry out tin enamel treatment to achieve the purpose of gold removal. The actual removal effect shall prevail. Please refer to standard QJ 3267;

d) Lead welding can be done by reflow welding or manual welding. Please refer to standards GJB 3243, QJ 3173, QJ3117 and SJ/T10670. It is forbidden for solder to flow to the bending and forming position of the lead, so that the lead can maintain its inherent buffering effect. During board-level use, lead deformation, tearing and falling off due to mismatch between lead material and circuit board should be avoided;

e) In order to ensure the reliability of board-level installation, it is recommended to use special glue to reinforce the device after lead welding. When reinforcing, be careful not to let the glue flow to the bend of the lead;

f) When operating or removing chips, anti-static measures must be taken, such as wearing anti-static gloves or anti-static bracelets;

g) When installing or removing the chip, pay attention to the direction of force application to ensure that the chip pins are evenly stressed. Do not use excessive force, which may damage the pins and render them unusable.