TGS32F031

Series 32-bit Microcontroller

Data sheet

1. Chip Introduction

1.1 Overview

The TGS32F031x6x series is our latest 32-bit general-purpose processor based on the ARM Cortex™ M0 core. The main applications are in the intelligent control market, such as power tools, aircraft models, small appliances, etc. The TGS32F031x6x series controllers have common peripherals, such as UART serial port, high-precision 12-bit ADC, watchdog timer (WDT), I2C bus interface, SPI interface, and 4 general-purpose timers; in addition, the TGS32F031x6x also integrates brushless DC motor control and motor control functions.

1.2 Main features

• High performance 32-bit ARM CPU core

ARM Cortex™-M0 processor running at up to 48 MHz

Single-cycle 32-bit hardware multiplier

Flexible NVIC interrupts

• Flash memory

32K capacity, 32-bit Flash data bus, supports high-performance application requirements

2K boot program area

• SRAM memory

4K bytes high-speed SRAM

• 16-bit PWM Timer Generator TIM1

Up to 6-channel PWM output with automatic dead-zone insertion

Hardware-based fault protection system

• Embedded system bootloader

Support Flash memory In-System-Program (ISP) and In-Application-Program (IAP)

• Flexible clock unit

Built-in 48MHz internal high-speed oscillator with ±5% accuracy

Built-in 32KHz watchdog oscillator

• Enhanced timer

2 basic timers and 2 enhanced timers

Basic timers support match interrupt function

Enhanced timers support match and capture interrupt functions

Enhanced timers support edge counting, gate counting, AB phase quadrature counting, trigger counting, symbol counting

• Analog peripherals

12-bit 1MHz ADC converter

Up to 8 channels

Supports software and hardware AD conversion trigger modes

• Rich communication interfaces and high-speed input/output ports (GPIO)

2 serial communication modules with 16-byte FIFO, supporting IrDA protocol

Extended SPI interface, supporting multiple protocols

I2C interface

Up to 27 high-speed GPIO interfaces

• Power management

Three power saving modes: sleep mode, deep sleep mode, power-down mode

Wake up the processor from deep sleep mode by configuring 8 pin ports

Supports brownout detection (BOD), two sets of detection points can generate brownout interrupt and forced reset respectively

Supports power-on reset (POR)

Integrated power management unit (PMU)

• Operating temperature range

Military grade (-55℃ ~ 105℃)

• 2.7V ~ 5.5V wide voltage operating range

• Package: TSSOP-20, QFN-20, QFN-28, QFN-32

2. Package pin information

2.1 TSSOP-20 package pin layout

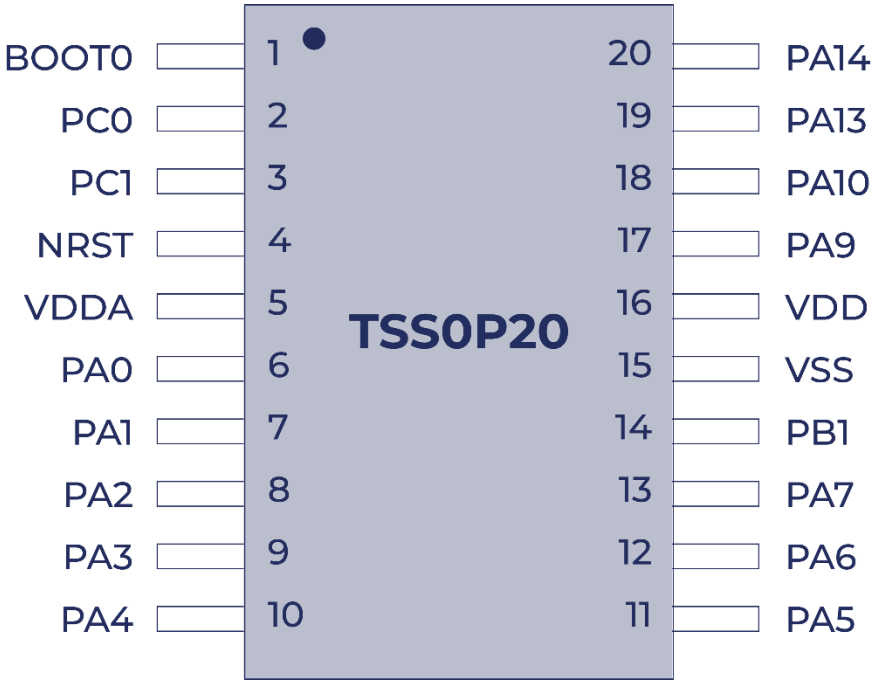

Figure 2-1 TSSOP-20 package pin layout

2.2 QFN-20 package pinout

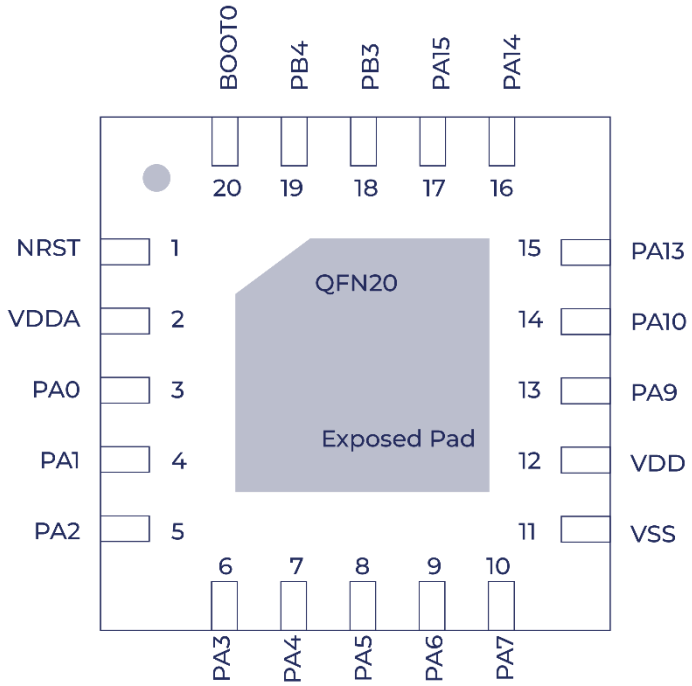

Figure 2-2 QFN-20 package pin layout

2.3 QFN-28 package pin layout

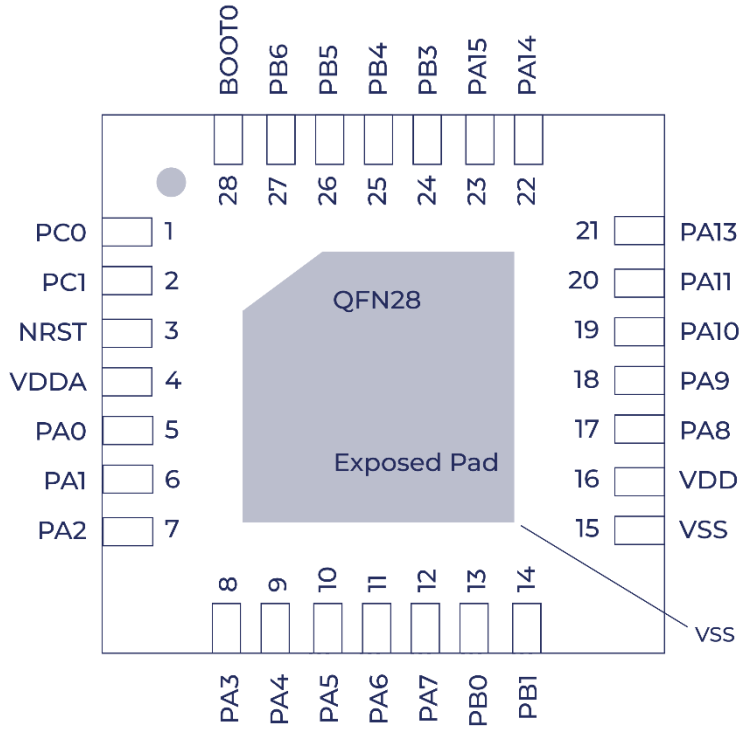

Figure 2-3 QFN28 package pin layout

2.4 QFN32 package pinout

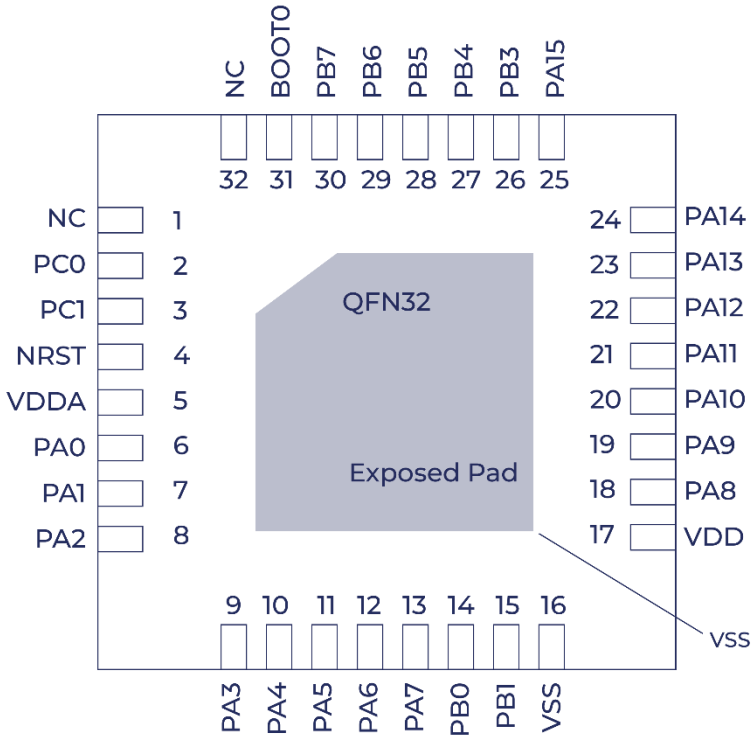

Figure 2-4 QFN32 package pin layout

2.5 Pin Function Description

Serial number	Name	Wake input	Pin type	Describe
1	BOOT0 (1)		I	BOOT0—Boot startup selection
			I/O	PC3—General purpose digital IO pin
2	PC0		I/O	PC0—General purpose digital IO pin
3	PC1		I/O	PC1—General purpose digital IO pin
4	NRST		I	NRST—RESET pin
			I/O	PC2—General purpose digital IO pin
5	VDDA		S	Analog power supply
6	PA0	●	I/O	PA0—General purpose digital IO pin
			I	ADC_IN0—ADC input channel 0
7	PA1	●	I/O	PA1—General purpose digital IO pin
			I	ADC_IN1—ADC input channel 1
8	PA2	●	I/O	PA2—General-purpose digital IO pin
			I	TIM3_CAP0—Capture input pin, channel 0, timer 3
			O	TIM3_MAT0—Match output pin, channel 0, timer 3
			O	TXD0—UART0 TX output pin
			I	ADC_IN2—ADC input channel 2
9	PA3	●	I/O	PA3—General purpose digital IO pin
			I	TIM3_CAP1—Capture input pin, channel 1, timer 3
			O	TIM3_MAT1—Match output pin, channel 1, timer 3
			I	RXD0—UART0 RX input pin
			I	ADC_IN3—ADC input channel 3
10	PA4	●	I/O	PA4—General purpose digital IO pin
			I	TIM3_CAP2—Capture input pin, channel 2, timer 3
			O	TIM3_MAT2—Match output pin, channel 2, timer 3
			I/O	SPI_SSEL—SPI chip select signal
			I	ADC_IN4—ADC input channel 4
11	PA5	●	I/O	PA5—General purpose digital IO pin
			I/O	SPI_SCK—SPI clock signal
			I	ADC_IN5—ADC input channel 5
12	PA6	●	I/O	PA6—General-purpose digital IO pin
			I	TIM1_FAULT—TIM1 PWM Fault in
			I	TIM2_CAP0—Capture input pin, channel 0, timer 2
			O	TIM2_MAT0—Match output pin, channel 0, timer 2
			I/O	SPI_MISO—SPI master input slave output pin
			I	ADC_IN6—ADC input channel 6
13	PA7	●	I/O	PA7—General-purpose digital IO pin
			O	TIM1_OUT1—TIM1 output pin channel 1
			I	TIM2_CAP1—Capture input pin, channel 1, timer 2
			O	TIM2_MAT1—Match output pin, channel 1, timer 2
			I/O	SPI_MOSI—SPI master output slave input pin
			I	ADC_IN7—ADC input channel 7
14	PB1		I/O	PB1—General purpose digital IO pin.
			O	TIM1_OUT5—TIM1 output pin channel 5
			I	TIM2_CAP3—Capture input pin, channel 3, timer 2
			O	TIM2_MAT3—Match output pin, channel 3, timer 2

15	VSS		S	land
16	VDD		S	Digital power
17	PA9		I/O	PA9—General purpose digital IO pin
			O	TIM1_OUT2—TIM1 output pin channel 2
			O	TXD0—UART0 TXD output pin
			I/O	I^2C_SCL—I^2C serial clock pin
18	PA10		I/O	PA10—General purpose digital IO pin
			O	TIM1_OUT4—TIM1 output pin channel 4
			I	RXD0—UART0 RXD input pin
			I/O	I^2C_SDA—I^2C serial data pin
19	PA13		I/O	PA13—General purpose digital IO pin
			I/O	SWD debug data pin
20	PA14		I/O	PA14—General purpose digital IO pin
			I/O	SWD debug clock pin
			O	TXD1—UART1 TX output pin

Note: (1) When the MCU is working normally, ensure that the Boot pin is at a low level or left floating.

Table 2-2 QFN20 package pin function description

Serial number	QFN-20	Wake input	Pin type	Describe
1	NRST		I	NRST—RESET pin
			I/O	PC2—General purpose digital IO pin
2	VDDA		S	Analog power supply
3	PA0	●	I/O	PA0—General purpose digital IO pin
			I	ADC_IN0—ADC input channel 0
4	PA1	●	I/O	PA1—General purpose digital IO pin
			I	ADC_IN1—ADC input channel 1
5	PA2	●	I/O	PA2—General-purpose digital IO pin
			I	TIM3_CAP0—Capture input pin, channel 0, timer 3
			O	TIM3_MAT0—Match output pin, channel 0, timer 3
			O	TXD0—UART0TX output pin
			I	ADC_IN2—ADC input channel 2
6	PA3	●	I/O	PA3—General purpose digital IO pin
			I	TIM3_CAP1—Capture input pin, channel 1, timer 3
			O	TIM3_MAT1—Match output pin, channel 1, timer 3
			I	RXD0—UART0 RX input pin
			I	ADC_IN3—ADC input channel 3
7	PA4	●	I/O	PA4—General purpose digital IO pin
			I	TIM3_CAP2—Capture input pin, channel 2, timer 3
			O	TIM3_MAT2—Match output pin, channel 2, timer 3
			I/O	SPI_SSEL—SPI chip select signal
			I	ADC_IN4—ADC input channel 4
8	PA5	●	I/O	PA5—General purpose digital IO pin

			I/O	SPI_SCK—SPI clock signal
			I	ADC_IN5—ADC input channel 5
9	PA6	●	I/O	PA6—General-purpose digital IO pin
			I	TIM1_FAULT—TIM1 PWM Fault in
			I	TIM2_CAP0—Capture input pin, channel 0, timer 2
			O	TIM2_MAT0—Match output pin, channel 0, timer 2
			I/O	SPI_MISO—SPI master input slave output pin
			I	ADC_IN6—ADC input channel 6
10	PA7	●	I/O	PA7—General-purpose digital IO pin
			O	TIM1_OUT1—TIM1 output pin channel 1
			I	TIM2_CAP1—Capture input pin, channel 1, timer 2
			O	TIM2_MAT1—Match output pin, channel 1, timer 2
			I/O	SPI_MOSI—SPI master output slave input pin
			I	ADC_IN7—ADC input channel 7
11	VSS		S	land
12	VDD		S	Digital power
13	PA9		I/O	PA9—General purpose digital IO pin
			O	TIM1_OUT2—TIM1 output pin channel 2
			O	TXD0—UART0 TXD output pin
			I/O	I^2C_SCL—I^2C serial clock pin
14	PA10		I/O	PA10—General purpose digital IO pin
			O	TIM1_OUT4—TIM1 output pin channel 4
			I	RXD0—UART0 RXD input pin
			I/O	I^2C_SDA—I^2C serial data pin
15	PA13		I/O	SWD debug data pin
			I/O	PA13—General purpose digital IO pin
16	PA14		I/O	SWD debug clock pin
			I/O	PA14—General purpose digital IO pin
			O	TXD1—UART1 TX output pin
17	PA15		I/O	PA15—General-purpose digital IO pin
			I/O	SPI_SSEL—SPI chip select pin
			I	RXD1—UART1 RX input pin
18	PB3		I/O	PB3—General purpose digital IO pin
			I/O	SPI_SCK—SPI serial clock pin
19	PB4		I/O	PB4—General purpose digital IO pin
			I/O	SPI_MISO—SPI master input slave output pin
			I	TIM2_CAP0—Capture input pin, channel 0, timer 2
			O	TIM2_MAT0—Match output pin, channel 0, timer 2
20	BOOT0[(1)]		I	BOOT0—Boot startup selection
			I/O	PC3—General purpose digital IO pin

Note: (1) When the MCU is working normally, ensure that the Boot pin is at a low level or left floating.

Table 2-3 QFN28 package pin function description

Serial number	QFN-28	Wake input	Pin type	Describe
1	PC0		I/O	PC0—General purpose digital IO pin
2	PCI		I/O	PC1—General purpose digital IO pin
3	NRST		I	NRST—RESET pin
			I/O	PC2—General purpose digital IO pin
4	VDDA		S	Analog power supply
5	PA0	●	I/O	PA0—General purpose digital IO pin
			I	ADC_IN0—ADC input channel 0
6	PA1	●	I/O	PA1—General purpose digital IO pin
			I	ADC_IN1—ADC input channel 1
7	PA2	●	I/O	PA2—General-purpose digital IO pin
			I	TIM3_CAP0—Capture input pin, channel 0, timer 3
			O	TIM3_MAT0—Match output pin, channel 0, timer 3
			O	TXD0—UART0 TX output pin
			I	ADC_IN2—ADC input channel 2
8	PA3	●	I/O	PA3—General purpose digital IO pin
			I	TIM3_CAP1—Capture input pin, channel 1, timer 3
			O	TIM3_MAT1—Match output pin, channel 1, timer 3
			I	RXD0—UART0 RX input pin
			I	ADC_IN3—ADC input channel 3
9	PA4	●	I/O	PA4—General purpose digital IO pin
			I	TIM3_CAP2—Capture input pin, channel 2, timer 3
			O	TIM3_MAT2—Match output pin, channel 2, timer 3
			I/O	SPI_SSEL—SPI chip select signal
			I	ADC_IN4—ADC input channel 4
10	PA5	●	I/O	PA5—General purpose digital IO pin
			I/O	SPI_SCK—SPI clock signal
			I	ADC_IN5—ADC input channel 5
11	PA6	●	I/O	PA6—General-purpose digital IO pin
			I	Tim1_fault—Tim1 PWM fault in
			I	TIM2_CAP0—Capture input pin, channel 0, timer 2
			O	TIM2_MAT0—Match output pin, channel 0, timer 2
			I/O	SPI_MISO—SPI master input slave output pin
			I	ADC_IN6—ADC input channel 6
12	PA7	●	I/O	PA7—General-purpose digital IO pin
			O	TIM1_OUT1—TIM1 output pin channel 1
			I	TIM2_CAP1—Capture input pin, channel 1, timer 2
			O	TIM2_MAT1—Match output pin, channel 1, timer 2
			I/O	SPI_MOSI—SPI master output slave input pin
			I	ADC_IN7—ADC input channel 7
13	PB0		I/O	PB0—General-purpose digital IO pin
			O	TIM1_OUT3—TIM1 output pin channel 3
			I	TIM2_CAP2—Capture input pin, channel 2, timer 2
			O	TIM2_MAT2—Match output pin, channel 2, timer 2
14	PB1		I/O	PB1—General purpose digital IO pin.
			O	TIM1_OUT5—TIM1 output pin channel 5
			I	TIM2_CAP3—Capture input pin, channel 3, timer 2

			O	TIM2_MAT3—Match output pin, channel 3, timer 2
15	VSS		S	Land
16	VDD		S	Digital power
17	PA8		I/O	PA8—General-purpose digital IO pin
			O	TIM1_OUT0—TIM1 output pin channel 0
			I	TIM3_CAP3—Capture input pin, channel 3, timer 3
			O	TIM3_MAT3—Match output pin, channel 3, timer 3
			O	CLKOUT—Internal clock output
18	PA9		I/O	PA9—General purpose digital IO pin
			O	TIM1_OUT2—TIM1 output pin channel 2
			O	TXD0—UART0 TXD output pin
			I/O	I^2C_SCL—I^2C serial clock pin
19	PA10		I/O	PA10—General purpose digital IO pin
			O	TIM1_OUT4—TIM1 output pin channel 4
			I	RXD0—UART0 RXD input pin
			I/O	I^2C_SDA—I^2C serial data pin
20	PA11		I/O	PA11—General purpose digital IO pin
			I	TIM2_CAP2—Capture input pin, channel 2, timer 2
			O	TIM2_MAT2—Match output pin, channel 2, timer 2
21	PA13		I/O	SWD debug data pin
			I/O	PA13—General purpose digital IO pin
22	PA14		I/O	SWD debug clock pin
			I/O	PA14—General purpose digital IO pin
			O	TXD1—UART1 TX output pin
23	PA15		I/O	PA15—General-purpose digital IO pin
			I/O	SPI_SSEL—SPI chip select pin
			I	RXD1—UART1 RX input pin
24	PB3		I/O	PB3—General purpose digital IO pin
			I/O	SPI_SCK—SPI serial clock pin
25	PB4		I/O	PB4—General purpose digital IO pin
			I/O	SPI_MISO—SPI master input slave output pin
			I	TIM2_CAP0—Capture input pin, channel 0, timer 2
			O	TIM2_MAT0—Match output pin, channel 0, timer 2
26	PB5		I/O	PB5—General purpose digital IO pin
			I/O	SPI_MOSI—SPI master output slave input pin
			I	TIM2_CAP1—Capture input pin, channel 1, timer 2
			O	TIM2_MAT1—Match output pin, channel 1, timer 2
27	PB6		I/O	PB6—General-purpose digital IO pin
			I/O	I^2C_SCL—I^2C serial clock pin
			O	TXD1—UART1 TX output pin
			I	TIM3_CAP0—Capture input pin, channel 0, timer 3
			O	TIM3_MAT0—Match output pin, channel 0, timer 3
28	BOOT0(1)		I	BOOT0—Boot startup selection
			I/O	PC3—General purpose digital IO pin

Note: (1) When the MCU is working normally, ensure that the Boot pin is at a low level or left floating.

Table 2-4 QFN32 package pin function description

Serial number	QFN-32	Wake input	Pin type	Describe
1	NC		S	Hanging in the air
2	PC0		I/O	PC0—General-purpose digital IO pin
3	PCI		I/O	PC1—General purpose digital IO pin
4	NRST		I	NRST—RESET pin
			I/O	PC2—General purpose digital IO pin
5	VDDA		S	Analog power supply
6	PA0	●	I/O	PA0—General purpose digital IO pin
			I	ADC_IN0—ADC input channel 0
7	PA1	●	I/O	PA1—General purpose digital IO pin
			I	ADC_IN1—ADC input channel 1
8	PA2	●	I/O	PA2—General purpose digital IO pin
			I	TIM3_CAP0—Capture input pin, channel 0, timer 3
			O	TIM3_MAT0—Match output pin, channel 0, timer 3
			O	TXD0—UART0 TX output pin
			I	ADC_IN2—ADC input channel 2
9	PA3	●	I/O	PA3—General purpose digital IO pin
			I	TIM3_CAP1—Capture input pin, channel 1, timer 3
			O	TIM3_MAT1—Match output pin, channel 1, timer 3
			I	RXD0—UART0 RX input pin
			I	ADC_IN3—ADC input channel 3
10	PA4	●	I/O	PA4—General purpose digital IO pin
			I	TIM3_CAP2—Capture input pin, channel 2, timer 3
			O	TIM3_MAT2—Match output pin, channel 2, timer 3
			I/O	SPI_SSEL—SPI chip select signal
			I	ADC_IN4—ADC input channel 4
11	PA5	●	I/O	PA5—General-purpose digital IO pin
			I/O	SPI_SCK—SPI clock signal
			I	ADC_IN5—ADC input channel 5
12	PA6	●	I/O	PA6—General-purpose digital IO pin
			I	TIM1_FAULT—TIM1 PWM Fault in
			I	TIM2_CAP0—Capture input pin, channel 0, timer 2
			O	TIM2_MAT0—Match output pin, channel 0, timer 2
			I/O	SPI_MISO—SPI master input slave output pin
			I	ADC_IN6—ADC input channel 6
13	PA7	●	I/O	PA7—General-purpose digital IO pin
			O	TIM1_OUT1—TIM1 output pin channel 1
			I	TIM2_CAP1—Capture input pin, channel 1, timer 2
			O	TIM2_MAT1—Match output pin, channel 1, timer 2
			I/O	SPI_MOSI—SPI master output slave input pin
			I	ADC_IN7—ADC input channel 7
14	PB0		I/O	PB0—General-purpose digital IO pin
			O	TIM1_OUT3—TIM1 output pin channel 3

Serial number	QFN-32	Wake input	Pin type	Describe
			I	TIM2_CAP2—Capture input pin, channel 2, timer 2
			O	TIM2_MAT2—Match output pin, channel 2, timer 2
15	PB1		I/O	PB1—General purpose digital IO pin.
			O	TIM1_OUT5—TIM1 output pin channel 5
			I	TIM2_CAP3—Capture input pin, channel 3, timer 2
			O	TIM2_MAT3—Match output pin, channel 3, timer 2
16	VSS		S	Land
17	VDD		S	Digital power
18	PA8		I/O	PA8—General-purpose digital IO pin
			O	TIM1_OUT0—TIM1 output pin channel 0
			I	TIM3_CAP3—Capture input pin, channel 3, timer 3
			O	TIM3_MAT3—Match output pin, channel 3, timer 3
			O	CLKOUT—Internal clock output
19	PA9		I/O	PA9—General purpose digital IO pin
			O	TIM1_OUT2—TIM1 output pin channel 2
			O	TXD0—UART0 TXD output pin
			I/O	I^2C_SCL—I^2C serial clock pin
20	PA10		I/O	PA10—General purpose digital IO pin
			O	TIM1_OUT4—TIM1 output pin channel 4
			I	RXD0—UART0 RXD input pin
			I/O	I^2C_SDA—I^2C serial data pin
21	PA11		I/O	PA11—General purpose digital IO pin
			I	TIM2_CAP2—Capture input pin, channel 2, timer 2
			O	TIM2_MAT2—Match output pin, channel 2, timer 2
22	PA12		I/O	PA12—General-purpose digital IO pin
23	PA13		I/O	SWD debug data pin
			I/O	PA13—General purpose digital IO pin
24	PA14		I/O	SWD debug clock pin
			I/O	PA14—General purpose digital IO pin
			O	TXD1—UART1 TX output pin
25	PA15		I/O	PA15—General purpose digital IO pin
			I/O	SPI_SSEL—SPI chip select pin
			I	RXD1—UART1 RX input pin
26	PB3		I/O	PB3—General-purpose digital IO pin
			I/O	SPI_SCK—SPI serial clock pin
27	PB4		I/O	PB4—General purpose digital IO pin
			I/O	SPI_MISO—SPI master input slave output pin
			I	TIM2_CAP0—Capture input pin, channel 0, timer 2
			O	TIM2_MAT0—Match output pin, channel 0, timer 2
28	PB5		I/O	PB5—General purpose digital IO pin
			I/O	SPI_MOSI—SPI master output slave input pin
			I	TIM2_CAP1—Capture input pin, channel 1, timer 2
			O	TIM2_MAT1—Match output pin, channel 1, timer 2

Serial number	QFN-32	Wake input	Pin type	Describe
29	PB6		I/O	PB6—General purpose digital IO pin
			I/O	I^2C_SCL—I^2C serial clock pin
			O	TXD1—UART1TX output pin
			I	TIM3_CAP0—Capture input pin, channel 0, timer 3
			O	TIM3_MAT0—Match output pin, channel 0, timer 3
30	PB7		I/O	PB7—General purpose digital IO pin
			I/O	I^2C_SDA—I^2C serial data pin
			I	RXD1—UART1 RX input pin
			I	TIM3_CAP1—Capture input pin, channel 1, timer 3
			O	TIM3_MAT1—Match output pin, channel 1, timer 3
31	BOOT0(1)		I	BOOT0—Boot startup selection
			I/O	PC3—General purpose digital IO pin
32	NC		S	Hanging in the air

Note: (1) When the MCU is working normally, ensure that the Boot pin is at a low level or left floating.

2.6 Peripheral Pin Description

To use MCU peripherals, you need to find the corresponding pins and set the pin functions through the IOCONFIG register. When the system is reset, the main SWD debug port and RESET reset function are the default settings, and all other pins are set to digital GPIO.

Table 2-5 Peripheral pin selection

Peripheral	Function name	TSSOP-20	QFN-20	QFN-28	QFN-32	Type	Optional pins		
ADC	AD0	√	√	√	√	I	PA0		
	AD1	√	√	√	√	I	PA1		
	AD2	√	√	√	√	I	PA2		
	AD3	√	√	√	√	I	PA3		
	AD4	√	√	√	√	I	PA4		
	AD5	√	√	√	√	I	PA5		
	AD6	√	√	√	√	I	PA6		
	AD7	√	√	√	√	I	PA7		
TIM2	TIM2_CAP0	√	√	√	√	I	PA6	PB4	
	TIM2_CAP1	√	√			I	PA7	PB5	
	TIM2_CAP2			√	√	I	PB0	PA11	
	TIM2_CAP3					I	PB1		
	TIM2_MAT0	√	√	√	√	O	PA6	PB4	
	TIM2_MAT1	√				O	PA7	PB5	
	TIM2_MAT2			√	√	O	PB0	PA11	

Peripheral	Function name	TSSOP-20	QFN-20	QFN-28	QFN-32	Type	Optional pins		
	TIM2_MAT3					O	PB1		
TIM3	TIM3_CAP0	√	√	√	√	I	PA2	PB6	
	TIM3_CAP1	√	√		√	I	PA3	PB7	
	TIM3_CAP2	√	√			I	PA4	PB8	
	TIM3_CAP3			√	√	I		PA8	
	TIM3_MAT0	√		√	√	O	PA2	PB6	
	TIM3_MAT1	√	√		√	O	PA3	PB7	
	TIM3_MAT2	√	√			O	PA4	PB8	
	TIM3_MAT3			√	√	O		PA8	
PWM	PWM_OUT0			√	√	O	PA8		
	PWM_OUT1	√	√	√	√	O	PA7		
	PWM_OUT2	√		√	√	O	PA9		
	PWM_OUT3			√	√	O	PB0		
	PWM_OUT4	√	√	√	√	O	PA10		
	PWM_OUT5	√		√	√	O	PB1		
	PWM_FAULT	√	√	√	√	I	PA6		
UART0	RXD0	√	√	√	√	I	PA3	PA10	
	TXD0	√	√	√	√	O	PA2	PA9	
UART1	RXD1			√	√	I	PA15	PB7	
	TXD1			√	√	O	PA14	PB6	
SPI	SSEL	√	√	√	√	I/O	PA4	PA15	
	SCK	√	√	√	√	I/O	PA5	PB3	
	MISO	√	√	√	√	I/O	PA6	PB4	
	MOSI	√	√	√	√	I/O	PA7	PB5	
I2C	SCL	√	√	√	√	I/O	PA9	PB6	
	SDA	√	√	√	√	I/O	PA10	PB7	
SWD	SWCLK	√	√	√	√	I	PA14		
	SWDIO	√	√	√	√	I/O	PA13		

3. System Block Diagram

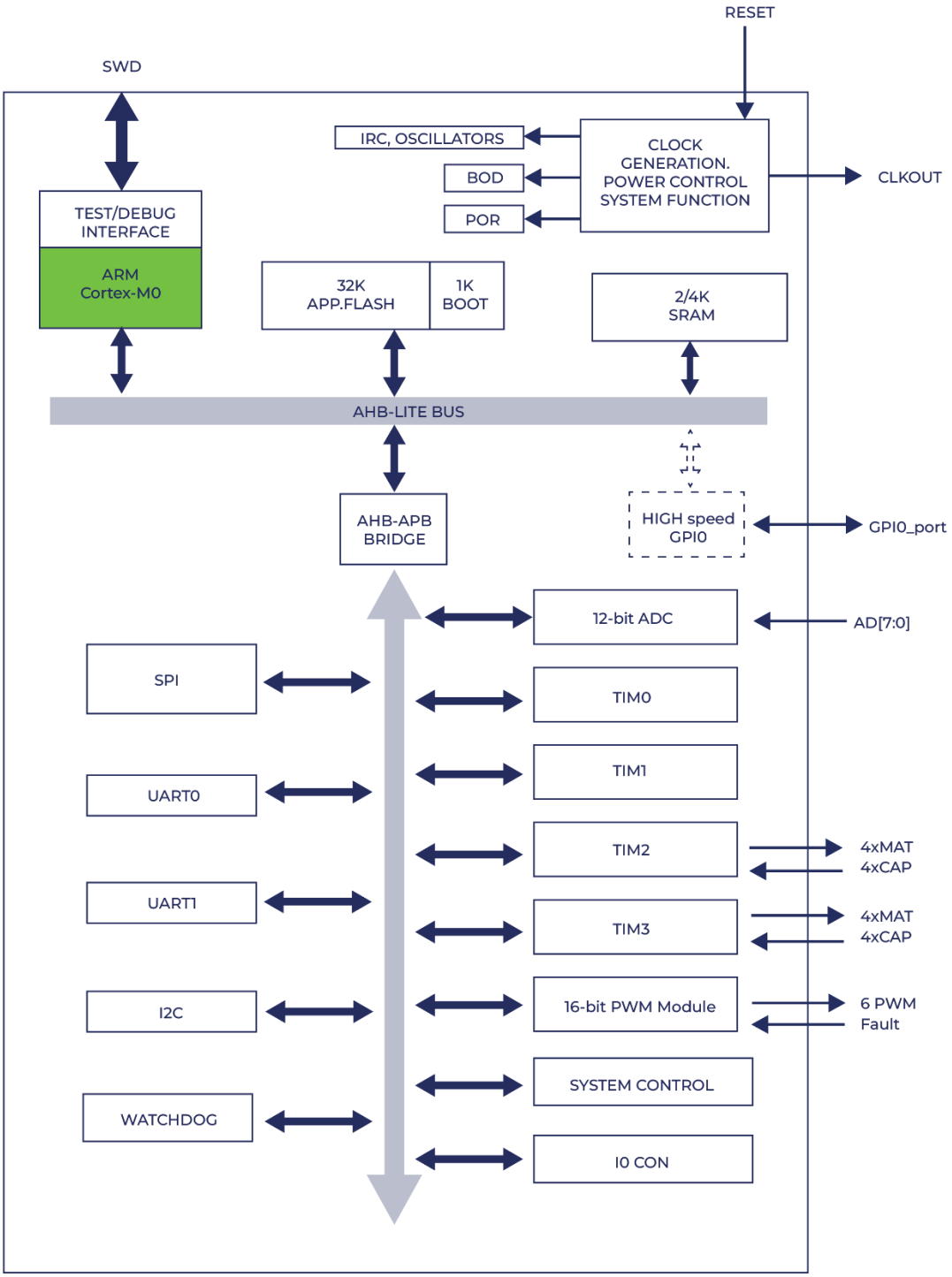

Figure 3-1 TGS32F031x6x block diagram

4. System Description

4.1 ARM Cortex™-M0 Core

The Cortex™ M0 processor is a 32-bit configurable multi-stage pipeline RISC processor with an embedded AMBA-Lite interface and a nested vector interrupt controller (NVIC). It has optional hardware debugging capabilities, can execute Thumb instructions, and is compatible with other Cortex-M series. It works in two modes: Thread mode and Handler mode. When a system exception occurs, it enters Handler mode. When returning from Handler mode, an exception return is executed. The system enters Thread mode when reset. Thread mode can also be entered when an exception returns.

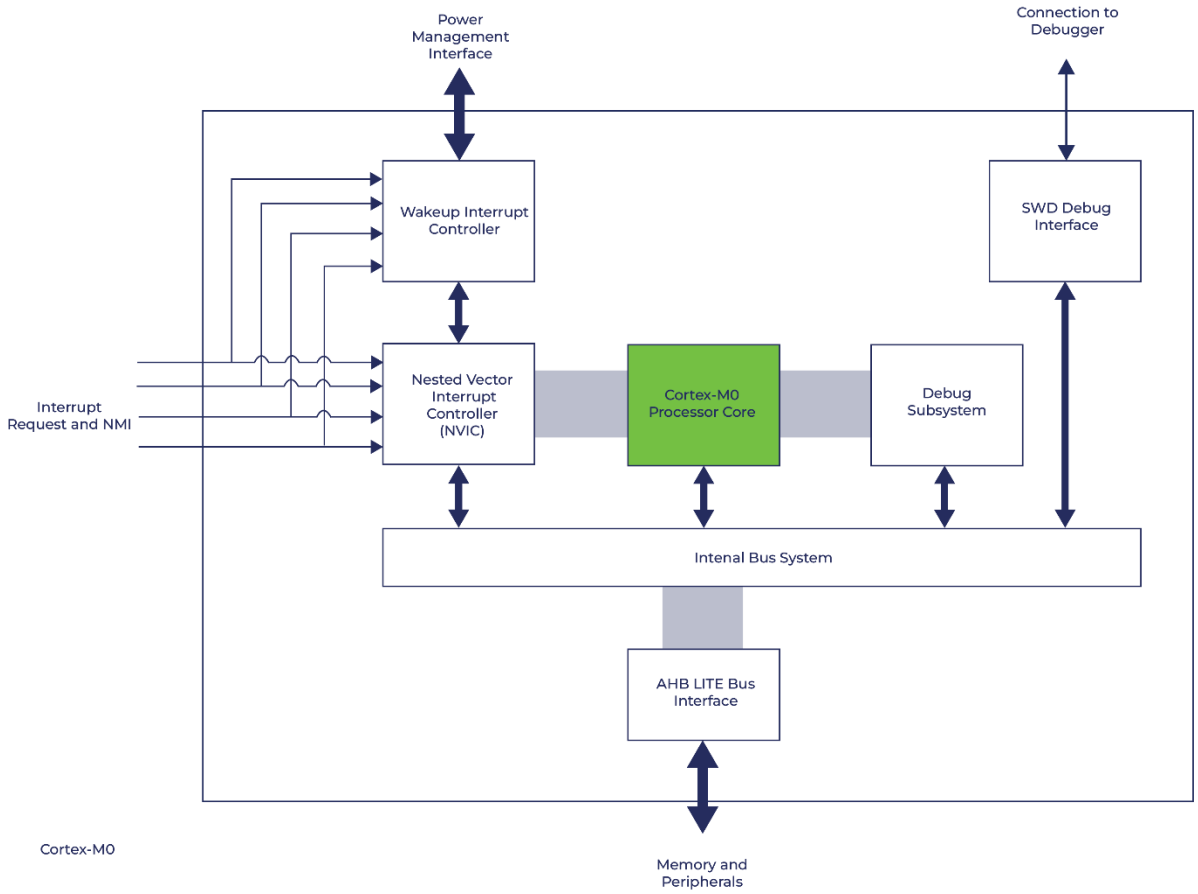

Figure 4-1 Cortex M0 core functional module diagram

ARM Cortex™-M0 processor features:

• ARMv6-M Thumb

• Thumb-2 technology

• ARMv6-M compatible 24-bit SysTick timer

• 32-bit hardware multiplier

• System interface supports little-endian data access

• Accurate and timely interrupt handling capability

• Load, store multiple data and multi-cycle multiplication instructions can be terminated and restarted to achieve fast interrupt handling

• Exception compatibility mode of C application binary interface (C-ABI). The ARMv6-M mode

allows users to implement interrupt handling using pure C functions

• Use interrupt wakeup (WFI) and event wakeup (WFE) instructions to enter low-power sleep mode, or exit sleep mode from interrupt

• NVIC features:

– 32 external interrupts, each with 4 levels of priority

– Dedicated non-maskable interrupt (NMI)

– Supports both level and pulse interrupt triggers

– Interrupt Wake-up Controller (WIC) to support very low power sleep modes

• Debug support

– Four hardware breakpoints

– Two watchpoints

– Program Counter Sample Register (PCSR) for non-intrusive code analysis

– Single-step and vector capture capabilities

• Bus Interface:

– Single 32-bit AMBA-3 ABH-Lite system interface that provides simple integration to all system peripherals and memories.

– Single 32-bit slave port with DAP (Debug Access Port) support

4.2 Memory Mapping

TGS32F031x6x memory address space supports 4GB size. It is divided into: boot area, Flash memory area, SRAM area, system-owned peripheral area, APB peripheral area and AHB peripheral area. The system-owned peripheral area is reserved for the M0 core.

The AHB peripheral area occupies 2M space and can support up to 128 peripherals. Among them, GPIO port and CRC are AHB peripherals. The APB peripheral area is a 512K space. Each APB peripheral is allocated 16K space. All peripheral control registers are read and written using word addressing, and users cannot access the high or low bytes of registers individually. The boot area has 2KB space for storing boot programs, ISP and IAP functions. TGS32F031x6x allows up to 32KB of user Flash space and 4KB of SRAM space. Both Flash and SRAM data buses use 32-bit operation.

The following figure is the memory address space allocation diagram of TGS32F031x6x:

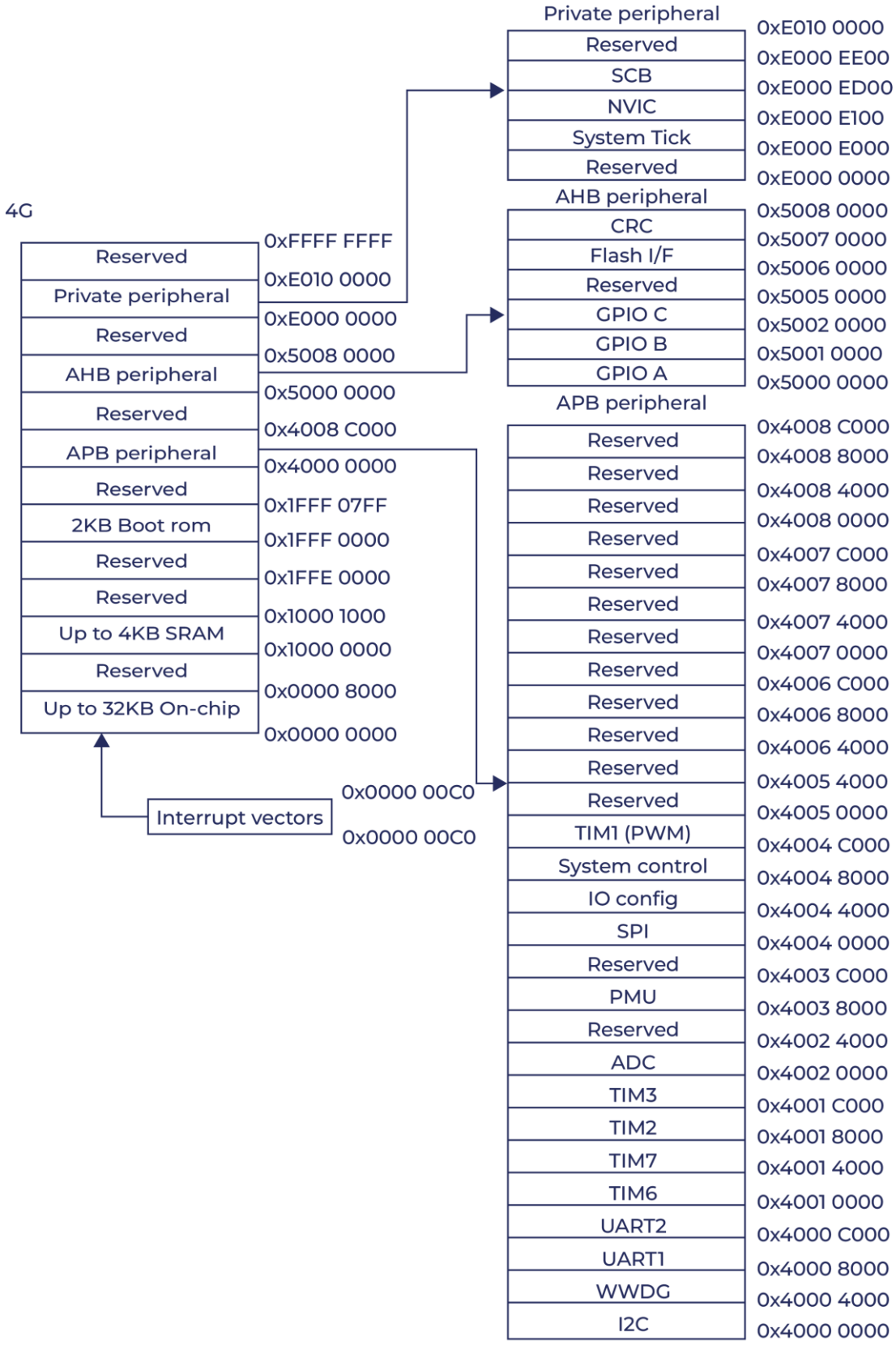

Figure 4-2 Memory allocation diagram

4.3 System Clock Control

Compared with other MCUs, TGS32F031x6x has a very flexible clock control system. Users can configure the clock according to different application requirements to achieve the highest performance and optimized energy management. The following figure is an overview of the clock system of TGS32F031x6x.

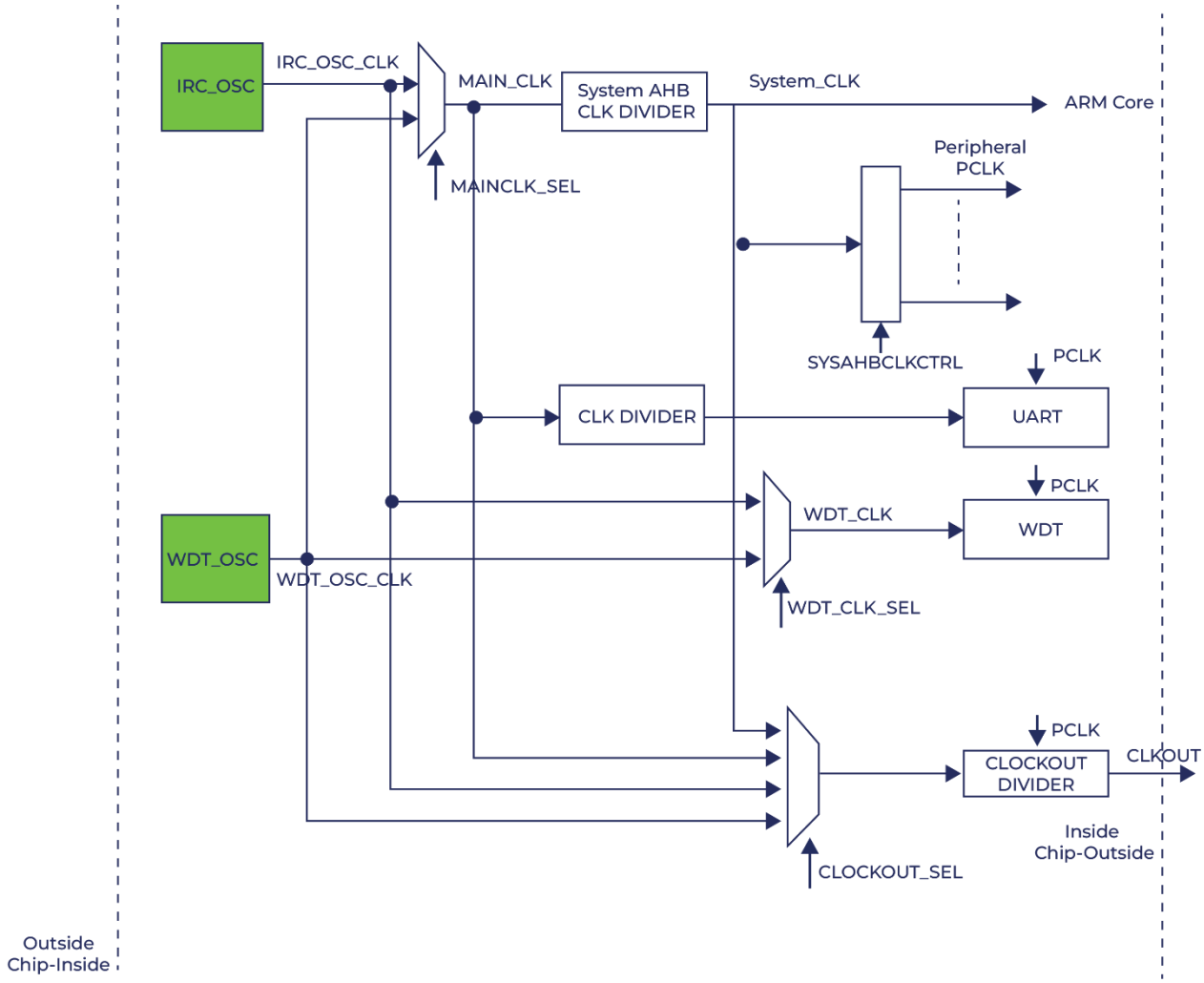

Figure 4-3 Clock system block diagram

After system reset, TGS32F031x6x will always use IRC clock until the user switches to another clock source using software. In this way, the system can execute the boot program at a known frequency without an external crystal.

SYSAHBCLKCTRL register is used for memory and peripheral clock supply control. UART1/2 has its own independent clock divider to obtain the operating clock from the main clock. The watchdog operating clock can come from the WDT oscillator or the main clock. The main clock, IRC, internal crystal oscillator and watchdog oscillator clock can all be output from the CLKOUT pin.

4.4 System Reset

The following events can trigger a system reset:

• Power-On Reset (POR)

• RESET# pin reset signal (low level)

• Watchdog timeout reset

• Brownout detection reset (BOD)

• Software reset

• Power-down mode wake-up reset

The RESET# pin is a Schmitt trigger input pin. A valid reset signal requires a signal width of not less than 15us.

Reset can be caused by any reset source. As long as the operating voltage is at an available level, the IRC will be started and remain valid. When the external reset is invalid, the oscillator is running and the flash controller is initialized.

When POR, BOD reset, external reset and watchdog reset occur, the following initialization will be performed:

• Start IRC. After the IRC startup time, the IRC provides a stable clock output for the system.

• Execute the boot program in the ROM area. The boot program will initialize the system and then jump into the user program.

When the external reset is invalid, the processor executes the boot area program mapped to address 0, and all processor and peripheral registers are assigned initial values.

4.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex™-M0 core. It allows the CPU to react to interrupts in the shortest possible time. The main features are:

• Short interrupt response latency.

• Handle system exceptions and peripheral interrupts.

• Support 32 interrupt vectors.

• Four programmable interrupt response priority levels.

• Generate software interrupts.

• Configurable non-maskable interrupt source (NMI).

The following table lists all system and peripheral interrupt sources. Each peripheral can generate 1 to multiple interrupts to the interrupt vector controller. Each interrupt may have multiple interrupt sources.

Table 4-1 Interrupt vector source and vector table

Exception code	IRQ number	Offset address	Exception type	Priority	Describe
		0x00	SP value		
1		0x04	Reset	-3 Superlative	
2	-14	0x08	NMI	-2	
3	-13	0x0C	HardFault	-1	
10~4		0x10~0x28	Reserve		

11	-5	0x2C	SVCall	Configurable	
13~12		0x30~0x34	Reserve		
14	-2	0x38	PendSV	Configurable	
15	-1	0x3C	SysTick	Configurable	
16	0	0x40	wake-up interrupt	Configurable	In deep sleep mode, PA0~PA11 generates wake-up interrupts
17	1	0x44	TIM1 fault interrupt	Configurable	
18	2	0x48	I2C	Configurable	SI status change
19	3	0x4C	TIM6	Configurable	Match 0~3
20	4	0x50	TIM7	Configurable	Match 0~3
21	5	0x54	TIM2	Configurable	Match 0~3 Capture 0~3
22	6	0x58	TIM3	Configurable	Match 0~3 Capture 0~3
23	7	0x5C	UART1	Configurable	TX FIFO empty/half empty RX FIFO half full/full Receive parity error Receive buffer overflow
24	8	0x60	UART2	Configurable	TX FIFO empty/half empty RX FIFO half full/full Receive parity error Receive buffer overflow
25	9	0x64	ADC	Configurable	
26	10	0x68	WWDG	Configurable	Watchdog interrupt (WDINT)
27	11	0x6C	BOD	Configurable	Power-off detection interrupt
28	12	0x70	PA	Configurable	GPIO port 0 interrupt status
29	13	0x74	PB	Configurable	GPIO port 1 interrupt status
30	14	0x78	PC	Configurable	GPIO port 2 interrupt status
31	15	0x7C	RTC	Configurable	RTC interrupt
32	16	0x80	SPI	Configurable	Tx FIFO half empty Rx FIFO half full Rx not empty interrupt Rx full interrupt
33	17	0x84	TIM1 PWM_Reload	Configurable	
34-48	18-32	-	-	-	-

4.6 IO Configuration

To achieve pin multiplexing, TGS32F031x6x designs an IOCON configuration register for each pin to define the pin function. The I/O configuration register controls the electrical characteristics of the pin. The following functions can be configured:

• Pin function

• Pin mode: internal pull-up resistor enabled/disabled

• Pin driver

• ADC pin analog input or digital mode switching

• IO pin anti-interference filtering

4.7 TIM1 (PWM) module

TGS32F031x6x can provide an independent event-driven pulse width modulation module PWM. The PWM module can be configured as 3 pairs of complementary outputs, 6 independent outputs or complementary and independent mixed PWM signal outputs (such as 2 pairs of complementary outputs, 2 independent outputs). It also supports edge-aligned and center-aligned modes with a duty cycle of 0~100%.

The PWM module uses a 16-bit counter, and its accuracy is one clock cycle when edge-aligned and 2 clock cycles when center-aligned. The clock cycle is determined by the PWM clock source PWM_PCLK (system clock), the prescaler register, and the modulus value. When the PWM signal is configured as a complementary output, the PWM has an automatic dead zone insertion function. Each PWM output can be controlled by a PWM generator, a system timer, an ADC conversion result, a GPIO input, and software. Asymmetric PWM can also allow the PWM duty cycle to be changed every half cycle without software involvement.

4.8 GPIO

In the QFN32 package, TGS32F031x6x provides up to 27 GPIO pins. The main features are:

• Digital pins can be defined as input or output by software

• Pin read and write can be masked

• Multiple pins can be set and cleared with one instruction

• Pin output is inverted

• Each pin can be used as an external interrupt signal

• Programmable interrupt trigger conditions and interrupt priority

• All GPIO pins are configured as input pins with pull-up resistors after reset

4.9 ADC Module

TGS32F031x6x supports 8-channel 12-bit high-resolution ADC to meet customer application requirements. The main functions are as follows:

• 1MHz conversion rate, 12-bit A/D converter

• Supports 8 external AD channel sampling conversions

• The module supports low power consumption power down

• ADC measurement range 0~VDDA.

• Supports burst mode ADC conversion

• Configurable ADC conversion trigger source - input pin level conversion or timer match signal.

• Each ADC converter has 8 registers to store conversion results, thereby reducing interrupt burden.

4.10 UART Interface

TGS32F031x6x provides 2 UART peripherals with 16-byte FIFO buffers: UART1, UART2. The serial interfaces support infrared transmission (IrDA) protocol function. Each UART has an independent clock divider so that it is not affected by the system clock.

• UART communication uses a fixed data communication format: 1 start bit, 8 data bits, 1 stop bit, optional parity check, no hardware handshake.

• The user can set the division value of the BAUDDIV register to generate a baud rate suitable for different applications.

4.11 SPI Interface

TGS32F031x6x supports extended SPI (Serial Peripheral interface) interface, which can support standard SPI operation and is compatible with 4-wire SSI (Synchronous Serial Interface). This interface allows multiple master and slave bus modes, but at the same time, only one master/slave is sending data. Data transmission supports 4-bit to 16-bit full-duplex mode. The main functions are as follows:

• Supports standard SPI, compatible with 4-wire SSI

• Synchronous serial communication

• Supports master/slave mode

• 8-frame deep FIFO (First In First Out) buffer

• Data length per frame 4-bit to 16-bit

4.12 I^2C Interface

I^2C is a two-wire serial communication interface that is compatible with the I^2C bus. It can support both master and slave modes of I^2C communication. The main functions are as follows:

• Compatible with standard I2C master and slave modes

• Programmable clock frequency supports different I2C data transfer rates

• Supports bidirectional data transmission in slave mode

• Serial clock synchronization enables devices with different transfer rates to communicate over a serial bus

• Supports rates up to 1MHz

• Can be set to up to 4 different slave addresses.

4.13 Timer

TGS32F031x6x has two basic and enhanced multi-function 16-bit timer/counters. The main functions of each timer/counter are as follows:

• Timer/counter with preset frequency division

• Enhanced timer/counter, supporting edge counting, gated counting, quadrature counting, trigger counting, and signed counting

• Capture timer, capable of triggering interrupts and signal measurements

• 4 match registers, capable of timing event interrupts

4.14 Flash/SRAM Memory and ISP/IAP Function

TGS32F031x6x has up to 32KB Flash and 4KB SRAM user memory space. Flash supports two programming methods: In-System Programming (ISP) and In-Application Programming (IAP). Users can call ISP/IAP functions through the TGS32F031x6x bootloader interface.

Flash user code protection is implemented through 2 levels of security. See the relevant section of the user manual for details.

4.15 Watchdog Timer

The watchdog timer is used to interrupt and reset the system after the user program fails to feed the watchdog. Using a programmable watchdog timer, the user can change the timer time to cope with different applications. The watchdog timer has the following main functions:

• Independent 32KHz watchdog clock oscillator with programmable frequency

• Watchdog timer can trigger interrupt or reset

• Support low power mode

4.16 Power and Power Management

TGS32F031x6x supports multiple power consumption control functions. In the normal operating mode of the processor, the power supply and clock of the selected peripherals can be optimized to reduce system power consumption. In addition, the processor has three special low power consumption modes: sleep mode, deep sleep mode and power-down mode.

4.16.1 Sleep Mode

In sleep mode, the clock to the ARM Cortex™-M0 core is turned off and all instruction execution is suspended until the system is reset or woken up by an interrupt.

For peripherals, their clocks are controlled by registers and can generate interrupts, thereby waking up the processor and restarting the execution of instructions. Sleep mode can reduce the system dynamic power consumption generated by the processor, memory, and internal buses. The processor status and registers, peripheral registers, memory data, and the logic state of the pins remain unchanged in sleep mode.

4.16.2 Deep Sleep Mode

In deep sleep mode, the processor system clock is turned off, and all analog modules (except BOD, watchdog oscillator and RTC crystal) are powered off. The power-on state of BOD, watchdog oscillator and RTC crystal is determined by the register configuration. The RTC module and RTC crystal operate normally in deep sleep mode unless the RTC is powered off. In deep sleep mode, the system can minimize the dynamic power consumption caused by the processor, memory, peripherals, related controllers and buses. Of course, the state and registers of the processor, peripheral registers, memory data and the logic state of the pins remain unchanged.

4.16.3 Power-down mode

In Power-down mode, the power and clock to the entire microcontroller are turned off, except for the WAKEUP pin.

If the RTC was enabled before entering Power-down mode, the RTC and RTC oscillator will continue to run in Power-down mode. If the RTC is not needed in Power-down mode, the RTC can be disabled to minimize power consumption.

In Power-down mode, the contents of the SRAM and registers will not be retained, except for a small amount of data that can be stored in the 4 32-bit backup registers of the PMU module.

In Power-down mode, all functional pins remain in their original state, except for the WAKEUP pin.

4.17 SWD Debug Port

TGS32F031x6x provides SWD debug interface to support standard ARM Serial Wire Debug mode. Functions include:

• Direct access to all memories, registers and peripherals for debugging.

• No target resources are required during the debugging phase.

• 4 breakpoints. 4 instruction breakpoints, which can be used to remap instruction addresses of code patches. 2 data comparators, which can be used to remap patch addresses to literal values.

2 data watchpoints, which can be used as trace triggers.

5. Electrical specifications

5.1 Absolute Maximum Ratings

Table 5-1 Absolute ratings

Name	Symbol	Smallest	Maximum	Unit
Working voltage	V_{SS}	-0.3		V
	V_{DD}	+3.0	+5.5	V
	V_{DDA}	+3.0	+5.5	V
I/O Input Voltage	V_{IN}	-3.0	+5.5	V
Storage temperature	T_S	-55	+150	℃
Maximum input current of V_{DD} pin	I_{DD}		50	mA
Maximum output current of V_{SS} pin	I_{SS}		50	mA
Maximum input sink current for I/O pins		-10		mA
Maximum output source current of I/O pins			10	mA
Electrostatic protection voltage	V_{ESD}		2000	V

5.2 Electrical Characteristics Table

Unless otherwise specified, the electrical characteristics shall be as specified in Table 1 and shall apply over the full temperature range.

Table 5-2 Electrical characteristics

(1) Chip parameter table

Symbol/ Name	Parameter description	Test conditions	Minimum value	Maximum value	Unit
V_{DD}	Supply voltage	I/O pin power supply (5V)	4.5	5.5	V
		I/O pin power supply (3.3V)	2.7	3.6	V
Standard port pinout					
I_{IL}	Low level input current	V_I=0V;	-5	20	μA
I_{IH}	High level input current	V_I=V_{DD}	-20	5	μA
V_{IH}	High level input		0.65V_{DD}	-	V
V_{IL}	low level input		-	0.5	V

V_{OH}	High level output	5V, normal output in high drive mode I_{Load}=12mA Normal output in low drive mode I_{Load}=6mA	2.7	V_{DD}	V
		3.3V, normal output in high drive mode I_{Load}=6mA Normal output in low drive mode I_{Load}=3mA	2.7	V_{DD}	V
V_{OL}	Low level output	5V, normal output in high drive mode I_{Load}=12mA Normal output in low drive mode I_{Load}=6mA	0	0.5	V
		3.3V, normal output in high drive mode I_{Load}=6mA Normal output in low drive mode I_{Load}=3mA	0	0.5	
I_{OH}	High level output current	5V, normal output in high drive mode Normal output in low drive mode	5 3	15 10	mA
		3.3V, normal output in high drive mode Normal output in low drive mode	5 3	15 10	mA
I_{OL}	Low level output current	5V, normal output in high drive mode Normal output in low drive mode	5 3	15 10	mA
		3.3V, normal output in high drive mode Normal output in low drive mode	5 1	10 8	mA
Rpup Rpdn	Pull-up/pull-down current[1]	5V/3.3V, guaranteed by design	20	100	KOhm

Note: [1] Guaranteed by design.

Table 5-3 Electrical characteristics

(2) BOD parameters

Symbol/Name	Parameter description	Test conditions	Minimum value	Maximum value	Unit
Vth	Threshold voltage[1]	Interrupt voltage			
		Insert interrupt	2.8	2.9	V
		Undo interrupt	2.85	2.95	V
		Reset voltage			
		The system enters reset state	0	2.65	V
		The system exits the reset state	2.5	2.75	V

Note: [1] Guaranteed by design.

Table 5-4 Electrical characteristics

(3) ADC parameters (T_A=-55℃～+105℃; V_{DD}=3.0V～5.5V)

Symbol/Name	Parameter description	Test conditions	Minimum value	Maximum value	Unit
-	Resolution		10	12	Bit
V_{IA}	Analog input voltage		0	V_{DDA}	V
Cin	Analog input capacitive impedance[8]		0	30	pF
DNL	Differential linearity error[1][2][3]	-	-1.0	1.5	LSB
INL	Integral linearity error[1][4][5]	-	-2.0	2.0	LSB
E_O	Offset error[1][5][8]	-	-3.0	3.0	LSB

E_G	Gain error[1][6]	-	-	±1.0	LSB
E_T	Absolute value error[1][7]	-	-	3	LSB
CLK	Clock frequency[8]		0.6	16	MHz
t_{ADC}	Conversion time[8]		12	16	Clock
$f_{c(ADC)}$	ADC conversion frequency		0	1000	KSPS

Note:

[1] Test conditions: V_{SS}=0V, V_{DD}=2.7V～5.5V.

[2] The ADC transfer function is monotonic and has no missing codes.

[3] Differential linearity error (DNL) is defined as the difference between the actual quantization step and the ideal value corresponding to 1LSB.

[4] Integral linearity error (INL) indicates the error value of the point where the error between the corresponding analog value and the true value is the largest among all numerical points, that is, the distance where the output value deviates the most from the linearity.

[5] Offset error (EO) refers to the absolute error between the actual and ideal value lines.

[6] Gain error (EG) refers to the relative error between the actual conversion value and the ideal value lines after removing the offset error.

[7] Absolute error (ET) refers to the maximum error between the actual conversion value and the ideal value lines of the uncalibrated ADC.

[8] Guaranteed by design.

Table 5-5 Electrical characteristics

(4) Flash memory parameters (T_A = -55 ° C ~ +105 ° C; V_{DD} = 3.0 V ~ 5.5 V)

Symbol/Name	Parameter description	Test conditions	Minimum value	Maximum value	Unit
t_{erase}	Erase time	One sector (1K bytes)[1]	4.5	5	ms
t_{prog}	Programming time	One word (4 bytes)[1]	18	20	μs
N_{cyc}	Erasing and programming lifespan[2]		8,000	100,000	Second-rate
t_{ret}	Data retention time[2]		8	10	Year

Note:

[1] Erase and programming times are only valid within the normal life cycle of Flash.

[2] Guaranteed by design.

Table 5-6 Electrical characteristics

(5) SPI pin parameters working in SPI mode (T_A=-55℃～+105℃)

Symbol/Name	Parameter description	Test conditions	Minimum value	Maximum value	Unit
$t_{cy(clk)}$	Clock cycle	Send [1]	500	10000	ns
		Take over	500	10000	ns
SPI master					
t_{DS}	Data creation time	SPI mode[2][5]	15	10000	ns
t_{DH}	Data retention time	SPI mode[2][5]	1	10000	ns
$t_{v(Q)}$	Data output valid time	SPI mode[2][5]	0	10	ns
$t_{h(Q)}$	Data output hold time	SPI mode[2][5]	0	10000	ns
SPI slave					
t_{DS}	Data creation time	SPI mode[3][4][5]	4	10000	ns
t_{DH}	Data retention time	SPI mode[3][4][5]	3xtcy(PCLK)+4	10000	ns
$t_{v(Q)}$	Data output valid time	SPI mode[3][4][5]	0	3xtcy(PCLK)+5	ns
$t_{h(Q)}$	Data output hold time	SPI mode[3][4][5]	0	3xtcy(PCLK)+5	ns

Note:

[1] tcy(clk), the clock cycle is inferred from the bit frequency of SPI.

[2] Tamb=-55℃～105℃;V_{DD}(3V3)=3.0V～3.6V;V_{DD}(IO)=3.0V～3.6V.

[3] tcy(clk)=12xtcy(PCLK). [4]Tamb=25℃;V_{DD}(3V3)=3.3V;V_{DD}(IO)=3.3V.

[5] Guaranteed by design.

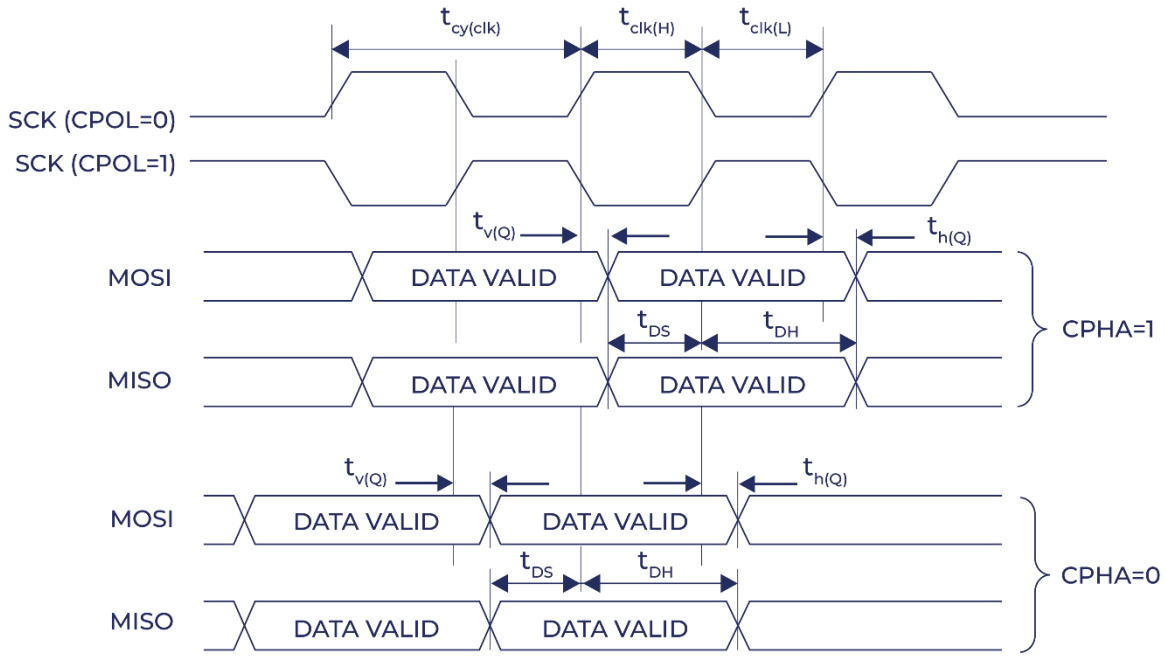

Figure 5-1 SPI Master Mode

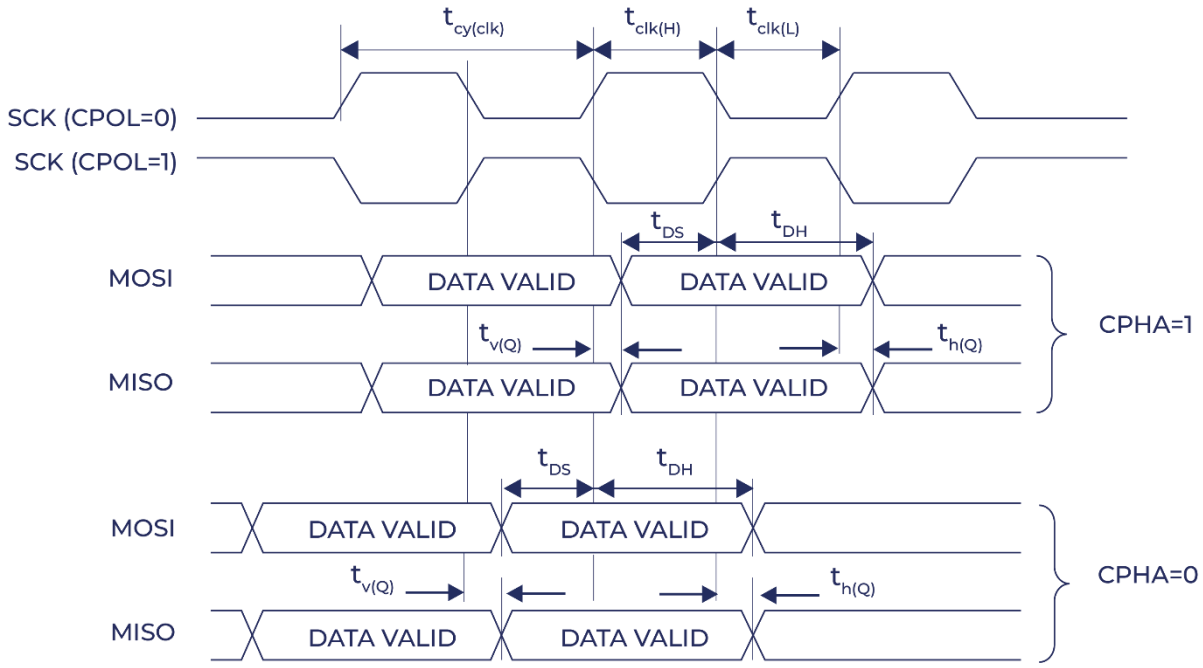

Figure 5-2 SPI slave timing

Table 5-7 Electrical characteristics

(6) I²C bus pin parameters T_A = -55℃～+105℃

Symbol/Name	Parameter description	Test conditions	Minimum value	Maximum value	Unit
f_{SCL}	SCL clock frequency	-	0	1	MHz
t_f	Falling edge time[2][3][4][7]	-	0	120	ns
t_{LOW}	SCL clock low level period	-	0.5	10000	μs
t_{HIGH}	SCL clock high level period	-	0.26	10000	μs
$t_{HD;DAT}$	Time keeping time[1][2][5][7]	-	0	10000	s
$t_{SU;DAT}$	Time Establishment Time[6][7]	-	50	10000	ns

Notes:

[1] tHD;DAT is the data hold time, starting from the falling edge of SCL; this time is the same for both data transmission and acknowledgement.

[2] While ensuring the VIH(min) of the SCL signal, the internal SDA signal of the device must be held for at least 300ns to cope with the undefined SCL falling edge time.

[3] Cb = total capacitive load on a single data bus, in pF.

[4] The maximum SDA and SCL tf time is 300ns. However, during the SDA time output phase, the maximum tf time of SDA is 250ns.

[5] The maximum tHD;DAT time can be between 3.45s and 0.9s, but must be less than the maximum data transmission tVD;DAT/tVD;ACK time.

[6] tSU;DAT is the setup time relative to the rising edge of SCL and applies to both data transmission and acknowledgement.

[7] Guaranteed by design.

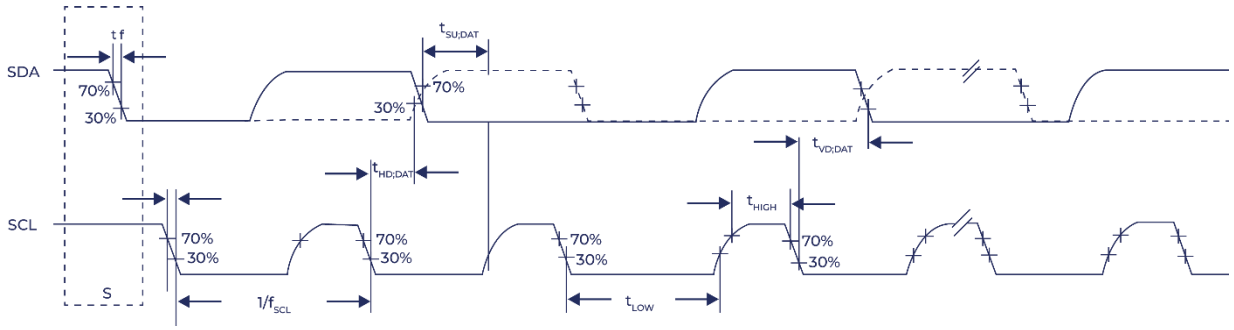

Figure 5-3 I²C bus timing

6. Package size

6.1 TSSOP-20 Package

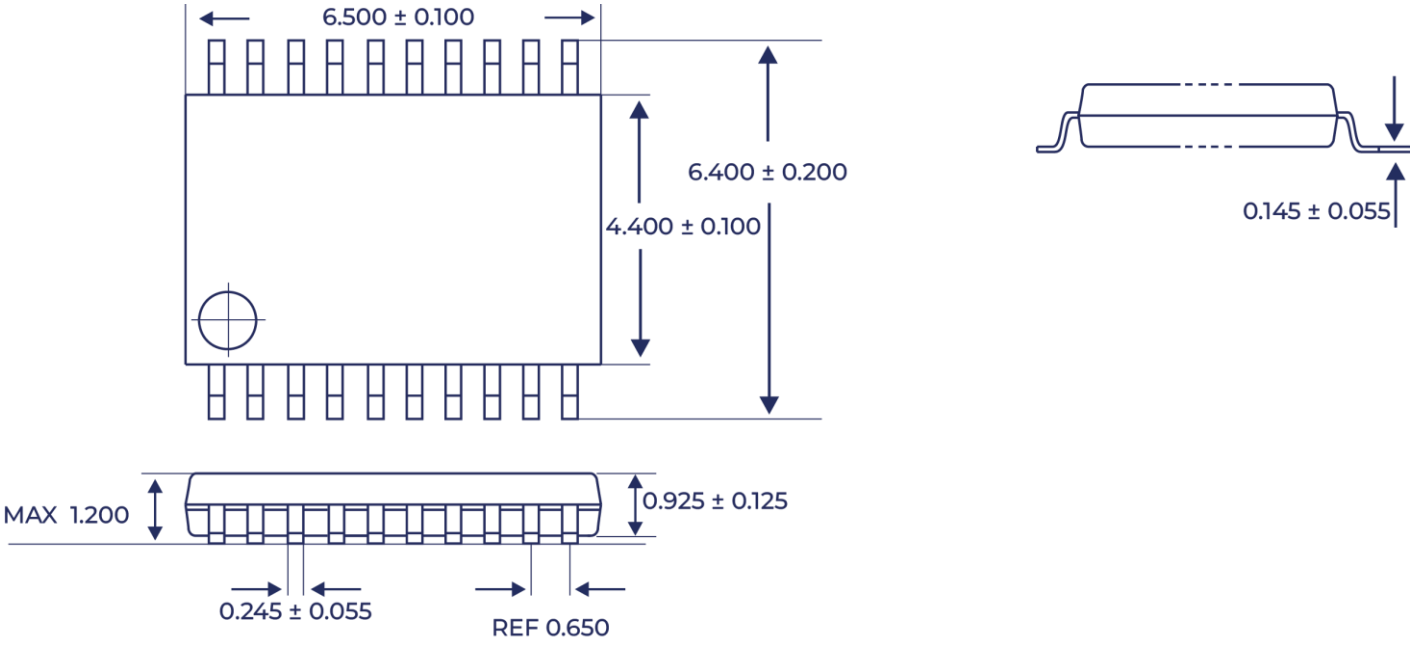

Figure 6-1 TSSOP-20 package dimensions

6.2 QFN-20 Package

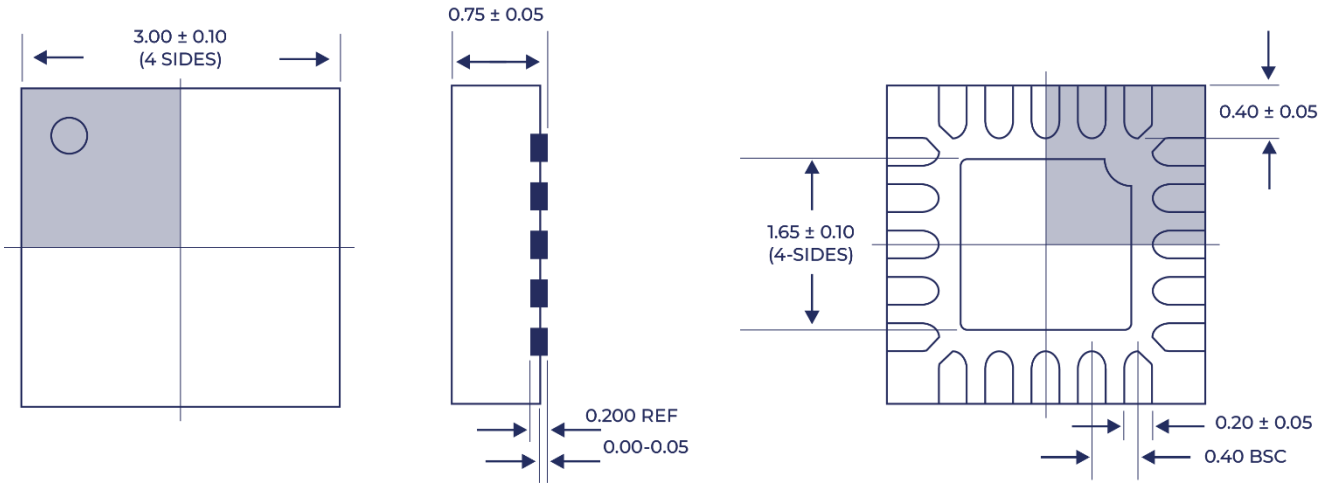

Figure 6-2 QFN20 package dimensions

6.3 QFN28 Package

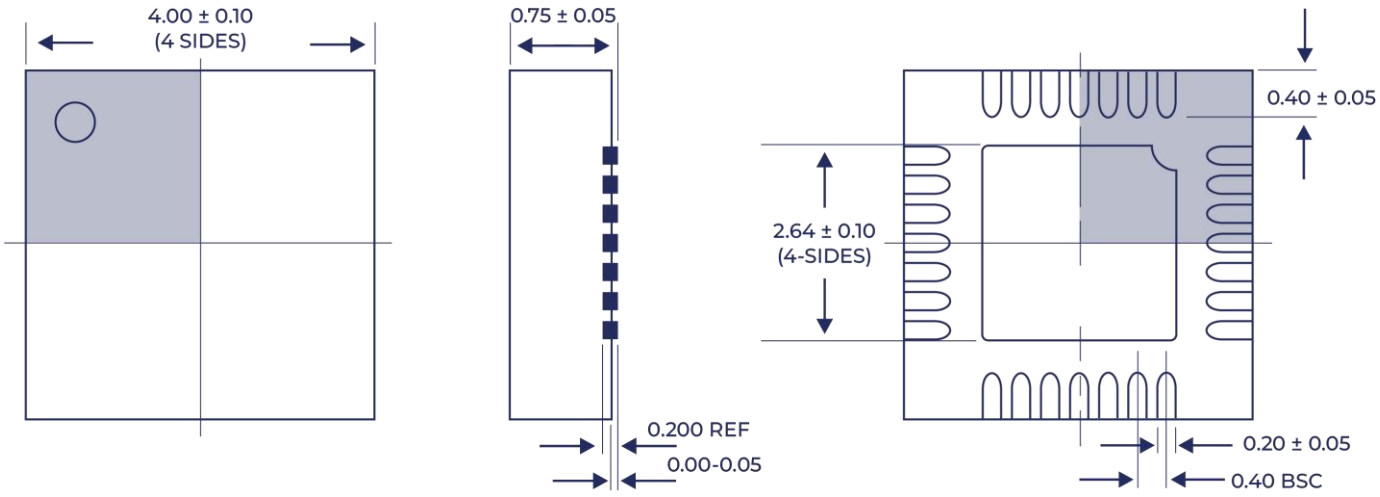

Figure 6-3 QFN28 package dimensions

6.4 QFN32 Package

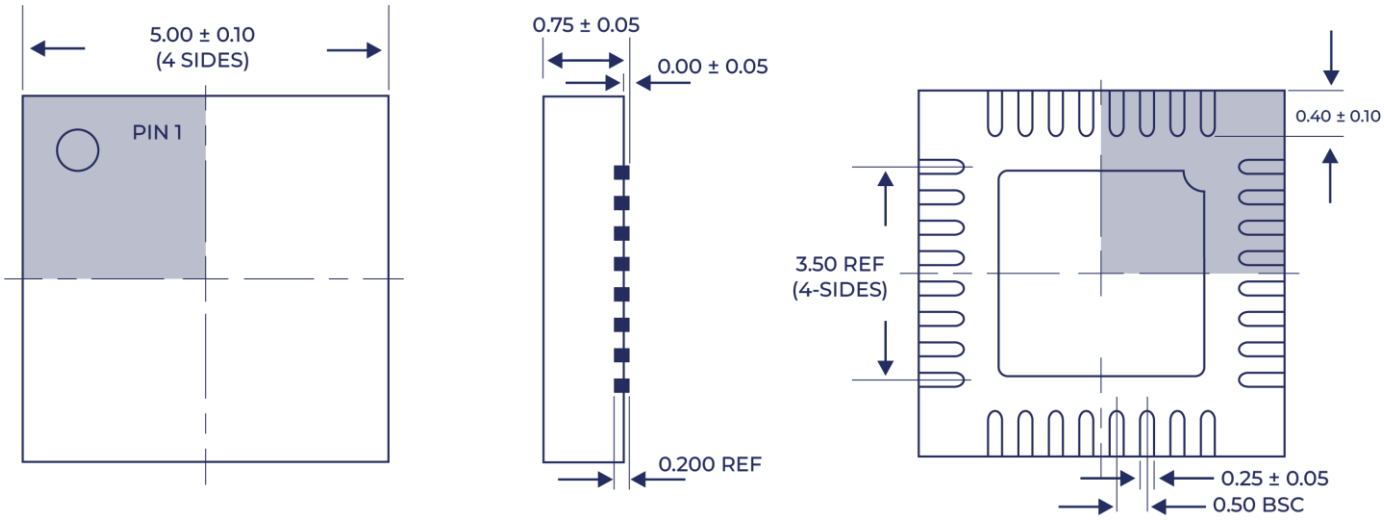

Figure 6-4 QFN32 package dimensions

7. Ordering Information

Table 7-1 Selection list

Serial number	Model	Package	Number of pins	Flash	SRAM
1	TGS32F031F6P	TSSOP-20	20	32K	4K
2	TGS32F031F6U	QFN-20	20	32K	4K
3	TGS32F031J6U	QFN-28	28	32K	4K
4	TGS32F031K6U	QFN-32	32	32K	4K