TGS1573

1553B Monolithic Dual Transceiver

Data sheet

1. Description

The TGS1573 is low power CMOS dual transceivers designed to meet the requirements of the MIL-STD-1553 specification.

The transmitter section of each bus takes complementary CMOS / TTL Manchester II bi- phase data and converts it to differential voltages suitable for driving the bus isolation transformer. Separate transmitter inhibit control signal are provided for each transmitter.

The receiver section of each bus converts the 1553 bus bi-phase differential data to complementary CMOS / TTL data suitable for input to a Manchester decoder. Each receiver has a separate enable input, which forces the receiver outputs to logic "0".

TGS1573 can pin-to-pin replace HI-1573.

2. Features

- Compliant to MIL-STD-1553A and B, ARINC 708A
- Data rate up to 1Mbps
- Power supply voltage range 3.3V±5%
- Operating Temperature range -55°C ~ +125°C

3. Technical Description

3.1 Pin configurations

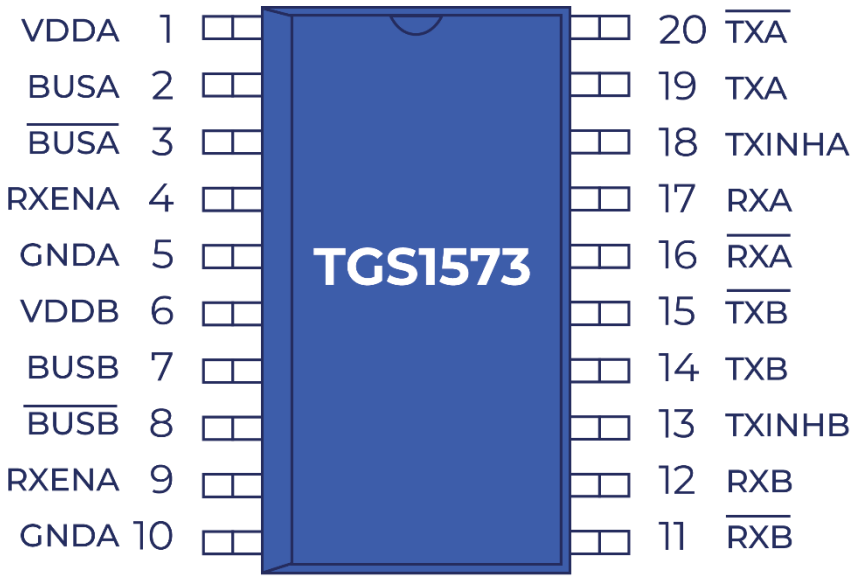


Fig.1 20-pin ESOP-20

3.2 Pin Description

Table 1 TGS1573 Pin Description

Pin	Symbol	Function	Description
1	VDDA	Power supply	+3.3-volt power for transceiver A
2	BUSA	Analog	MIL-STD-1533 bus driver A, positive signal
3	$\overline{\text{BUSA}}$	Analog	MIL-STD-1553 bus driver A, negative signal
4	RXENA	Digital input	Receiver A enable. If low, forces RXA and RXA low
5	GNDA	Power supply	Ground for transceiver A
6	VDDB	Power supply	+3.3-volt power for transceiver B
7	BUSB	Analog	MIL-STD-1533 bus driver B, positive signal
8	$\overline{\text{BUSB}}$	Analog	MIL-STD-1553 bus driver B, negative signal
9	RXENB	Digital input	Receiver B enable. If low, forces RXB and RXB low
10	GNDB	Power supply	Ground for transceiver B
11	$\overline{\text{RXB}}$	Digital output	Receiver B output, inverted
12	RXB	Digital output	Receiver B output, non-inverted
13	TXINHB	Digital input	Transmit inhibit, bus B. If high BUSB, BUSB disabled
14	TXB	Digital input	Transmitter B digital data input, non-inverted
15	$\overline{\text{TXB}}$	Digital input	Transmitter B digital data input, inverted
16	$\overline{\text{RXA}}$	Digital output	Receiver A output, inverted
17	RXA	Digital output	Receiver A output, non-inverted
18	TXINHA	Digital input	Transmit inhibit, bus A. If high BUSA, BUSA disabled
19	TXA	Digital input	Transmitter A digital data input, non-inverted
20	$\overline{\text{TXA}}$	Digital input	Transmitter A digital data input, inverted

3.3 Functional Description

The TGS1573 family of data bus transceivers contain differential voltage source drivers and differential receivers. They are intended for applications using a MIL-STD-1553 A/B data bus. The device produces a trapezoidal output waveform during transmission.

3.3.1 Transmitter

Data input to the device's transmitter section is from the complementary CMOS inputs TXA/B and TXA/B. The transmitter accepts Manchester II bi-phase data and converts it to differential voltages on BUSA/Band BUSA/B. The transceiver outputs are either director transformer-coupled to the MIL- STD-1553 data bus. Both coupling methods produce a nominal voltage on the bus of 7.5 voltspeak to peak.

The transmitter is automatically inhibited and placed in the high impedance state when both TXA/B and TXA/B are driven with the same logic state. A logic "1" applied to the TXINHA/B input will force the transmitter to the high impedance state, regardless of the state of TXA/Band TXA/B.

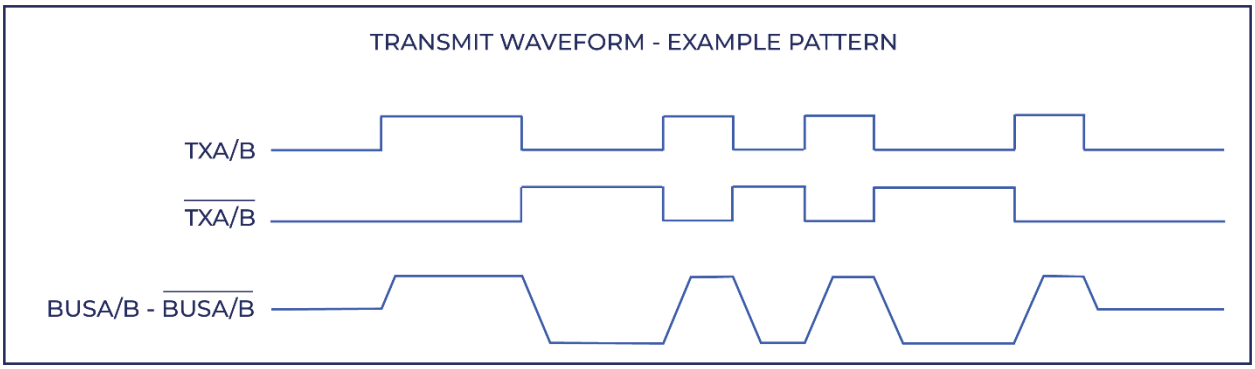


Fig. 2 Transmit Wave

3.3.2 Receiver

The receiver accepts bi-phase differential data from the MIL- STD-1553 bus through the same director transformer- coupled interface as the transmitter.

The receiver's differential input stage drives a filter and threshold comparator that produces CMOS data at the RXA/B and RXA/B output pins. When the MIL-STD-1553 bus is idle and RXENA or RXENB are high, RXA/B will be logic "0". The receiver outputs are forced to the bus idle state (logic «0») when RXENA or RXENB is low.

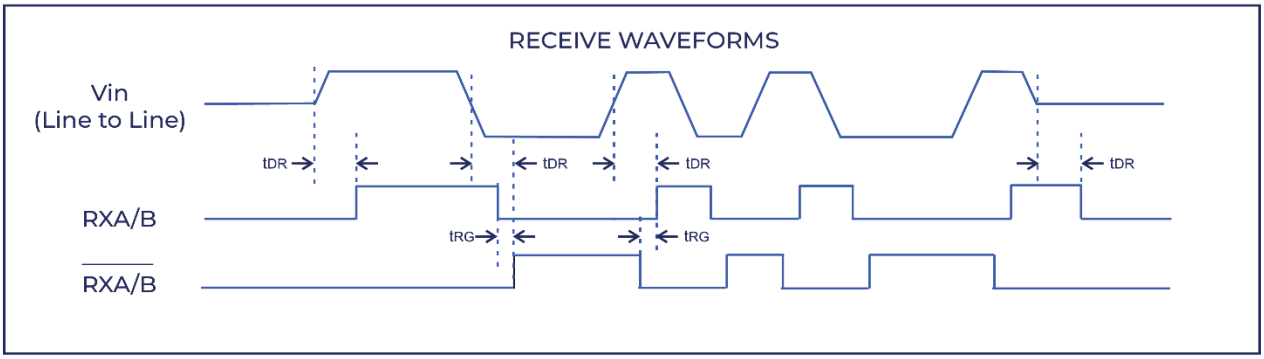


Fig. 3 Receive Waveform

3.3.3 MIL-STD-1553 Bus Interface

A direct-coupled interface (see Figure 5) uses a 1:2.5 ratio isolation transformer and two 55-ohm isolation resistors between the transformer and the bus.

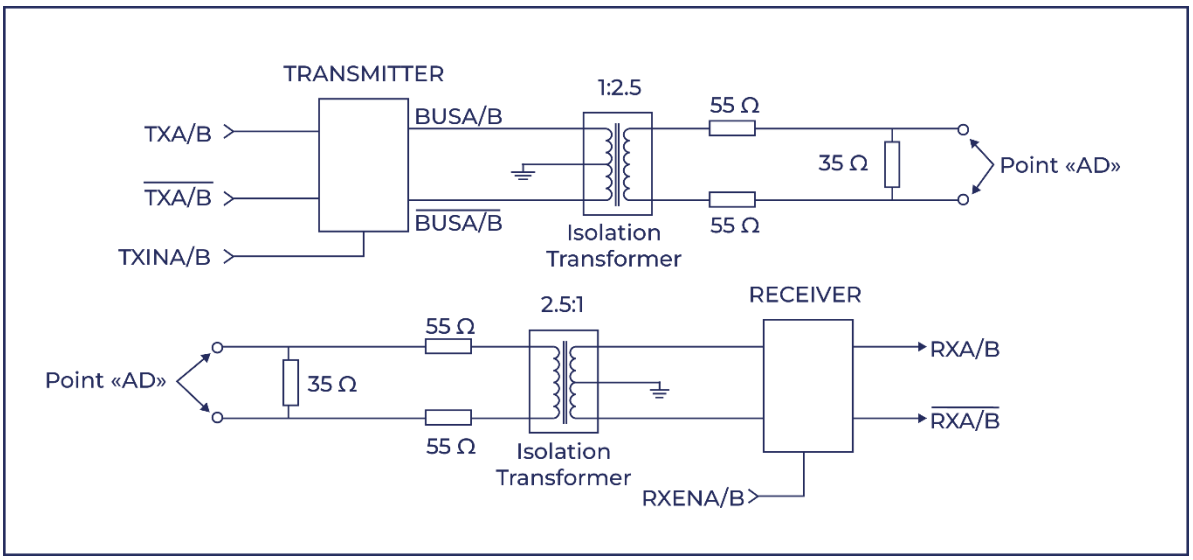


Fig. 4 Direct Coupled Test Circuit

In a transformer-coupled interface (see Figure 6), the transceiver is connected to a 1:1.79 isolation transformer which in turn is connected to a 1:1.4 coupling transformer. The transformer- coupled method also requires two coupling resistors equal to 75% of the bus characteristic impedance (Zo) between the coupling transformer and the bus.

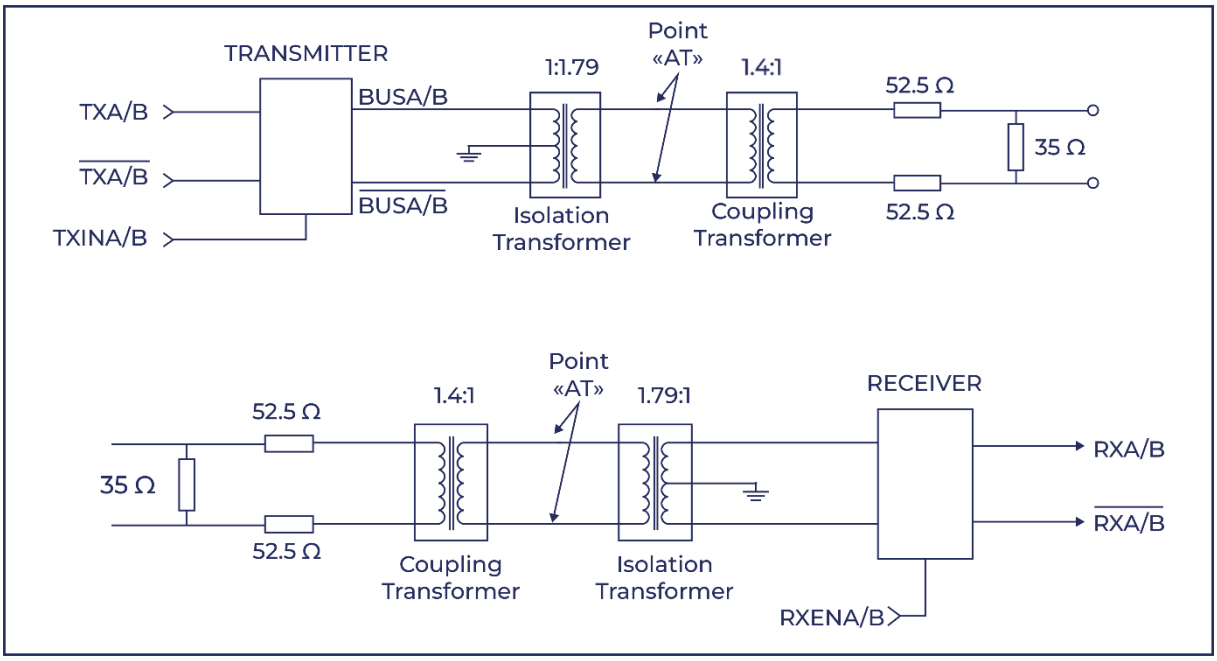


Fig. 5 Transformer Coupled Test Circuit

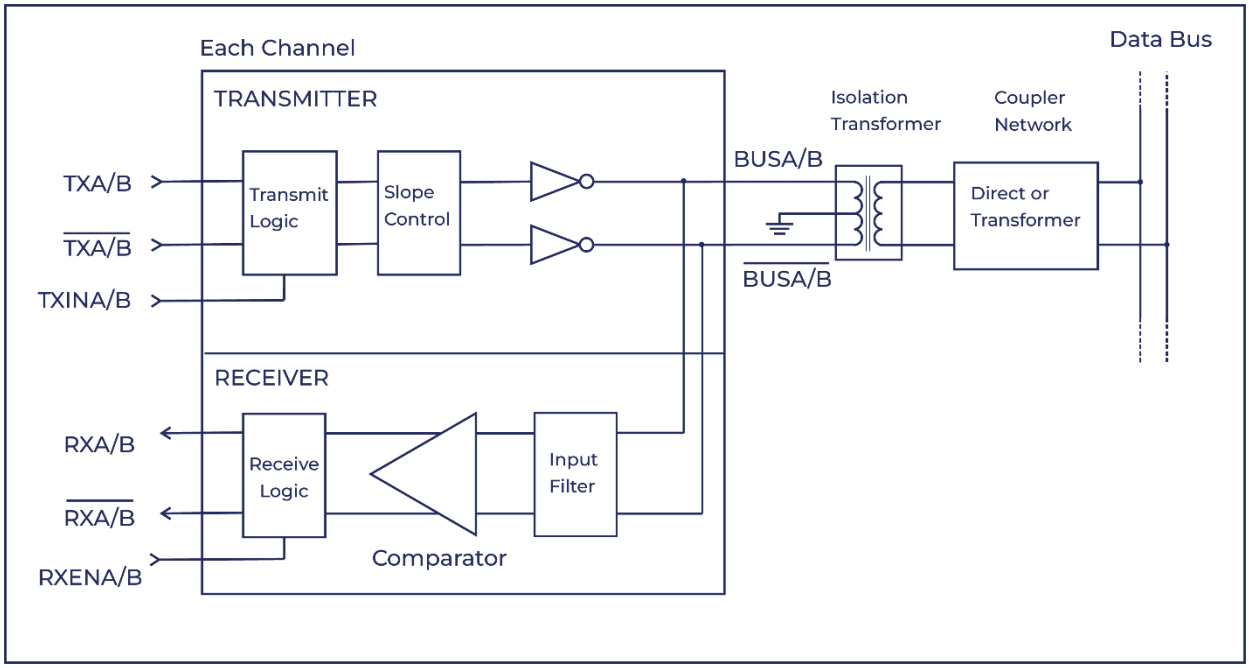


Fig. 6 Block diagram

3.5 Absolute maximum ratings (1)

- Supply voltage: V_D (V to +5V)
- Logic input voltage range: V_{IN} (-0.3V to +3.6V)
- Receiver differential voltage: 50 VP-P
- Driver peak output current: 1.0A
- Storage Temperature: -65°C to +150°C
- Solder Reflow Temperature: +300°C (10s)
- Operating Temperature: -55°C to +125°C

(1) Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

3.6 Parameters

3.6.1 DC Electrical characteristics

V_{DD} = 3.3V, -55°C ≤ T_A ≤ +125°C

Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
Operating Voltage	V_{DD}		3.15	3.30	3.45	V
Total Supply Current	I_{CC1}	Not Transmitting	-	10	17	mA
	I_{CC2}	Transmit one bus @ 50% duty cycle		250	450	mA
	I_{CC3}	Transmit one bus @ 100 % duty cycle		500	900	mA

Parameters		Symbol	Condition	Min.	Typ.	Max.	Units
Thermal Resisters		R_{JA}	T_A 125℃	-	-	15.34	℃/W
Power Dissipation		P_{D1}	Not Transmitting	-	0.033	0.060	W
		P_{D2}	Transmit one bus @ 100 % duty cycle		0.475	0.550	W
Min. Input Voltage (HI)		V_{IH}	Digital inputs	70%	-	-	V_{DD}
Max. Input Voltage (LO)		V_{IL}	Digital inputs	-	-	30%	V_{DD}
Min. Input Current (HI)		I_{IH}	Digital inputs	-	-	20	μA
Max. Input Current (LO)		I_{IL}	Digital inputs	-20	-	-	μA
Min. Output Voltage (HI)		V_{OH}	I_{OUT} = -1.0mA，Digital inputs	90%	-	-	V_{DD}
Max. Output Voltage (LO)		V_{OL}	I_{OUT} = -1.0mA，Digital inputs	-	-	10%	V_{DD}
RECEIVER (Measured at Point «AD» in Figure 5 unless otherwise specified)							
Input resistance		R_{IN}	Differential (at chip pins)	7	-	-	KΩ
Input resistance		C_{IN}	Differential	-	-	5	pF
Common mode rejection ratio		CMRR		40	-	-	dB
Input Level		V_{IN}	Differential	-	-	9	Vp-p
Input common mode voltage		V_{ICM}		-5.0	-	5.0	V-pk
Threshold Voltage - Direct-coupled	Detect	V_{THD}	1 Mhz Sine Wave Measured at Point «**AD**» in Figure 5	1.15	-	-	Vp-p
	No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$	-	-	0.28	Vp-p
Theshold Voltage - Transformer-coupled	Detect	V_{THD}	1 Mhz Sine Wave Measured at Point «**AD**» in Figure 5	0.86	-	-	Vp-p
	No Detect	V_{THND}	No pulse at RXA/B, $\overline{RXA/B}$	-	-	0.20	Vp-p
TRANSMITTER (Measured at Point «AD» in Figure 5 unless otherwise specified)							
Output Voltage	Direct coupled	V_{OUT}	35Ω load	6.0	-	9.0	Vp-p
	Transformer coupled	V_{OUT}	70Ω load	18.0	-	27.0	Vp-p
Output Noise		V_{ON}	Differential, inhibited	-	-	10.0	mVp-p
Output Dynamic Offset Voltage	Direct coupled	V_{DYN}	35Ω load	-90	-	90	mV
	Transformer coupled	V_{DYN}	70Ω load	-250	-	250	mV
Output resistance		R_{OUT}	Differential, not transmitting	3	-	-	KΩ
Output Capacitance		C_{OUT}	1MHz sine wave	-	-	15	pF

3.6.2 AC Electrical characteristics

V_{DD} = 3.3V, -55°C ≤ T_A ≤ +125°C

Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
RECEIVER (Measured at Point «AT» in Figure 6)						
Receiver Delay	t_{DR}	From input zero crossing to RXA/B or $\overline{RXA/B}$	-	-	500[3]	ns
Receiver gap time	t_{RG}	Spacing between RXA/B and $\overline{RXAB}$ pulses	60[1]	-	430[2]	ns
Receiver Enable Delay	t_{REN}	From RXENA/B rising or falling edge to RXA/B or RXA/B	-	-	40	ns
TRANSMITTER (Measured at Point «AD» in Figure 5)						
Driver Delay	t_{DT}	TXA/B, $\overline{TXA/B}$ to BUSA/B, $\overline{BUSA/B}$	-	-	150	ns
Rise time	t_r	35Ω load	100	-	300	ns
Fall Time	t_f	35Ω load	100	-	300	ns
Inhibit Delay	t_{DI-H}	Inhibited output	-	-	100	ns
	t_{DI-L}	Active output	-	-	150	ns

[1]: Measured using a 1MHz sinusoid, 20V peak to peak, line to line at point «AT» (Guaranteed but not tested).

[2]: Measured using a 1 MHz sinusoid, 860 mV peak to peak, line to line at point «AT» (100% tested).

[3]: Measured using a 1 MHz sinusoid, 860 mV peak to peak, line to line at point «AT». Measured from input zero crossing point.

3.7 Applications

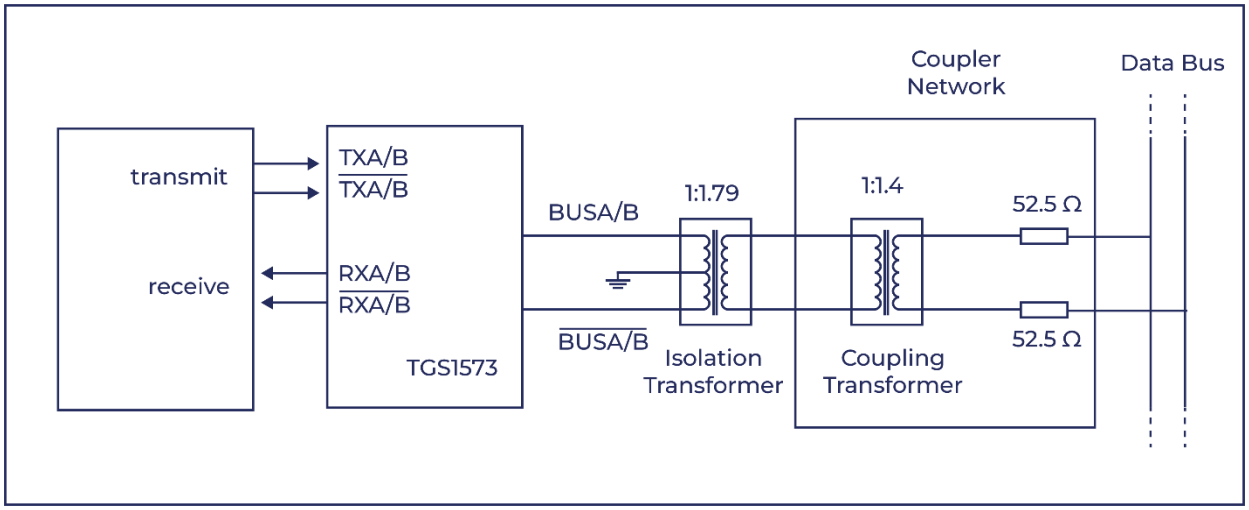
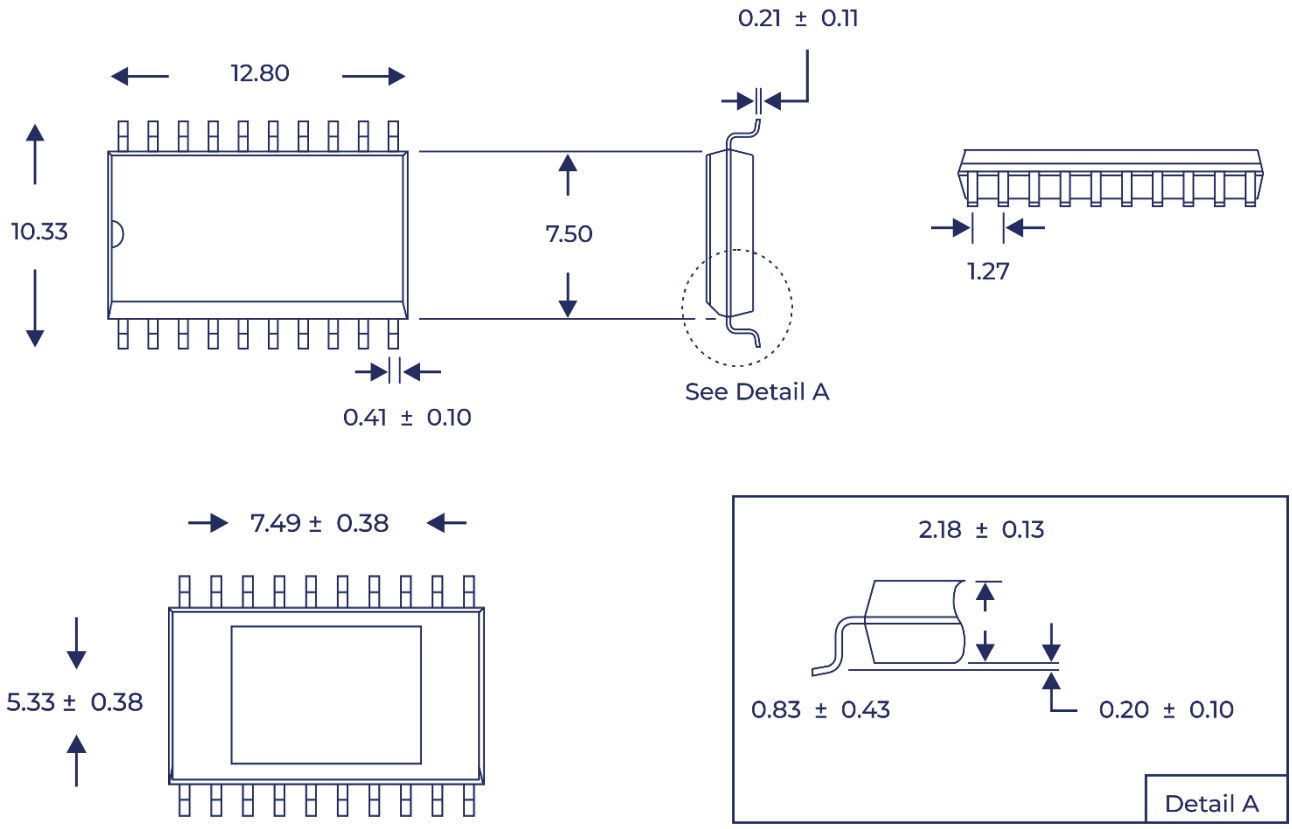


Fig.7 Application

4. Ordering information’s

Part Number	Operating Temperature	Package	Grade
TGS1573ESN1	-55°C to +125°C	ESOP-20	GJB7400 N1

5. Outlines



Product marking

First line: Part number model

Second line: Manufacturer date code*

Note*

YY - last two digits of the calendar year

WW - last two digits being the week of the year